National Semiconductor

July 1994

54VHC/74VHC74 • 54VHCT/74VHCT74
Dual D-Type Flip Flop with Preset and Clear

General Description

The VHC/VHCT74 is an advanced high speed CMOS Dual D-Flip Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to the Q OUTPUT during the positive going transition of the CK pulse. CLR and PR are independent of the CK and are accomplished by setting the appropriate input low.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

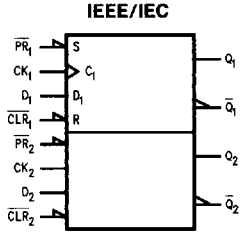
- High speed:
  VHC f_{MAX} = 170 MHz (typ) at V_{CC} = 5V
  VHCT f_{MAX} = 160 MHz (typ) at V_{CC} = 5V
- High noise immunity:
  VHC $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
  VHCT V_{IH} = 2.0V, V_{IL} = 0.8V
- Operating voltage:
  VHC V_{CC} (opr) = 2V ~ 5.5V
  VHCT V_{CC} (opr) = 4.5V–5.5V
- Power down protection:
  VHC inputs only
  VHCT inputs and outputs
- Low noise:
  VHC V_{OLP} = 0.3V (typ)
  VHCT V_{OLP} = ?V (typ)
- Low power dissipation:
  I_{CC} = 2 μA (max) at T_A = 25°C
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Pin and function compatible with 74HC/HCT74

NOTE:

ADD EXTERNAL PULL UP RESISTOR TO 'VHCT OUTPUTS TO DRIVE CMOS INPUTS
MILITARY SPECIFICATIONS ARE PRELIMINARY

Logic Symbol

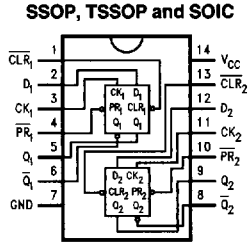
IEEE/IEC



TL/F/11505–1

Connection Diagrams

Pin Assignment for SSOP, TSSOP and SOIC



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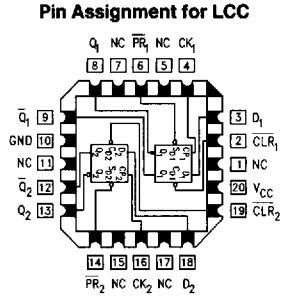
Pin Assignment for LCC



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Truth Table

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	Q_n	No Change

 TL/F/11505

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RRD-B20M114/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
VHC	−0.5V to V_{CC} + 0.5V
VHCT*	−0.5V to 7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	
VHC	±20 mA
VHCT	−20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
Soldering (10 seconds)	300°C

*V_{OUT} > V_{CC} only if output is in H state.

Note 1: *Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading varaibles. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
VHC	2.0V to 5.5V
VHCT	4.5V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
54VHC/VHCT	−55°C to +125°C
74VHC/VHCT	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V (VHC only)	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			54VHC T_A = −55°C to +125°C		74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.40 3.70		2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.50 0.50		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		80.0		20.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC		54VHC	74VHC	Units	Conditions
			$T_A = 25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Limits	Limits	Limits		
*V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.3	0.8			V	$C_L = 50$ pF
*V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.3	−0.8			V	$C_L = 50$ pF
*V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5			V	$C_L = 50$ pF
*V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5			V	$C_L = 50$ pF

*Parameter guaranteed by design.

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	74VHCT			54VHCT		74VHCT		Units	Conditions	
			$T_A = 25°C$			$T_A = -55°C$ to $+125°C$		$T_A = -40°C$ to $+85°C$				
			Min	Typ	Max	Min	Max	Min	Max			
V_{IH}	High Level Input Voltage	4.5	2.0					2.0		V		
		5.5	2.0					2.0				
V_{IL}	Low Level Input Voltage	4.5			0.8				0.8	V		
		5.5			0.8				0.8			
V_{OH}	High Level Output Voltage	4.5	3.15	3.65				3.15		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\ \mu A$
		4.5	2.5					2.4				$I_{OH} = -8$ mA
V_{OL}	Low Level Output Voltage	4.5		0.0	0.1				0.1	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\ \mu A$
		4.5			0.36				0.44			$I_{OL} = 8$ mA
I_{IN}	Input Leakage Current	0–5.5			±0.1				±1.0	μA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0				20.0	μA	$V_{IN} = V_{CC}$ or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35				1.50	mA	$V_{IN} = 3.4V$ Other Inputs = V_{CC} or GND	
I_{OPD}	Output Leakage Current (Power Down State)	0.0			+0.5				+5.0	μA	$V_{OUT} = 5.5V$	

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$		54VHCT $T_A = -55°C$ to $+125°C$	74VHCT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Limits	Limits	Limits		
*V_{OLP}	Quiet Output Maximum Dynamic V_{OL}						V	C_L = 50 pF
*V_{OLV}	Quiet Output Minimum Dynamic V_{OL}						V	C_L = 50 pF
*V_{IHD}	Minimum High Level Dynamic Input Voltage			2.0			V	C_L = 50 pF
*V_{ILD}	Maximum Low Level Dynamic Input Voltage			0.8			V	C_L = 50 pF

*Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			54VHC $T_A = -55°C$ to $+125°C$		74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	80	125				70		MHz	C_L = 15 pF
			50	75				45			C_L = 50 pF
		5.0 ± 0.5	130	170				110		MHz	C_L = 15 pF
			90	115				75			C_L = 50 pF
t_{PLH}, t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	3.3 ± 0.3		6.7	11.9			1.0	14.0	ns	C_L = 15 pF
				9.2	15.4			1.0	17.5		C_L = 50 pF
		5.0 ± 0.5		4.6	7.3			1.0	8.5	ns	C_L = 15 pF
				6.1	9.3			1.0	10.5		C_L = 50 pF
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	3.3 ± 0.3		7.6	12.3			1.0	14.5	ns	C_L = 15 pF
				10.1	15.8			1.0	18.0		C_L = 50 pF
		5.0 ± 0.5		4.8	7.7			1.0	9.0	ns	C_L = 15 pF
				6.3	9.7			1.0	11.0		C_L = 50 pF
C_{IN}	Input Capacitance			4	10				10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			25						pF	(Note 1)

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/2 (per F/F).

AC Operating Requirements for 'VHC

Symbol	Parameter	*V_{CC} (V)	74VHC T_A = 25°C		54VHC T_A = −55°C to +125°C	74VHC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Minimum				
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CK)	3.3 5.0		6.0 5.0		7.0 5.0	ns	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	3.3 5.0		6.0 5.0		7.0 5.0	ns	
t_S	Minimum Setup Time	3.3 5.0		6.0 5.0		7.0 5.0	ns	
t_H	Minimum Hold Time	3.3 5.0		0.5 0.5		0.5 0.5	ns	
t_{rem}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	3.3 5.0		5.0 3.0		5.0 3.0	ns	

*V_{CC} is 3.3 ±0.3V or 5.0 ±0.5V

AC Electrical Characteristics for 'VHCT

Symbol	Parameter	*V_{CC} (V)	74VHCT T_A = 25°C			54VHCT T_A = −55°C to +125°C		74VHCT T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	5.0	100	160				80		MHz	C_L = 15 pF
		5.0	80	140				65			C_L = 50 pF
t_{PLH}, t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	5.0		5.8	7.8			1.0	9.0	ns	C_L = 15 pF
		5.0		6.3	8.8			1.0	10.0		C_L = 50 pF
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	5.0		7.6	10.4			1.0	12.0	ns	C_L = 15 pF
		5.0		8.1	11.4			1.0	13.0		C_L = 50 pF
C_{IN}	Input Capacitance			4	10				10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			24						pF	(Note 1)

*V_{CC} is 5.0 ±0.5V

Note 1: C_{PD} is defined as the value of internal equivalent capacitance which is calculcated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr) = C_{PD} × V_{CC} × f_{IN} + I_{CC}/2 (per flip-flop).

AC Operating Requirements for 'VHCT

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$		54VHCT $T_A = -55°C$ to $+125°C$	74VHCT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Minimum				
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CK)	5.0 ± 0.5				5.0	ns	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		5.0		5.0	ns	
t_S	Minimum Setup Time	5.0 ± 0.5		5.0		5.0	ns	
t_H	Minimum Hold Time	5.0 ± 0.5		0		0	ns	
t_{rem}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		3.5		3.5	ns	

Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:

74 VHC 74 M X

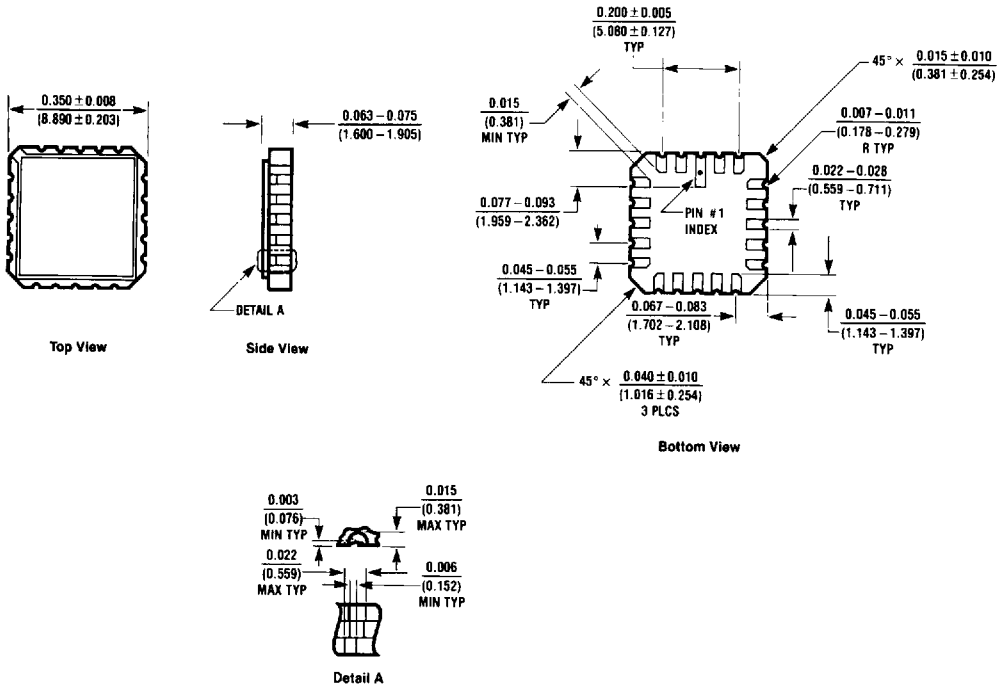
Temperature Range Family
- 74 VHC = Commercial VHC
- 54 VHC = Military VHC
- 74 VHCT = Commercial TTL-Compatible VHC
- 54 VHCT = Military TTL-Compatible VHC

Device Type

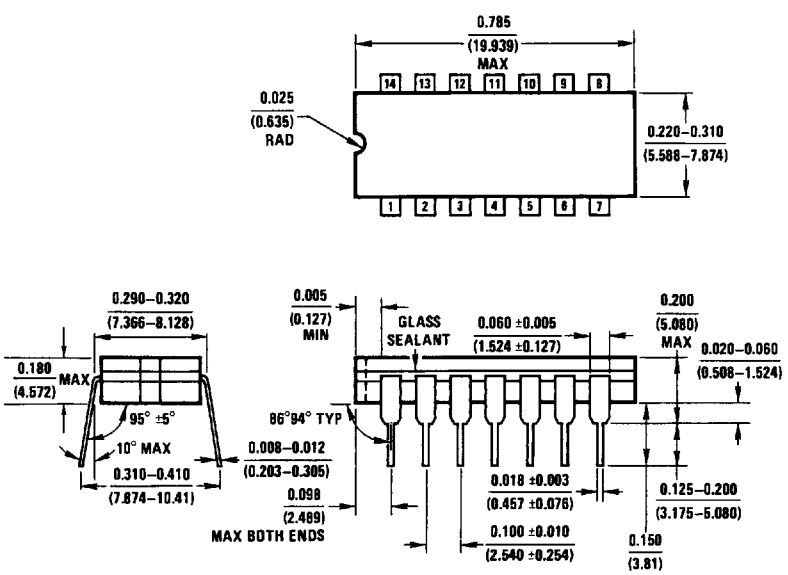
Package Code
- M = Small Outline JEDEC SOIC
- SJ = Small Outline EIAJ SOIC
- MSC = Shrink Small Outline EIAJ SSOP Type 1
- MTC = Thin Shrink Small Outline EIAJ TSSOP Type 1
- J/883 = Ceramic DIP
- W/883 = Ceramic Flatpak
- E/883 = Leadless Ceramic Chip Carrier

Special Variations
- "X" = Tape and Reel
- " " = Rail/Tube

Physical Dimensions inches (millimeters)

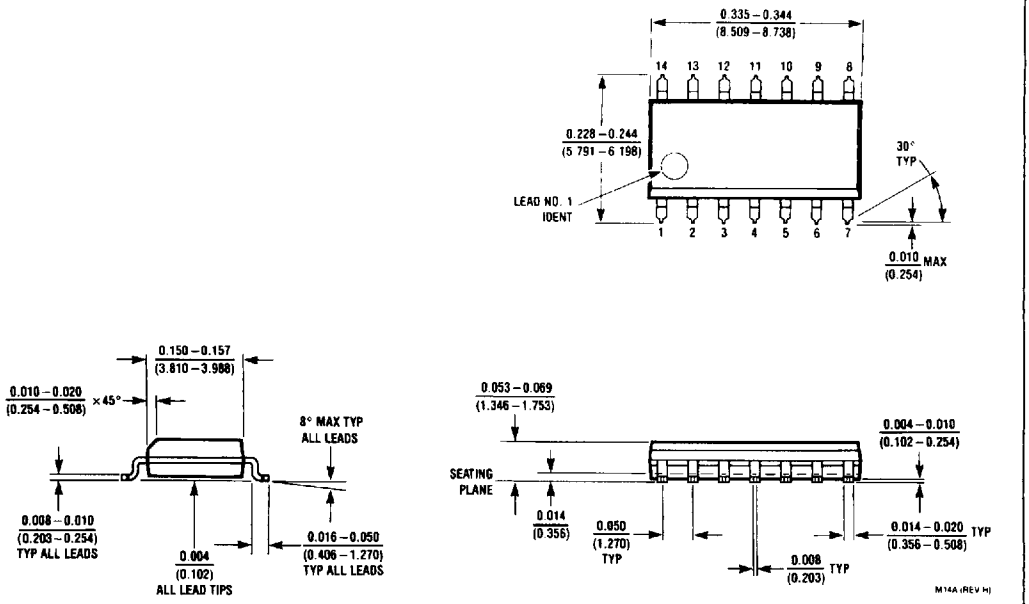


20-Lead Ceramic Leadless Chip Carrier, Type C (L)
Order Number 54VHC74E/883 or 54VHCT74E/883
NS Package Number E20A

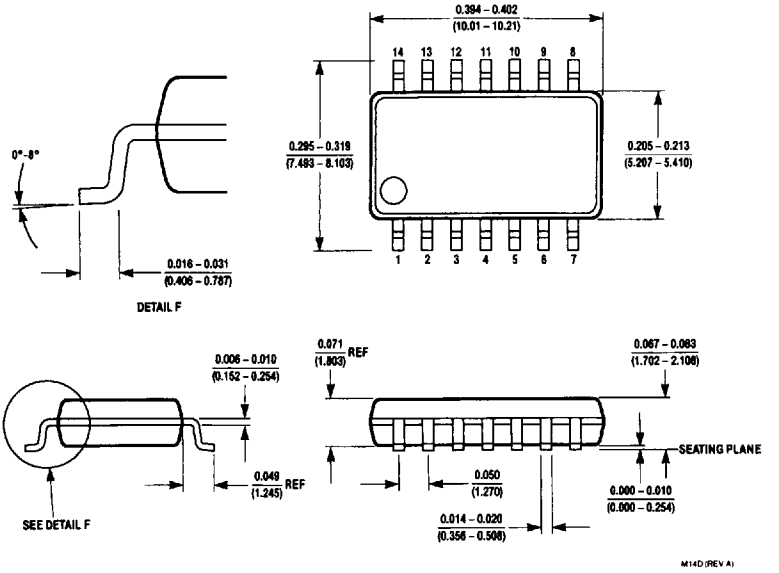


14-Lead Ceramic Dual-In-Line Package (D)
Order Number 54VHC74J/883 or 54VHCT74J/883
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

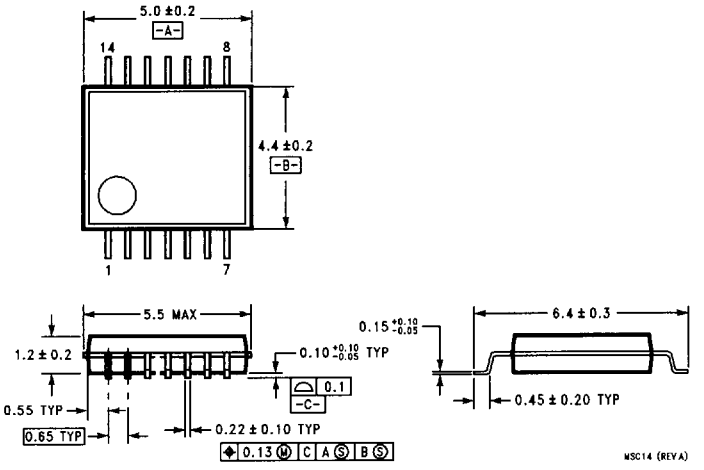


14-Lead Small Outline Integrated Circuit—JEDEC (M)
Order Number 74VHC74M, 74VHC74MX, 74VHCT74M or 74VHCT74MX
NS Package Number M14A

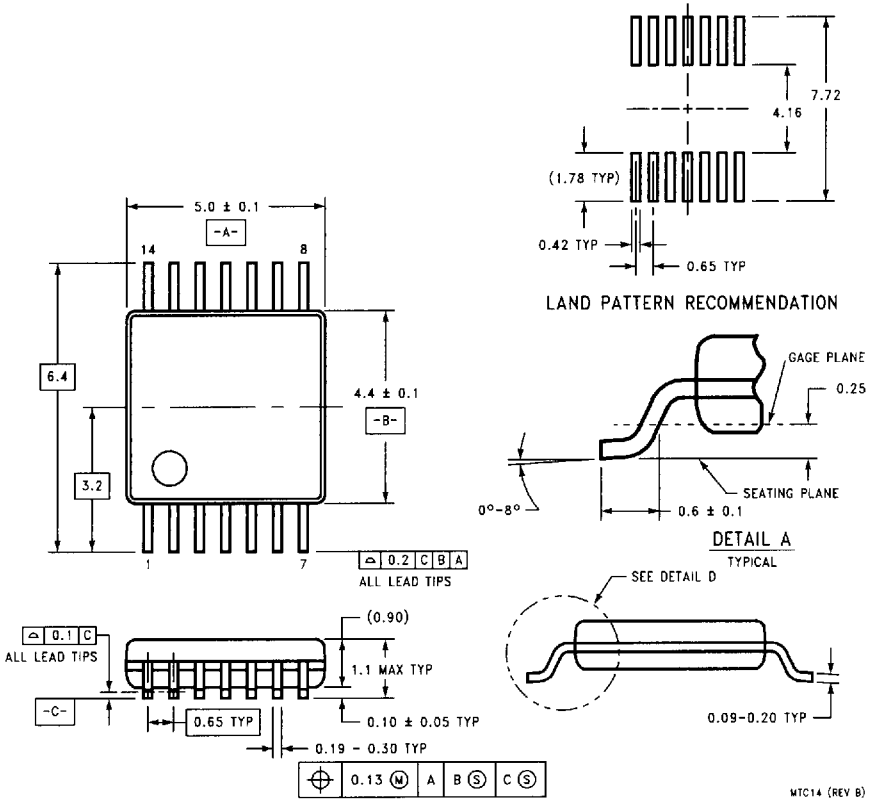


14-Lead Small Outline Package - EIAJ (SJ)
Order Number 74VHC74SJ, 74VHC74SJX, 74VHCT74SJ or 74VHCT74SJX
NS Package Number M14D

Physical Dimensions inches (millimeters) (Continued)



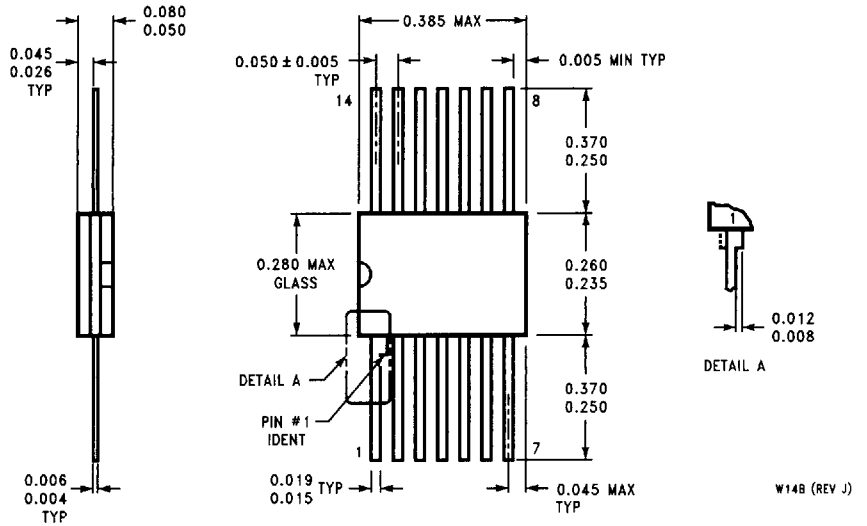
14-Lead Plastic EIAJ SSOP Type 1 (MSC)
Order Number 74VHC74MSCX or 74VHCT74MSCX
NS Package Number MSC14



14-Lead Plastic EIAJ TSSOP Type 1 (MTC)
Order Number 74VHC74MTC, 74VHC74MTCX, 74VHCT74MTC or 74VHCT74MTCX
NS Package Number MTC14

Physical Dimensions inches (millimeters) (Continued)

Lit. # 118050-002



14-Lead Cerpack (F)
Order Number 54VHC74W/883 or 54VHCT74W/883
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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