



8-Line Multiplexer

**ELECTRICALLY TESTED PER:
5962-8772901**

The 10H564 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

The 10H564 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The 10H564 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the 10H564 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional 10H564's.

- Propagation Delay, 1.5 ns Typical
- 455 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
V _{CC1}	1	5	2	GND
Enable	2	6	3	OPEN
X ₃	3	7	4	OPEN
X ₂	4	8	5	OPEN
X ₁	5	9	7	OPEN
X ₀	6	10	8	GND
A	7	11	9	OPEN
V _{EE}	8	12	10	V _{EE}
B	9	13	12	OPEN
C	10	14	13	OPEN
X ₄	11	15	14	OPEN
X ₅	12	16	15	OPEN
X ₆	13	1	17	OPEN
X ₇	14	2	18	OPEN
Z	15	3	19	51 Ω to V _{TT}
V _{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = -2.0 V MAX/ -2.2 V MIN

V_{EE} = -5.7 V MAX/ -5.2 V MIN

Military 10H564

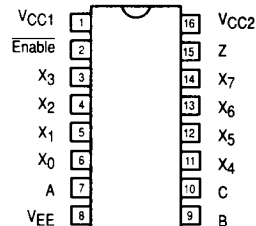


AVAILABLE AS

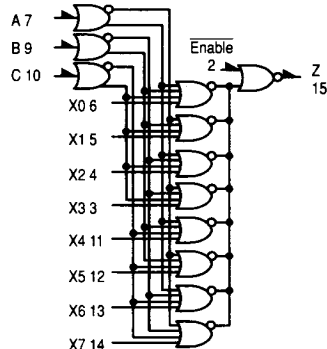
- 1) JAN: N/A
 - 2) SMD: 5962-8772901
 - 3) 883: 10H564/BXAJC
- X = CASE OUTLINE AS FOLLOWS:**

**PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

**The letter "M" appears before
the slash on LCC.**



LOGIC DIAGRAM

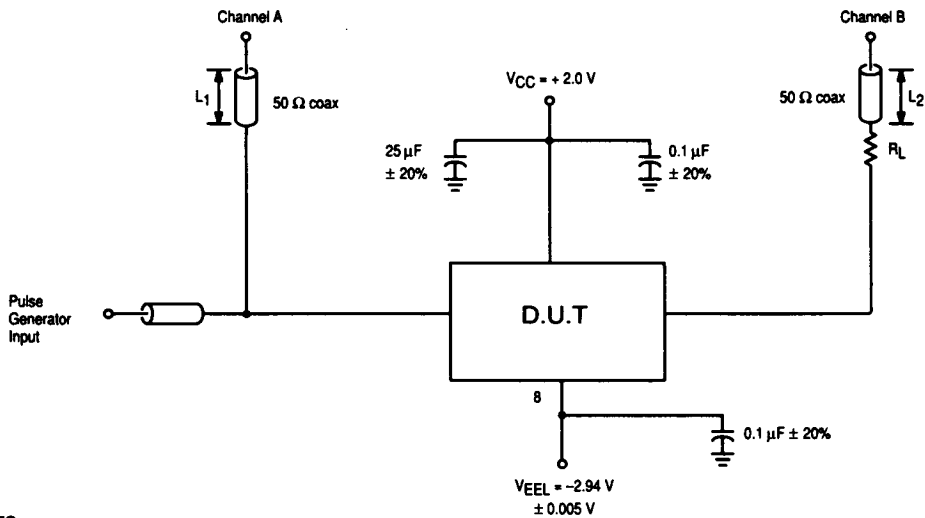


**10H564
TRUTH TABLE**

ENABLE	ADDRESS INPUTS			Z
	C	B	A	
L	L	L	L	X ₀
L	L	L	H	X ₁
L	L	H	L	X ₂
L	L	H	H	X ₃
L	H	L	L	X ₄
L	H	L	H	X ₅
L	H	H	L	X ₆
L	H	H	H	X ₇
H	Ø	Ø	Ø	L

Ø = Don't Care

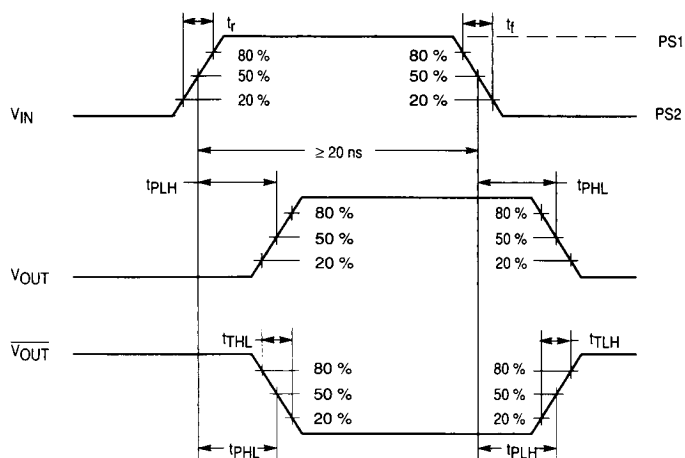
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NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. $R_L = 50 \Omega$.

Figure 1. Switching Test Circuit

**NOTES**

V_{IN} has the following characteristics:

1. $P_{\overline{V}} = 20$ ns.
2. $f_{IN} = 1.0$ MHz.
3. $t_r = t_f = 1.0$ ns $\pm$ 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H564 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EE1}	V _{EE2}	V _{EE1}	V _{EE2}
T _A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-5.46	-4.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-5.46	-4.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	VEE1	VEE2	VCC	P.U.T.
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 14	2, 9 10			8		1, 16	15
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	2, 7, 9 10, 14	2 - 7 9 - 14			8		1, 16	15
V _{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 13	2, 7, 9 10	3 - 5, 7 9 - 14	2, 7 9, 10	8		1, 16	15
V _{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	7, 9 10, 14	2, 7, 9 10	2	3 - 6 11 - 14	8		1, 16	15
I _{EE}	Power Supply Current	-75		-83		-83		mA					8		1, 16	8
I _{IH}	Input Current High		320		510		510	μA	2 - 7 9 - 14				8		1, 16	2 - 7, 9 - 14
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		2 - 7 9 - 14			8		1, 16	2 - 7, 9 - 14

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	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS ₁	PS ₂	VEE1	VEE2	VEEL	
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T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		PS2	VIN	VOUT	VCC	VEEL	PS1	P.U.T.	
tTLH	Rise Time	0.5	1.7	0.5	1.7	0.5	1.7	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tTHL	Fall Time	0.5	1.7	0.5	1.7	0.5	1.7	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tPLH	Propagation Delay Address to Output	1.45	2.7	1.6	3.2	1.4	2.6	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tPHL	Propagation Delay Address to Output	1.45	3.2	1.6	3.4	1.4	3.1	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tPLH	Propagation Delay Data to Output	1.0	2.3	1.15	2.6	1.0	2.2	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tPHL	Propagation Delay Data to Output	1.1	2.7	1.6	3.4	1.0	2.5	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tPLH	Propagation Delay Enable to Output	0.5	1.9	0.55	2.0	0.45	2.0	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	
tPHL	Propagation Delay Enable to Output	0.66	2.0	0.7	2.0	0.55	2.0	ns	2-7 9-14	2-7 9-14	15	1, 16	8	2-7 9-14	15	