1024Kx32 FLASH BALL GRID ARRAY *PRELIMINARY**

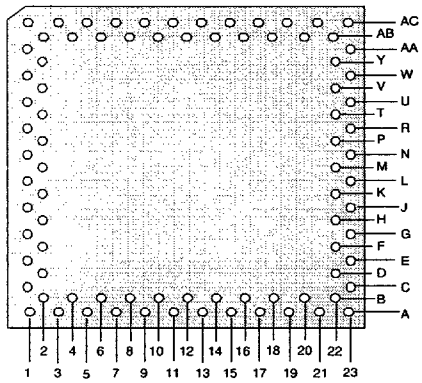
FEATURES

- Access Times of 90, 150ns
- Perimeter Ball Grid Packaging
  - 35mm BGA: pitch on same row - 0.120"
    pitch from row to row - 0.060"
  - Total I/O - 84 balls
  - Complies with JEDEC MO151, 35mm
- Sector Architecture
  - 16 equal size sectors of 64K bytes per each 1024Kx8 chip
  - Two step sequence of erase ensures that memory contents are not accidentally erased.
- 100,000 Erase/Program Cycles
- Organized as 1024Kx32
- Commercial and Industrial Temperature Ranges
- 5 Volt Power Supply, 12 V_{PP}
- Low Power CMOS
- Automated Byte Write and Block Erase
  - Command User Interface
  - Status Register
- Microsoft Flash File System (FFS)

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION FOR WPF1024K32-XPBX

BOTTOM VIEW



PIN DESCRIPTION

A_{0-19}	Address Inputs
D_{0-31}	Data Input/Output
$CE\#_{1-4}$	Chip Select
OE#	Output Enable
$WE\#_{1-4}$	Write Enable
$RY/BY\#_{1-4}$	Ready/Busy
$RP\#_{1-4}$	Reset/Power Down
V_{CC}	+5.0V Power
V_{SS}	Ground
V_{PP}	Program/Erase Supply
NC (WP#1-4)	Reserved for Addition of H/Ware Write Protect
NC	Not Connected

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PIN FUNCTIONS

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
A1	NC	B22	A11	AB22	OE#	AB2	A10
B2	A1	A23	A12	AC23	V_{PP}	AC1	A9
A3	A0	C23	A13	AC21	D15	AA1	A8
B4	D16	D22	A14	AB20	D14	Y2	A7
A5	D17	E23	A15	AC19	D13	W1	A6
B6	D18	F22	A16	AB18	D12	V2	NC (WP#2)
A7	D19	G23	NC (WP#3)	AC17	D11	U1	RP#2
B8	D20	H22	RP#3	AB16	D10	T2	RY/BY#2
A9	D21	J23	RY/BY#3	AC15	D9	R1	WE#2
B10	D22	K22	WE#3	AB14	D8	P2	CE#2
A11	D23	L23	CE#3	M22	GND	AC13	GND
N1	Vcc	A13	GND	N23	Vcc	AB12	Vcc
M2	GND	B12	Vcc	AC11	D7	L1	CE#1
B14	D24	P22	WE#4	AB10	D6	K2	WE#1
A15	D25	R23	CE#4	AC9	D5	J1	RY/BY#1
B16	D26	T22	RY/BY#4	AB8	D4	H2	RP#1
A17	D27	U23	RP#4	AC7	D3	G1	NC (WP#1)
B18	D28	V22	NC (WP#4)	AB6	D2	F2	A5
A19	D29	W23	A17	AC5	D1	E1	A4
B20	D30	Y22	A18	AB4	D0	D2	A3
A21	D31	AA23	A19	AC3	NC	C1	A2

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ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on Any Pin with Respect to GND (except V_{CC} and V_{PP})	-2.0 to +7.0	V
V_{PP} Program Voltage with Respect to GND during Block Erase/Byte Write	-2.0 to +14.0	V
V_{CC} Supply Voltage with Respect to GND	-2.0 to +7.0	V
Output Short Circuit Current	100	mA

NOTES:

1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a Stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp.	T_A	0	+70	°C

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
A_0-A_{18} Capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	40	pF
OE# Capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	20	pF
Write Enable Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	50	pF
Chip Select Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	20	pF
D_0 - D_{31} Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = V_{CC} to GND			10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{OUT} = V_{CC} to GND			10	µA
V_{CC} Standby Current	I_{CCS}	V_{CC} = 5.5, CS# = RP# = V_{IH}, f = 5mHz		3.0	8	mA
V_{CC} Read Current	I_{CCR}	V_{CC} = 5.5, CS# = V_{IL}, f = 5 MHz, I_{OUT} = 0mA		80	140	mA
V_{CC} Byte Write Current	I_{CCW}	Byte Write in Progress		30	120	mA
V_{CC} Block Erase Current	I_{CCE}	Block Erase in Progress		30	120	mA
V_{CC} Powerdown Current	I_{CCD}	RP# = GND, I_{OUT} (RY/BY#) = 0mA		1.0	10	µA
V_{PP} Standby Current	I_{PPS}	V_{PP} < V_{CC}		4	60	µA
V_{PP} Powerdown Current	I_{PPD}	RP# = GND		1.0	25	µA
V_{PP} Byte Write Current	I_{PPW}	V_{PP} = V_{PPH}, Byte Write in Progress		40	140	mA
V_{PP} Block Erase Current	I_{PPE}	V_{PP} = V_{PPH}, Block Erase in Progress		40	140	mA
Output Low Voltage	V_{OL}	V_{CC} = 4.5, I_{OL} = 5.8 mA			0.45	V
Output High Voltage	V_{OH}	V_{CC} = 4.5, I_{OH} = -2.5 mA	2.4			V
V_{PP} during Normal Operations	V_{PPL}[3]		0.0		6.5	V
V_{PP} during Erase/Write Operations	V_{PPH}		11.4	12.0	12.6	V
V_{CC} Erase/Write Lock Voltage	V_{LKO}		2.0			V

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. Valid for all speeds.
2. I_{CCES} is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block Erases/Byte Writes are inhibited when V_{PP} = V_{PPL} and not guaranteed in the range between V_{PPH} and V_{PPL}.
4. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - WE# CONTROLLED

Parameter	Symbol		-90		-150		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	10		10		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	40		40		ns
V_{PP} Setup Time (1)	t_{VPWH}	t_{VPS}	90		90		ns
Address Setup Time	t_{AVWH}	t_{AS}	40		40		ns
Data Setup Time	t_{DVWH}	t_{DS}	40		40		ns
Data Hold Time	t_{WHDX}	t_{DH}	5		5		ns
Address Hold Time	t_{WHAX}	t_{AH}	5		5		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	10		10		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		ns
Duration of Byte Write Operation (1,2,3)	t_{WHQV1}		6		6		µs
Duration of Block Erase Operation (1,2,3)	t_{WHQV2}		0.3		0.3		sec
Write Recovery before Read	t_{WHGL}		0		0		µs
Write Enable high to RY/BY# going low	t_{WHRL}			100		100	ns
RP# High Recovery Time	t_{PHWL}	t_{PS}	1.0		1.0		µs

NOTES:
1. Guaranteed by design, not tested.
2. The on-chip Write State Machine incorporates all byte write and block erase functions and overhead of the flash memory, this includes byte program and verify, block precondition and veify, erase and verify.
3. Byte write and block erase durations are measured to completion (SR. 7 = 1, RY/BY# = V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).

AC CHARACTERISTICS – WRITE OPERATION - CS# CONTROLLED (1)

Parameter	Symbol		-90		-150		Unit
			Min	Max	Min	Max	
Write Enable Cycle Time	t_{AVAV}	t_{WC}	90		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	60		60		ns
V_{PP} Setup Time (1)	t_{VPEH}	t_{VPS}	90		90		ns
Address Setup Time	t_{AVEH}	t_{AS}	40		40		ns
Data Setup Time	t_{DVEH}	t_{DS}	40		40		ns
Data Hold Time	t_{EHDX}	t_{DH}	5		5		ns
Address Hold Time	t_{EHAX}	t_{AH}	5		5		ns
Write Enable Hold Time	t_{EHWH}	t_{WH}			0		ns
Chip Select Pulse Width High	t_{EHEL}	t_{EPH}	30		30		ns
Duration of Byte Write Operation (3)	t_{EHQV1}		6		6		µs
Duration of Block Erase Operation (3)	t_{EHQV2}		0.3		0.3		sec
Write Recovery before Read	t_{EHGL}		0		0		µs
RP# High Recovery to CS# Low	t_{PHEL}	t_{PS}	1.0		1.0		ns
Chip Select High to RY/BY# going low	t_{EHRL}			100		100	µs

NOTES:
1. Chip-Select Controlled Writes: Write operations are driven by the valid combination of CS# and WE#. In systems where CS# defi nes the write pulsewidth (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CS# waveform.
2. Guaranteed by design, not tested.
3. Byte write and block erase durations are measured to completion (SR.7 = 1, RY/BY# = 1, V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).

AC CHARACTERISTICS – READ-ONLY OPERATIONS

Parameter	Symbol		-90		-150		Unit
			Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	90		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		90		150	ns
Chip Select to Output Valid (1)	t_{ELQV}	t_{CE}		90		150	ns
Output Enable to Output Valid (1)	t_{GLQV}	t_{OE}		50		70	ns
Chip Select to Output Low Z (2)	t_{ELQX}	t_{LZ}	0		0		ns
Chip Select High to Output High Z (2)	t_{EHQZ}	t_{HZ}		65		65	ns
Output Enable to Output Low Z (2)	t_{GLQX}	t_{OLZ}	0		0		ns
Reset to Output Valid	t_{PHQV}	t_{PWH}		400		400	ns
Output Enable High to Output High Z (2)	t_{GHQZ}	t_{DF}		50		50	ns
Output Hold from Addresses, CS# or OE# Change, Whichever is First [2]		t_{OH}	0		0		ns

NOTES:
1. OE# may be delayed up to t_{CE}-t_{OE} after the falling edge of CS# without impact on t_{CS}.
2. Guaranteed by design, not tested.

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FIG. 2 AC WAVEFORMS FOR WRITE-ERASE-PROGRAM OPERATIONS, WE# CONTROLLED

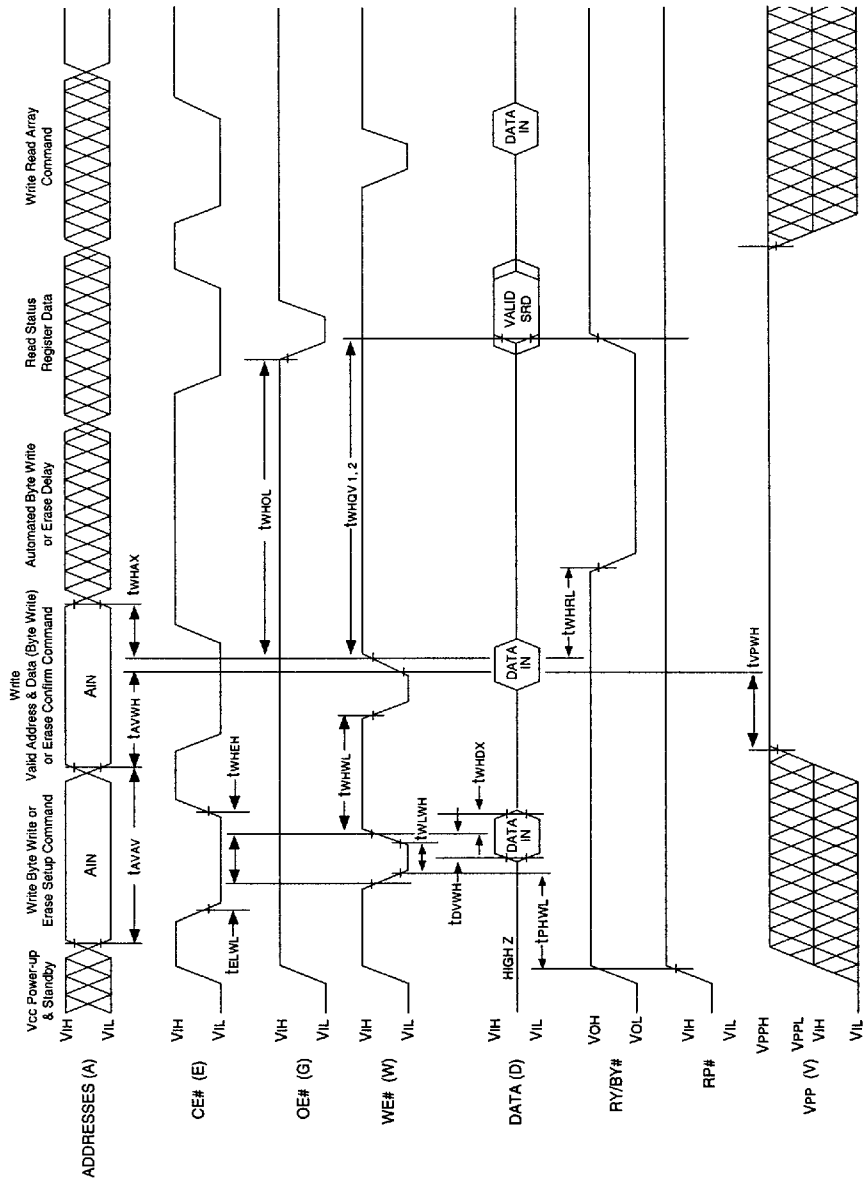

FIG. 3 ALTERNATE AC WAVEFORM FOR WRITE OPERATIONS - CS# CONTROLLED

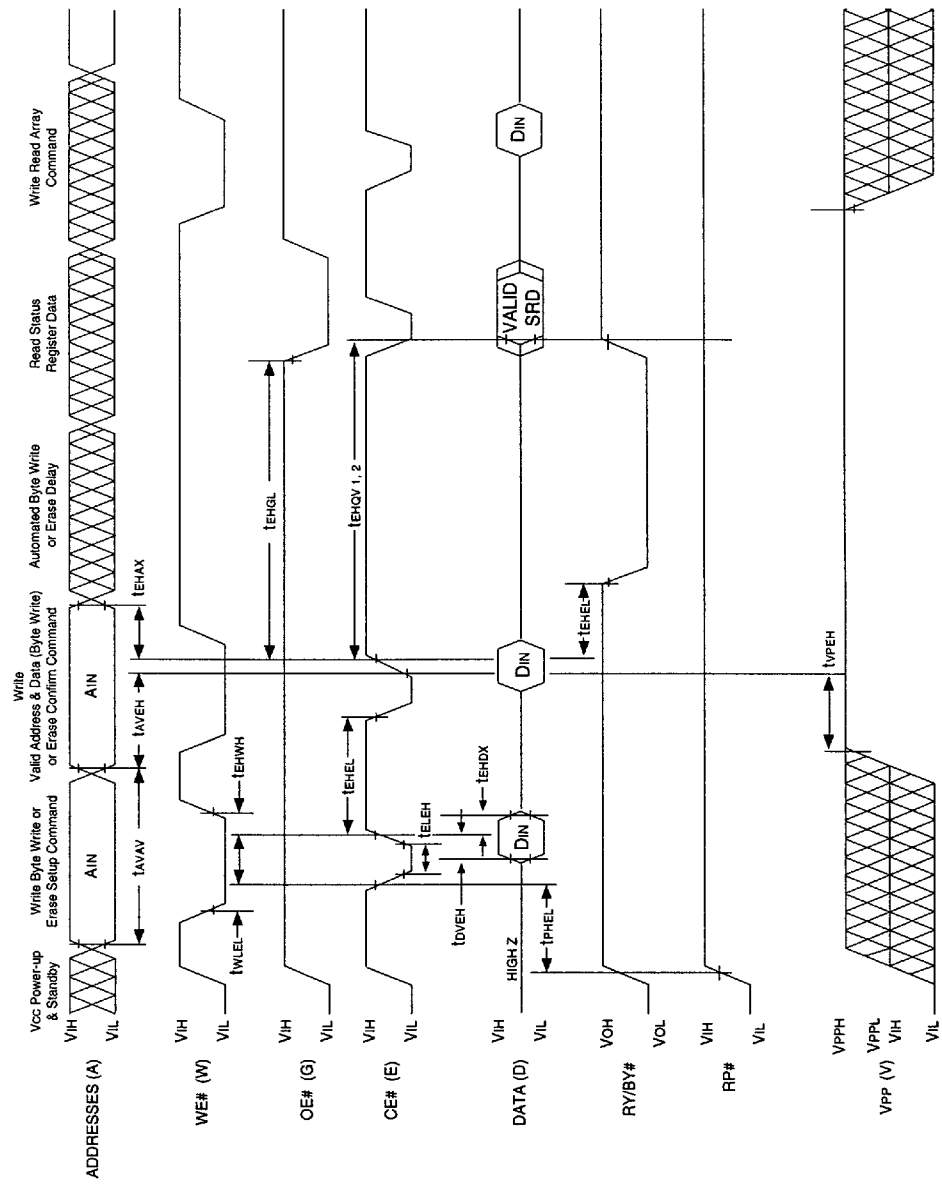

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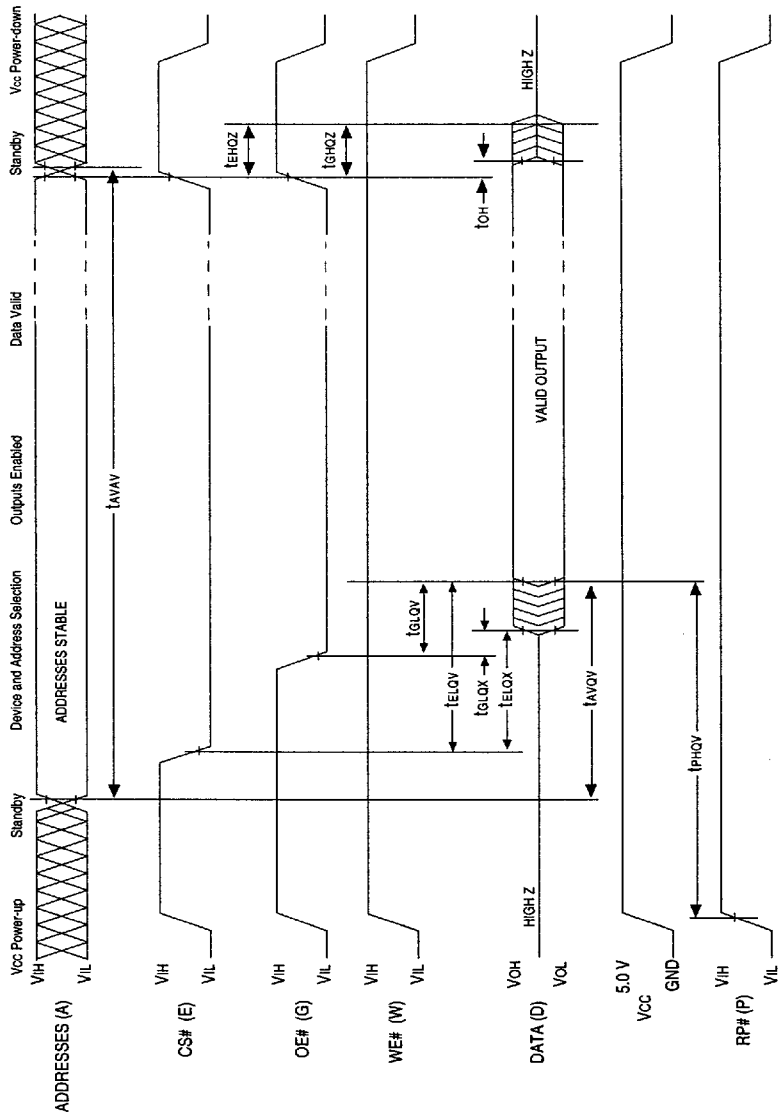
FIG. 4 AC WAVEFORM FOR READ OPERATIONS



PRINCIPLES OF OPERATION

The following Principles of Operation of the WS-1024K32-XPBX MCM is applicable to each of the four memory chips inside the MCM. Chip 1 is distinguished by CS#1 and I/O0-7, Chip 2 by CS#2 and I/O8-15, Chip 3 by CS3 and I/O16-23, and Chip 4 by CS#4 and I/O24-31.

The WPF1024K32-XPBX includes write automation to manage write and erase functions. The Write State Machine allows for 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with RAM-like interface timings.

After initial device powerup the WPF1024K32-XPBX functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. The status register can also be accessed through the command user interface when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables successful block erasure and byte writing of the device. Functions associated with altering memory contents—byte write, block erase—are accessed via the command user interface and verified thru the status register.

Commands are written using standard microprocessor write timings. Command user interface contents serve as input to the write status machine, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the device are again possible via the read array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

COMMAND USER INTERFACE AND WRITE AUTOMATION

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the Status Register on each of the four memory chips in the MCM. QFP options with RY/BY# also return progress via the Status Register for each of the four memory chips. Byte write is similarly controlled, after destination address and expected data are supplied.

DATA PROTECTION

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. Additionally, all functions are disabled whenever V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The two-step byte write/block erase command user interface write sequence provides additional software write protection.

BUS OPERATION

Flash memory reads, erase and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

The WPF1024K32-XPBX can be read from any of its blocks, and information can be read from the status register of each chip selected. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate read mode command to the command user interface. The device automatically resets to read array mode upon initial device powerup or after exit from deep powerdown. Chip select CS# is the device selection control, and when active enables the selected memory device. Output Enable (OE#) is the data input/output (D_0 - D_{31}) direction control, and when active drives data from the select memory onto the I/O bus. RP# and WE# must also be at V_{IH}. Figure 6 illustrates read bus cycle waveforms.

OUTPUT DISABLE

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (I/O0-31) are placed in a high-impedance state.

STANDBY

CS# at a logic-high level (V_{IH}) places the device in a standby mode. Standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (D_0 - D_{31}) are placed in a high-impedance state independent of the status of OE#. If the device is deselected during block erase or byte write, it will continue functioning and consuming normal active power until the operation is completed.

WRITE

Writes to the command user interface enable reading of device data. They also control inspection and cleaning of the status register. Additionally, when VPP = VPPH, the command user interface controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.

The command user interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase setup and erase confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The command user interface is written by bringing WE# to a logic-low level (VIL) while CS# is low. Address and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operation, Figures 4 and 5, for specific timing parameters.

COMMAND DEFINITIONS

When VPPL is applied to the VPP pin of the chip selected, read operations from the status register, or array blocks are enabled. Placing VPPH on VPP enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the command user interface of the chip selected. Table 2 defines the WPF1024K32-XPBX commands.

READ ARRAY COMMAND

Upon initial device powerup the device defaults to Read Array mode. This operation is also initiated by writing FFH into the command user interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command user interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when VPP = VPPL or VPPH.

TABLE 1 - BUS OPERATIONS

Mode	RP#	CS#	OE#	WE#	A0	VPP	D0-31	RY/BY#
Read (1,2,4)	VIH	VIL	VIH	X	X	DOUT	X	
Output Disable (4)	VIH	VIL	VIH	VIH	X	X	High Z	X
Standby (4)	VIH	VIH	X	X	X	High Z	X	
Deep Powerdown	VIL	X	X	X	X	X	High Z	VOH
Write (3,4)	VIH	VIL	VIH	VIL	X	X	DIN	X

NOTES:
1. Refer to DC Characteristics. When VPP = VPPL, memory contents can be read but not written or erased.
2. X can be VIL or VIH for control pins and addresses, and VPPL or VPPH for VPP. See DC Characteristics for VPPL and VPPH voltages.
3. Command writes involving block erase or byte write are only successfully executed when VPP = VPPH.
4. RY/BY# is VOL when WSM is executing internal Block Erase or Byte Write algorithms. It is VOH when WSM is not busy, in erase suspend mode or deep power-down mode.

TABLE 2 - COMMAND DEFINITIONS

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array/Reset	1	Write	X	FFH			
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H			
Erase Setup/Erase Confirm	2	Write	BA[1]	20H	Write	BA[1]	DOH
Erase Suspend/Erase Resume	2	Write	X	BOH	Write	X	DOH
Byte Write Setup/Write	2	Write	WA[1]	40H[3]	Write	WA[1]	WD[2]
Alternate Byte Write Setup/Write	2	Write	WA[1]	10H[3]	Write	WA[1]	WD[2]

NOTES:
1. BA = Address within the block being erased. WA = Address of memory location to be written.
2. SRD = Data read from status register. See Table 3 for a description of the status register bits. WD = Data to be written at location WA. Data is latched on the rising edge of WE#.
3. Either 40H or 10H are recognized by the WSM as the Byte Write Setup command.

TABLE 3
STATUS REGISTER DEFINITIONS

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy
SR.6 = ERASE SUSPENDED STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed
SR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase
SR.4 = BYTE WRITE STATUS
1 = Error in Byte Write
0 = Successful Byte Write
SR.3 = VPP STATUS
1 = VPP Low Detect; Operation Abort
0 = VPP OK
SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use and should be masked out when polling the status register.

NOTES:
The Write State Machine Status or RY/BY# bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success.

If the Byte Write and Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.

If V_{PP} low status is detected, the status register must be cleared before another byte write or block erase operation is attempted.

The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

READ STATUS REGISTER COMMAND

Each chip of the WPF1024K32-XPBX contains a status register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the read status register command (70H) to the command user interface. After writing this command, all subsequent read operations output data from the status register, until another valid command is written to the command user interface. The contents of the status register are latched on the falling edge of OE# or CS#, whichever occurs last in the read cycle. OE# or CS# must be toggled to V_{IH} before further reads to update the status register latch. The read status register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

CLEAR STATUS REGISTER COMMAND

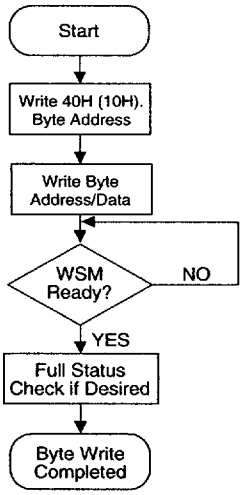
The erase status and byte write status bits are set to "1"s by the Write State Machine on each chip and can only be reset by the clear status register command. These bits indicate various failure conditions (see Table 3). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The status register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (SR.3) of the chip selected MUST be reset by system software before further byte writes or block erases are attempted. To clear the status register, the clear status register command (50H) is written to the command user interface. The clear status register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

ERASE SETUP/ERASE CONFIRM COMMANDS

Erase is executed one block at a time, initiated by a two-cycle command sequence. An erase setup command (20H) is first written to the command user interface, followed by the Erase Confirm command (DOH). These commands require both appropriate sequencing and address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two command erase sequence is written to it, the WPF1024K32-XPBX automatically outputs status register data when read (see Figure 8; Block Erase Algorithm). The CPU can detect the completion of the erase event by analyzing the output of the WSM Status bit of the status register.

FIG. 5
AUTOMATED BYTE WRITE ALGORITHM



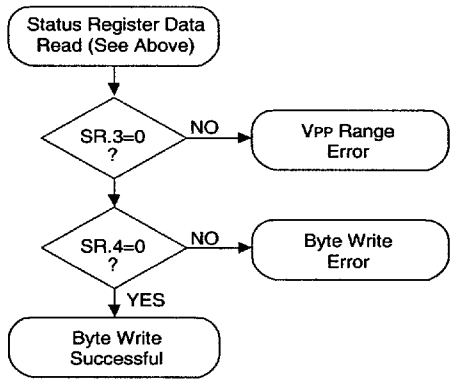
Bus Operation	Command	Comments
Write	Byte Write Setup	Data = 40H (10H) Address = Byte to be Written
Write	Byte Write	Data to be written Address = Byte to be Written
Standby/Read		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE# or CE# to update Status Register

Repeat for subsequent bytes

Full status check can be done after each byte or after a sequence of bytes

Write FFH after the last byte write operation to reset the device to Ready Array Mode

FULL STATUS CHECK PROCEDURE



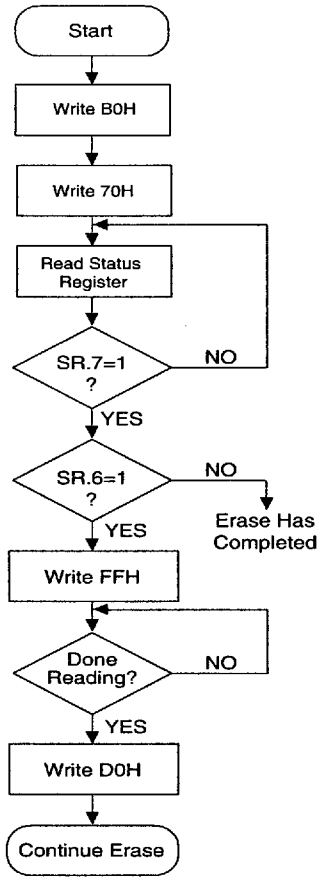
Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 Both 1 = Byte Write Error

SR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the clear status register command, in cases where multiple bytes are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

FIG. 6
ERASE SUSPEND/RESUME ALGORITHM



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H
Write	Read Status Register	Data = 70H
Standby/Read		Check RY/BY# bit VOH = Ready, VOL = Busy or Read Status Register
		Check SR.7 1 = Ready, 0 = Busy Toggle OE# or CE# to update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

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ERASE SUSPEND/ERASE RESUME COMMANDS

The erase suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the erase suspend command (B0H) to the command user interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The WPF1024K32-XPBX continues to output status register data when read, after the erase suspend command is written to it. Polling the WSM status and erase suspend status bits will determine when the erase operation has been suspended (both will be set to "1").

At this point, a read array command can be written to the command user interface to read data from blocks other than that which is suspended. The only other valid commands at this time are read status register (70H) and erase resume (D0H), at which time the WSM will continue with the erase process. The erase suspend status and WSM status bits of the status register will be automatically cleared. After the erase resume command is written to it, the device automatically outputs status register data when read (see Figure 9). V_{PP} must remain at V_{PPH} while in erase suspend.

VCC, VPP, RP TRANSITIONS AND THE COMMAND/STATUS REGISTERS

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} Status bit of the Status Register (SR.3) is set to "1", a Clear Status Register command MUST be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (SR.4) or Erase (SR.5) Status bits of the Status Register will be set to "1"s if error is detected. RP# transitions to V_{IL} during byte write and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device poweroff, or RP# transitions to V_{IL}, clear the Status Register to initial value 10000 for the upper 5 bits.

The Command User Interface latches commands as issued by system software and is not altered by V_{PP} or CS# transitions or WSM actions. Its state upon powerup, after exit from deep powerdown or after V_{CC} transitions below V_{LKO}, is Read Array Mode.

After byte write or block erase is complete, even after V_{PP} transitions down to V_{PPL}, the Command User interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

POWER UP/DOWN PROTECTION

The WPF1024K32-XPBX is designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the device ensures that the Command User interface is reset to the Read Array mode on power up.

POWERDOWN AND RESET

The WPF1024K32-XPBX offers a deep power-down feature, entered when RP# is a V_{IL}. Current draw thru V_{CC} is 0.8 µA typical in deep power-down mode, with current draw through V_{PP} typically 0.4 µA. During read modes, RP#-low deselects the memory, places output drivers in a high-impedence state and turns off all internal circuits. The device requires time t_{PWH} (see AC Characeristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command User Interface is reset to Read Array, and the upper 5 bits of the Status Register are cleared to value 10000, upon return to normal operation.

During block erase or bytewrite modes. RP# low will abort either operaton. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time t_{PS} after RP# goes to logic-high (V_{IH}) is required before another command can be written.

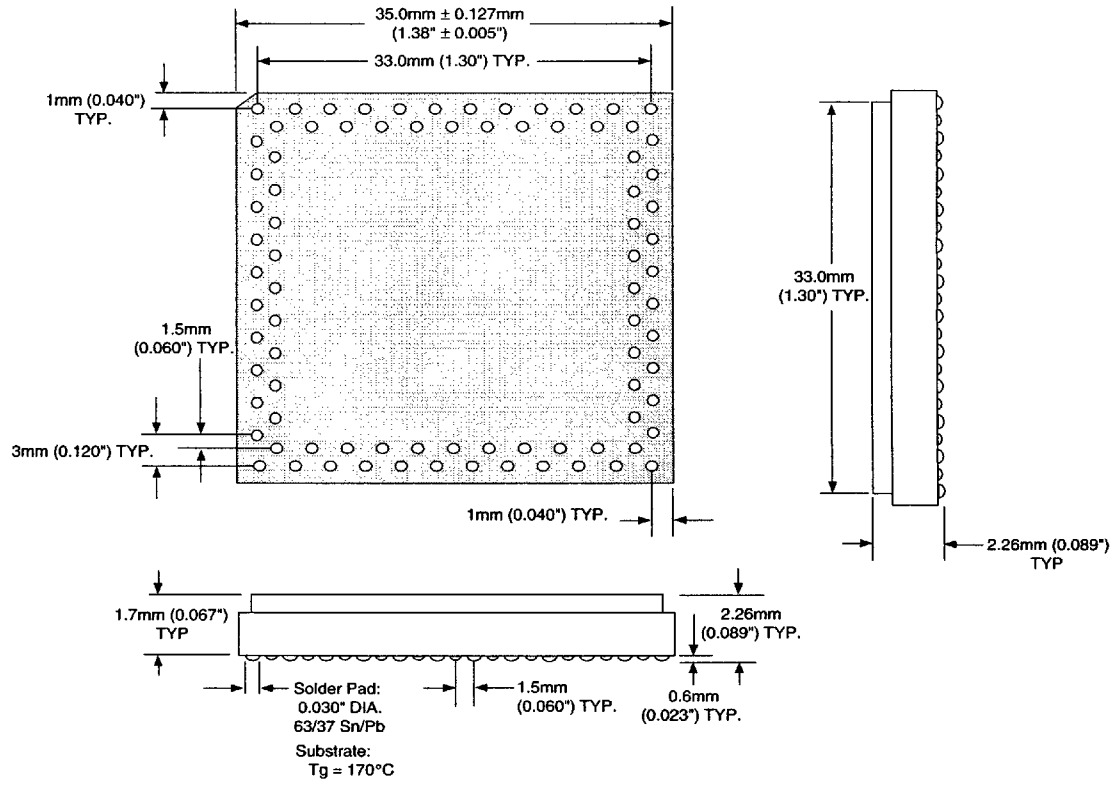
This use of RP# during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during write/erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur beause the flash memory would be providing the status information instead of array data. These flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application RP# is controlled by the same RESET# signal that resets the system CPU.

RY/BY# AND BYTE WRITE/BLOCK ERASE POLLING

RY/BY# is a full CMOS output that provides a hardware method of detecting byte write and block erase completion. It transitions low time t_{WHRL} after a write or erase command sequence is written to the device, and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to the interrupt input of the system CPU or controller. It is active at all times, not tristated if the device CS# or OE# inputs are brought to V_{IH}. RY/BY# is also V_{OH} when the device is in Erase Suspend or deep powerdown modes.

FIG. 7
PACKAGE DIMENSION



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