

7-75-57



# HD-6409

CMOS Manchester  
Encoder-Decoder (MED)

HD-6409

## Features

- Converter or Repeater Mode
- Independent Manchester Encoder and Decoder Operation
- Static to One Megabit/sec Data Rate Guaranteed
- Low Bit Error Rate
- Digital PLL Clock Recovery
- On Chip Oscillator
- Low Operating Power: 50mW at +5V Supply
- Two Temperature Ranges Available
  - ▶ HD-6409-9..... -40°C to +85°C
  - ▶ HD-6409-2/-8..... -55°C to +125°C

## Description

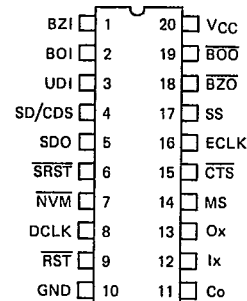
The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409 easily interfaces to protocol controllers.

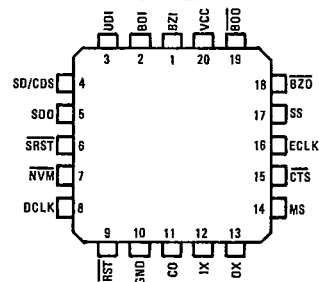
## Pinout

TOP VIEW



## LCC

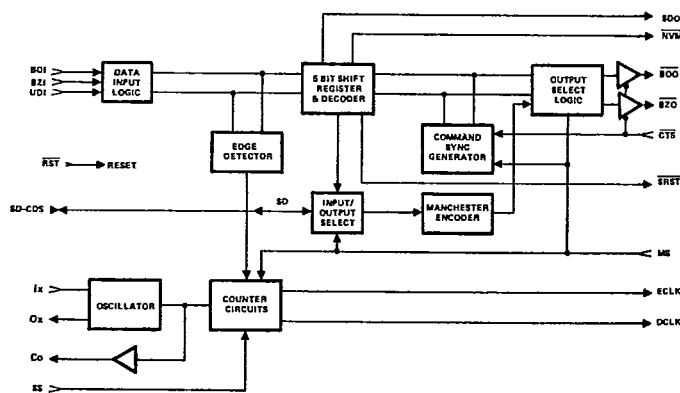
TOP VIEW



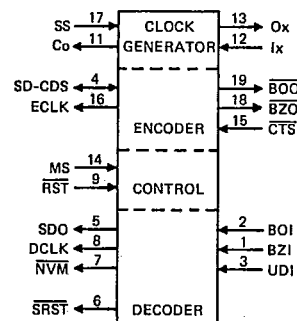
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## Functional Diagram



## Logic Symbol



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

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**Pin Description**

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
1	I	BZI	Bipolar Zero Input	Used in conjunction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder, BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2	I	BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder, BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3	I	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4	I/O	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5	O	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{RST}$ is low.
6	O	SRST	Serial Reset	In the converter mode, $\overline{SRST}$ follows $\overline{RST}$ . In the repeater mode, when $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero, and a valid synchronization sequence is received.
7	O	$\overline{NVM}$	Nonvalid Manchester	A low on $\overline{NVM}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{NVM}$ is set low by a low on $\overline{RST}$ , and remains low after $\overline{RST}$ goes high until valid sync pulse followed by two valid Manchester bits is received.
8	O	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI to synchronously output received NRZ data (SDO).
9	I	$\overline{RST}$	Reset	In the converter mode, a low on $\overline{RST}$ forces SDO, DCLK, $\overline{NVM}$ , and $\overline{SRST}$ low. A high on $\overline{RST}$ enables SDO and DCLK, and forces $\overline{SRST}$ high. $\overline{NVM}$ remains low after $\overline{RST}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{RST}$ has the same effect on SDO, DCLK and $\overline{NVM}$ as in the converter mode. When $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero and a valid synchronization sequence is received.

(I) — Input  
(O) — Output

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**Pin Description**

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
10	I	GND	Ground	Ground
11	O	Co	Clock Output	Buffered output of clock input Ix. May be used as clock signal for other peripherals.
12	I	Ix	Clock Input	Ix is the input for an external clock or, if the internal oscillator is used, Ix and Ox are used for the connection of the crystal.
13	O	Ox	Clock Drive	If the internal oscillator is used, Ox and Ix are used for the connection of the crystal.
14	I	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15	I	CTS	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$ , $\overline{BZO}$ high and ECLK low. A high to low transition of CTS initiates transmission of a Command sync pulse. A low on CTS enables $\overline{BOO}$ , $\overline{BZO}$ , and ECLK. In the repeater mode, the function of CTS is identical to that of the converter mode with the exception that a transition of CTS does not initiate a synchronization sequence.
16	O	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
17	I	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18	O	$\overline{BZO}$	Bipolar Zero Output	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19	O	$\overline{BOO}$	Bipolar One Out	See pin 18.
20	I	VCC	VCC	VCC is the +5V power supply pin. A 0.1 $\mu$ F decoupling capacitor from VCC (pin-20) to GND (pin-10) is recommended.

(I)—Input  
(O)—Output

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## Specifications HD-6409

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## Absolute Maximum Ratings

Supply Voltage.....	+7.0 Volts	$\theta_{JA}$ .....	91°C/W (CERDIP Package), 96°C/W (LCC Package)
Input, Output or I/O Voltage Applied.....	GND -0.3V to VCC +0.3V	Gate Count.....	250 Gates
Maximum Package Power Dissipation.....	1 Watt	Junction Temperature.....	+150°C
Storage Temperature Range.....	-65°C to +150°C	Lead Temperature (Soldering, Ten Seconds).....	+275°C
$\theta_{JC}$ .....	32°C/W (CERDIP Package), 37°C/W (LCC Package)		

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

## Operating Conditions

Operating Voltage Range.....	+4.5V to +5.5V
Operating Temperature Range.....	
HD-6409-9.....	-40°C to +85°C
HD-6409-2/-8.....	-55°C to +125°C

## Electrical Specifications

VCC = 5V  $\pm$  10%; GND = 0V; T<sub>A</sub> = -40°C to +85°C (HD-6409-9);  
T<sub>A</sub> = -55°C to +125°C (HD-6409-2)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
DC	V <sub>IH</sub>	Logic-1 Input Voltage	70% VCC		V	V <sub>IN</sub> = V <sub>CC</sub> or GND DIP Pins 1-4, 9, 12, 14, 15, 17 I <sub>OH</sub> = -2.0mA I <sub>OL</sub> = 2.0mA V <sub>IN</sub> = V <sub>CC</sub> = 5.5V V <sub>CC</sub> = 5.5V, f <sub>CO</sub> = 16MHz
	V <sub>IL</sub>	Logic-0 Input Voltage		20% VCC	V	
	V <sub>IHR</sub>	Logic-1 Input Voltage (Reset)	VCC -0.5		V	
	V <sub>ILR</sub>	Logic-0 Input Voltage (Reset)		GND +0.5	V	
	V <sub>IHC</sub>	Logic-1 Input Voltage (Clock)	VCC -0.5		V	
	V <sub>ILC</sub>	Logic-0 Input Voltage (Clock)		GND +0.5	V	
	I <sub>I</sub>	Input Leakage	-1.0	+1.0	$\mu$ A	
	V <sub>OH</sub>	Logic-1 Output Voltage	VCC -0.4		V	
	V <sub>OL</sub>	Logic-0 Output Voltage		0.4	V	
	I <sub>CCQ</sub>	Supply Current Quiescent		1.0	$\mu$ A	
AC	I <sub>CCOP</sub>	Supply Current Operating*		7.0	mA	I <sub>X</sub> or X <sub>TAL</sub>  CL = 20pF for Co, 50pF Otherwise 50ns Maximum TCYCLE = 62ns, Fig. 6 TCYCLE = 62ns, Fig. 6
	(1) f <sub>C</sub>	Clock Frequency		16	MHz	
	(2) t <sub>C</sub>	Clock Period		1/f <sub>C</sub>	s	
	(3) t <sub>1</sub>	Bipolar Pulse Width	t <sub>C</sub> -10		ns	
	(4) t <sub>2</sub>	Sync Transition Span		1.5 x CR x t <sub>C</sub> ① ②	ns	
	(5) t <sub>3</sub>	One-Zero Overlap		t <sub>C</sub> -10	ns	
	(6) t <sub>4</sub>	Short Data Transition Span		0.5 x CR x t <sub>C</sub> ① ②	ns	
	(7) t <sub>5</sub>	Long Data Transition Span		CR x t <sub>C</sub>	ns	
	(8) t <sub>6</sub>	Output Rise & Fall Time		50	ns	
	(9) t <sub>7</sub>	Clock Out Co Rise & Fall Time		1/(5 x f <sub>C</sub> )	s	
	(10) t <sub>8</sub>	Input Rise & Fall Time		1/(5 x f <sub>C</sub> )	s	
	(11) t <sub>9</sub>	Clock High Time	20		ns	
		Clock Low Time	20		ns	

## CONVERTER MODE

ENCODER SECTION							
AC	(12) t <sub>CE1</sub>	SD Setup Time	120			ns	
	(13) t <sub>CE2</sub>	SD Hold Time	0			ns	
	(14) t <sub>CE3</sub>	SD to BZO, BOO Prop Delay		1	1.5	DBP	
	(15) t <sub>CE4</sub>	CTS Low to BZO, BOO Enabled		1	1.5	DBP	
	(16) t <sub>CE5</sub>	CTS Low to ECLK Enabled		10.5		DBP	
	(17) t <sub>CE6</sub>	CTS High to ECLK Disabled		1.0	1.5	DBP	
	(18) t <sub>CE7</sub>	CTS High to BZO, BOO Disabled		2.0	2.5	DBP	
DECODER SECTION							
AC	(19) t <sub>CD1</sub>	UDI to SDO, NVM	2.5		3	DBP ①	
	(20) t <sub>CD2</sub>	DCLK to SDO, NVM			40	ns	
	(21) t <sub>CD3</sub>	RST Low to DCLK, SDO, NVM Low		0.5	1.5	DBP ①	CL = 50pF
	(22) t <sub>CD4</sub>	RST High to DCLK Enabled		0.5	1.5	DBP ①	CL = 50pF
REPEATER MODE							
AC	(23) t <sub>R1</sub>	UDI to BOO, BZO		1		DBP ①	
	(24) t <sub>R2</sub>	ECLK to BZO			40	ns	
	(25) t <sub>R3</sub>	UDI to SDO, NVM	2.5		3	DBP ①	

NOTES: ① CR — Clock Rate, either 16X or 32X.  
② t<sub>C</sub> = 1/f<sub>C</sub>  
③ DBP — Data Bit Period, CR = 16X, one DBP = 16 clock cycles; CR = 32X, one DBP = 32 clock cycles  
\* Guaranteed and sampled but not 100% tested.

Capacitance T<sub>A</sub> = +25°C, Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNIT	TEST CONDITIONS
C <sub>IN</sub>	Input Capacitance	6.0	pF	All measurements are referenced to device GND
C <sub>OUT</sub>	Output Capacitance	8.0	pF	

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**Converter Mode****ENCODER OPERATION**

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock 1X for internal timing.  $\overline{CTS}$  is used to control the encoder outputs, ECLK,  $\overline{BOO}$  and  $\overline{BZO}$ . A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on  $\overline{CTS}$  enables encoder outputs ECLK,  $\overline{BOO}$  and  $\overline{BZO}$ , while a high on  $\overline{CTS}$  forces  $\overline{BZO}$ ,  $\overline{BOO}$  high and holds ECLK low. When  $\overline{CTS}$  goes from high to low ①, a synchronization sequence is transmitted out on  $\overline{BOO}$  and  $\overline{BZO}$ . A synchronization sequence consists of eight Manchester

"0" bits followed by a command sync pulse. ② A command sync pulse is a three bit wide pulse with the first 1½ bits high followed by 1½ bits low. ③ Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on  $\overline{BOO}$  and  $\overline{BZO}$  following the command sync pulse. ④ Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by  $\overline{CTS}$ . Manchester data out is inverted.

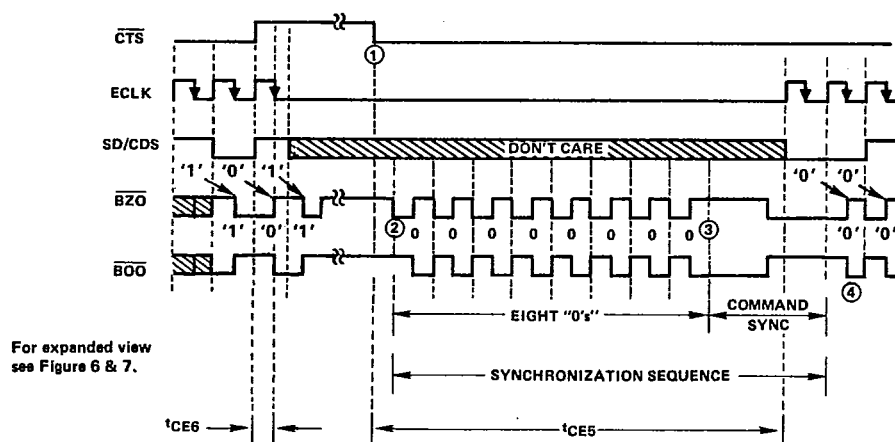


FIGURE 1.

**DECODER OPERATION**

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data i.e. Bipolar One Out through an inverter to Unipolar Data Input. The decoder continuously monitors this data input for a valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a three bit delay between UDI, BOI or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the  $\overline{RST}$  pin. When  $\overline{RST}$  is low, SDO, DCLK and  $\overline{NVM}$  are forced low. When  $\overline{RST}$  is high, SDO is transmitted out synchronously with the recovered clock DCLK. The  $\overline{NVM}$  output remains low after a low to high transition on  $\overline{RST}$  until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every high to low transition of this clock.

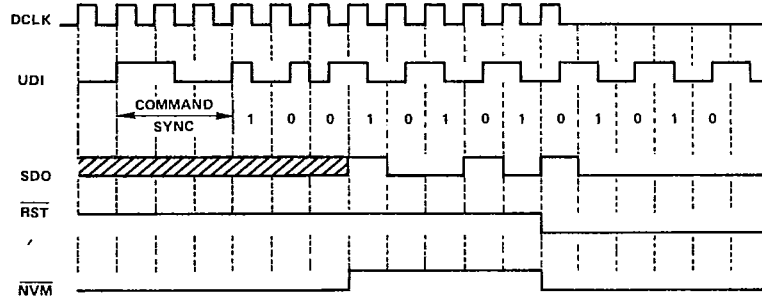
Three bit periods after an invalid Manchester bit is received on, UDI, or BOI,  $\overline{NVM}$  goes low synchronously with the questionable data output on SDO. FURTHER, THE DECODER DOES NOT REESTABLISH PROPER DATA DECODING UNTIL ANOTHER SYNC PATTERN IS RECOGNIZED

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For expanded view see Figure 9.

FIGURE 2.

### Repeater Mode

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only non-inverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs BOO and BZO. The 2X ECLK is transmitted out of the repeater synchronously with BOO and BZO.

A low on  $\overline{\text{CTS}}$  enables ECLK, BOO, and BZO. In contrast to the converter mode, a transition on  $\overline{\text{CTS}}$  does not initiate a synchronization sequence of eight 0's and a command sync. The repeater mode does recognize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When  $\overline{\text{RST}}$  is low, the outputs SDO, DCLK, and  $\overline{\text{NVM}}$  are low, and  $\overline{\text{SRST}}$  is set low.  $\overline{\text{SRST}}$  remains low after  $\overline{\text{RST}}$  goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. The reset bit is the first data bit after the sync pulse. With  $\overline{\text{RST}}$  high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

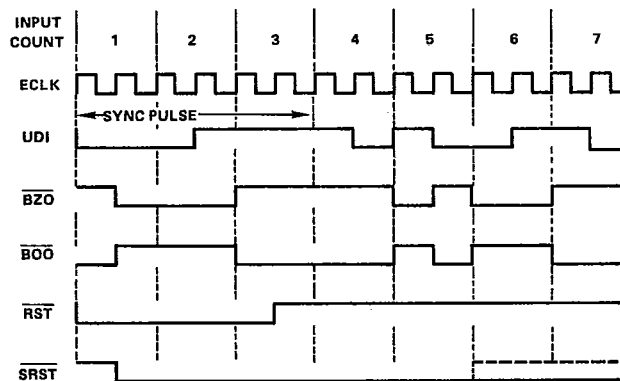


FIGURE 3.

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## Switching Waveforms

NOTE: UDI = 0, FOR NEXT DIAGRAMS

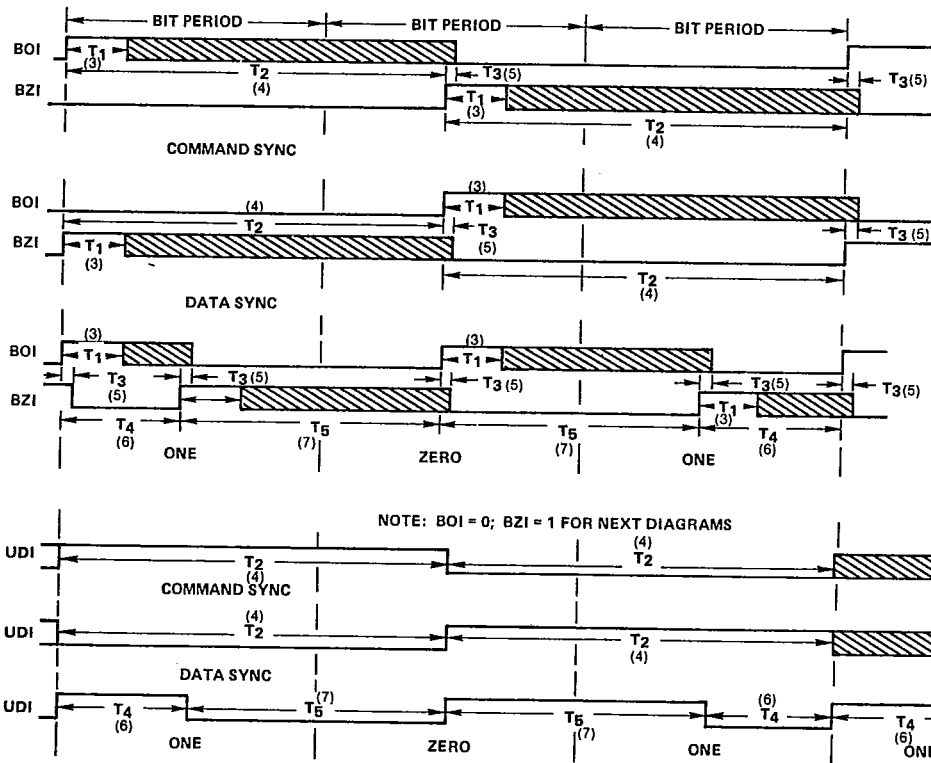


FIGURE 4.

## A.C. Testing Input, Output Waveform

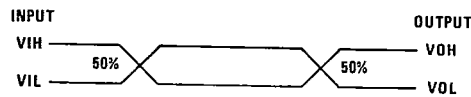


FIGURE 5.

A.C. Testing: All input signals must switch between  $V_{IL}$  and  $V_{IH}$ . Input rise and fall times are driven in 1nsec per volt.

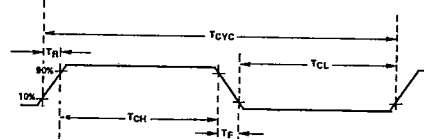


FIGURE 6.

NOTE: Reference parameters  $t_6$ ,  $t_7$ ,  $t_8$ ,  $t_9$

## Encoder Timing

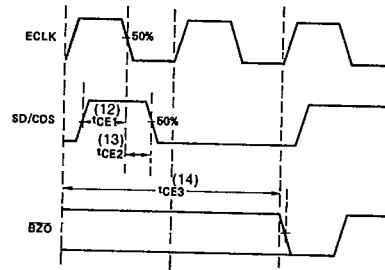


FIGURE 7.

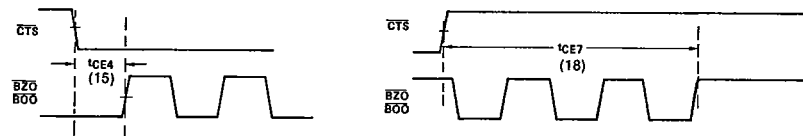
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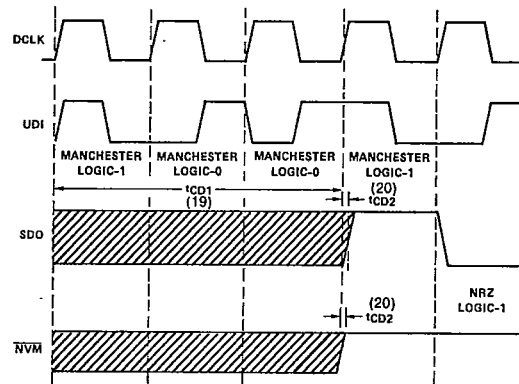
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NOTE:  $t_{CE5}$  - See Figure 1  
 $t_{CE6}$  - See Figure 1

FIGURE 8.

**Decoder Timing**

NOTE: Manchester Data In is not synchronous with Decoder Clock.  
 Decoder Clock is synchronous with decoded NRZ out of SDO.

FIGURE 9.

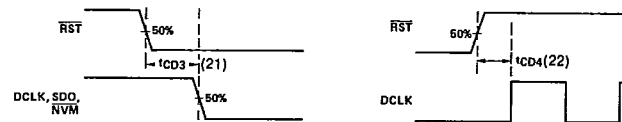


FIGURE 10.

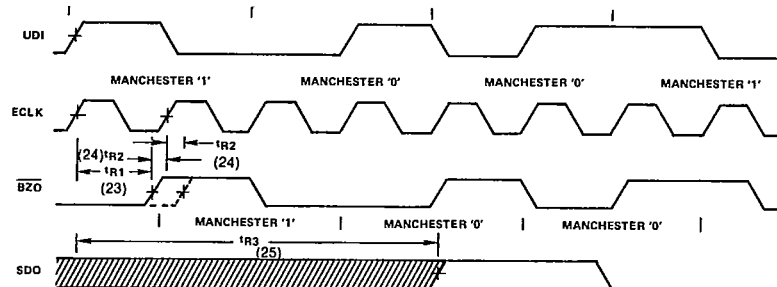
**Repeater Timing**

FIGURE 11.



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## MANCHESTER CODE

Nonreturn to Zero (NRZ) code represents the binary values logic-0 and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

The Manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a low to high transition in the middle of the data cell, and a logic-1 as a high to low mid bit transition. Manchester II is also known as Biphasic-L code.

The bandwidth of NRZ is from DC to the clock frequency  $f_c/2$ , while that of Manchester is from  $f_c/2$  to  $f_c$ . Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octave, while the ratio for NRZ is the range of 5-10 octaves. It is much easier to design a narrow band than a wideband amp.

Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that

there is no transition, an error indication is given, and synchronization must be re-established. This places relatively stringent requirements on the incoming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. There is no phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily have transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over successive data cells. A final synchronization advantage concerns the HD-6409's sync pulse used to initiate synchronization. This three bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

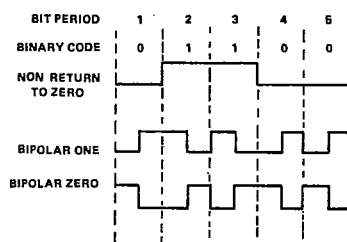
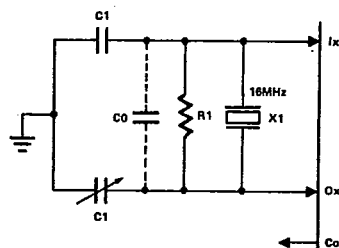


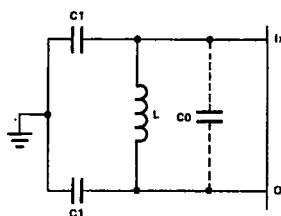
FIGURE 12.

## Crystal Oscillator Mode



C1 = 32pF  
C0 = Crystal + Stray  
X1 = AT CUT PARALLEL  
RESONANCE FUND-  
AMENTAL MODE  
R1 (TYP) = 30Ω  
R1 = 15 MΩ

## LC Oscillator Mode



C1 = 20pF  
C0 = 5pF  
 $C_0 \approx \frac{C1 - 2C0}{2}$   
 $f_0 \approx \frac{1}{2\pi\sqrt{LC_0}}$

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