mim ELECTRONICS LIMITED

C3008 SERIES

Real Time Clock Module

KEY FEATURES

- Industry standard dual in line JEDEC 24 pin Ram or Rom compatibility
- Time keeping during power down
- Complete clock/calendar function
- Quartz controlled accuracy
- Hi-rel lithium technology backup giving up to ten years life
- Write protected
- Easy to use like Ram with fast access time
- Alarm, stopwatch and timer
- Compatible with earlier types C1076 and C2008

OTHER FEATURES:

- Low supply current (≤8μA)
- 4 Bit byte serial BCD data format
- Processor bus compatible
- Cmos technology
- Optional use of 7 × 8 bit non volatile ram bytes, enabling power down storage of current time
- 125ns access time (H version)
- Optional 4.5v write disable (D version)
- Wide operating temperature range
- Synchronisation (option)

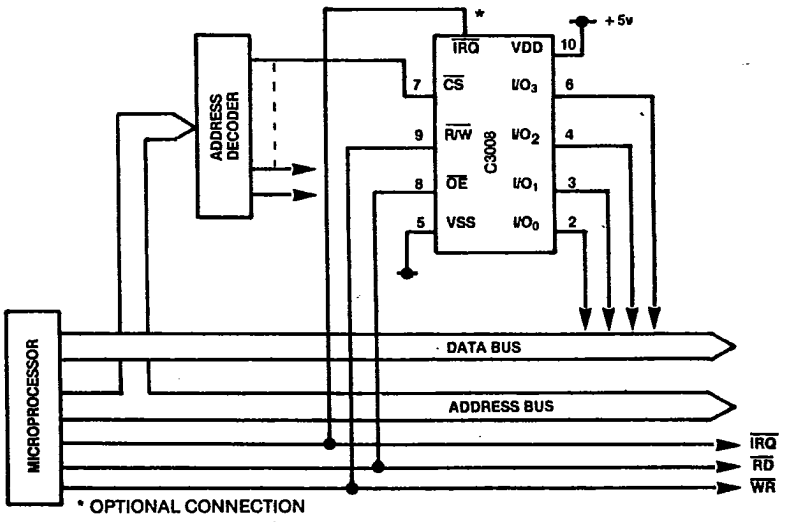
APPLICATION ENVIRONMENTS:

- Processor controlled instrumentation
- Word Processors
- Data Loggers
- Business Machines
- Home Computors
- Time Clock
- Heating and Air conditioning systems
- Point of sale terminals
- Traffic Control
- Security systems
- Energy Conservation systems
- Event recorders

GENERAL:

The 3008 Clock Module is a unique and versatile functional module for OEM systems designs requiring Real Time Clock functions. It is also particularly suited to 'Retro Fit' situations where a spare Ram or Eprom socket is already on board.
Time with a resolution in seconds is available. The module also has a complete calendar function with day of the week, day of the month, month of year and year, directly available. An automatic leap year correction is implemented and week number (of year) is also directly available.
The internal lithium cell ensures maintenance of accurate time data. When the voltage between Vdd and Vss falls below 2.5v ± 0.5v (4.5v, + 0.25v, – 0.1v D version) access to the device is disabled.
An Alarm function is available via a flying lead connection to the module interrupt pin. Connected to the System interrupt the module will provide a programmed alarm on date and time down to seconds. A Timer function can be obtained, providing a programmed delay in seconds up to 24 hours via the interrupt pin. the Timer registers can also be used as a 24 hour, seconds resolution stopwatch.

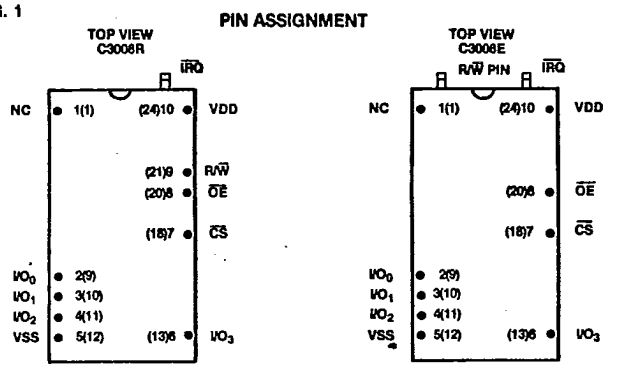
TYPICAL APPLICATION



PACKAGE DATA:

C3008R compatible with industry standard Ram pinout configurations including 6116, 4118, 2128, 5516.

FIG. 1 PIN ASSIGNMENT



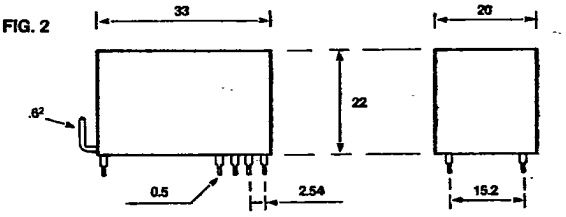
NOTE: Numbers shown in parenthesis correspond to Standard Memory Pin-out.

C3008E compatible with industry standard Eprom pinout configurations including 2732, 2708, 2516 Connect system write line to module R/W via flying lead.

TABLE 1

PIN	NAME	DESCRIPTION
1	NC	No Connection
2	I/O_0	Data Input/Output Lines
3	I/O_1	Data Input/Output Lines
4	I/O_2	Data Input/Output Lines
5	VSS	Ground Terminal (GND)
6	I/O_3	Data Input/Output Lines
7	$\overline{CS}$	Chip Select Input
8	$\overline{OE}$	Output Enable. If High, Outputs go to Hi – Z
9	R/$\overline{W}$	Read if High. Write if Low, Input
10	VDD	Positive Supply Terminal
	$\overline{IRQ}$	Interupt Active Low

FIG. 2



ABSOLUTE MAXIMUM RATINGS:

Voltage Vdd to Vss	8.0v
Voltage any pin to Vss	−0.3v
Storage temp range	−20 to +60°C
Operating temp range	0° to +60°C
Operating temp range (H Version)	−20° to +60°C

HANDLING PRECAUTIONS:

Normal handling precedures for ESD sensitive devices should be taken. Unused devices should be stored in conductive foam.

MODE OF OPERATION:

RAM

The 16 × 8 Ram is used to store all watch, alarm, timer and status data. The allocation of Ram addresss is shown in table 1. All time data are stored in the form of two 4-bit BCD words. If the alarm and timer functions are not used, the Ram section allocated to the addresses 8 to E may be employed as an additional non-volative system storage. In this case the data may assume any hexadecimal value. It should be noted however, that if the unused function is inadvertly activated by changing the status word, the stored data may be modified. See Table 2.

STATUS REGISTER

The status word is stored at Ram address $F. The individual bits of this word control the clock and stopwatch functions. Bits 2 and 3 flag the stopwatch and alarm interrupts. See Table 3.

INTERNAL UPDATE CYCLE

Every second, an internal time update occurs and lasts for a maximum of 6ms. During this time, the Ram is allocated to the ALU. If an external data transfer is already initiated, the internal update cycle is postponed for a maximum of one second. Then, the external transfer will be aborted. During the update cycle the data on the I/O lines is $F.

TABLE 3

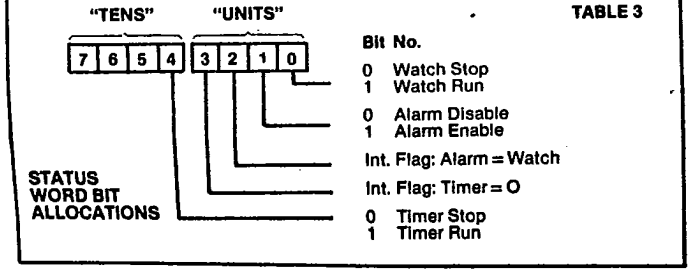


TABLE 2 I/O Address Locations

Address	Data	Group	Max. Value*	Operations
0	Seconds	WATCH	59	Time data locations
1	Minutes		59	incremented
2	Hours		23	under control of
3	Date		28, 29, 30, 31	status Bit 0
4	Month		12	
5	Year		99	
6	Week day		07	
7	Week no.		53	
8	Seconds	ALARM	59	Alarm data locations
9	Minutes		59	preset by user
A	Hours		23	to provide $\overline{IRQ}$ output
B	Date		28, 29, 30, 31	at specified time
C	Seconds	TIMER	59	Timer data locations
D	Minutes		59	incremented under
E	Hours		23	control of status bit 4
F	Status	STATUS		Control

* Only applicable to WATCH, ALARM and TIMER data.

ELECTRICAL SPECIFICATION
Standard Version

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Battery Life Note 1	VDD = Ov	Tb		10		years
I/O LINES Input High Voltage		VIH	2.4	0.5VDD	VDD	V
Input Low Voltage		VIL	VSS		0.8	V
Input Leakage Current	Vss _ Vin _ VDD	IL			1	uA
Input Current For OE	Vin = Vss				10	uA
Out put High Voltage	IOH = 2.0mA	VOH	2.4			V
Out put Low Voltage	IOL = 3.2mA	VOL			0.4	V
3 State Leakage Current	OE or CS at VDD	IHI-Z			1	uA
Clock Accuracy		TA		5	10	Min/Yr
Supply Current	INPUTS AT VDD or VSS	IDD			8	uA
Chip Select Duration		tcsd	0.3			uA
RAM Access Time		tacc		0.2	0.3	uS
Data Settle Time		tdw	0.2	0.25		uS
Data Valid to high impedance		tdf		0.2		uS
Minimum Time Between 2 Transfers		twait		1.0		uS
Data Hold Time		tdh	0.03	0.05		uS
Supply Voltage to Disable Write		VDDL	2.0	2.5	3.0	V
Weight				27		G

ADDITIONAL DATA D VERSION

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage to Disable Write		VDDI	4.4	4.5	4.75	V
Supply Current					5	MA

ADDITIONAL DATA H VERSION

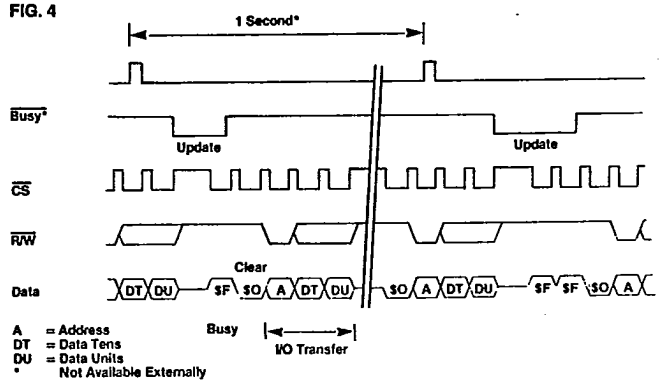
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Chip Select Duration		tcsd	0.28			uS
RAM Access Time		tacc		0.125	0.2	uS
Data Hold Time		tdh	0			uS

Typical values are at 20°C and nominal voltages, unless specified measurements are taken at typical values.

1. When power is applied to the clock the internal battery is disconnected consequently the limit on battery life is set by storage life, which is Ten years.

I/O TRANSFER WAVEFORMS

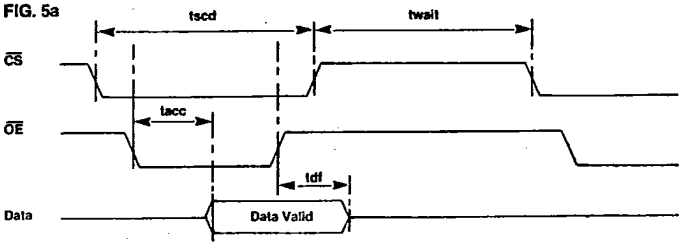
FIG. 4



A = Address
DT = Data Tens
DU = Data Units
* Not Available Externally

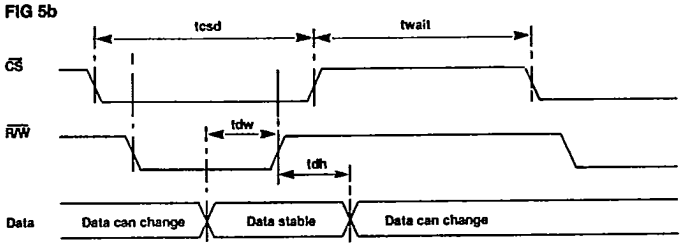
READ CHARACTERISTICS

FIG. 5a



WRITE CHARACTERISTICS

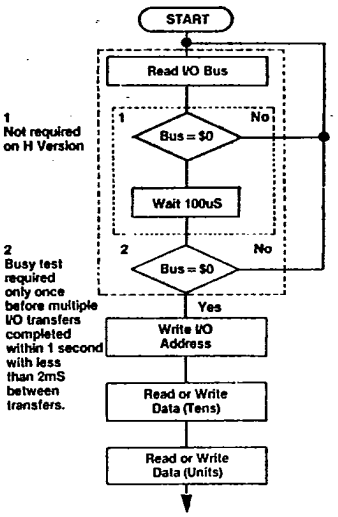
FIG 5b



If OE is not used, it should be connected to CS. "tac" and "tdf" must then be related to CS.

BUSYTEST AND I/O TRANSFER

FIG. 6



WRITE PROTECTION

On power down in typical microprocessor based systems, the buses will become undefined when the supply voltage reaches a critical value. This point is processor/system dependant and there is a possibility of "garbage" being written into RAM type components when this happens. To this end it has been usual in battery backed system to generate a power failure signal to disable the read write line and hence guard against data corruption. Write protection is built into the C3008 Clock Module and is available at two nominal voltage levels. The standard version at 2.5v, and the D version at 4.5v.

DATA I/O TRANSFERS:

TRANSFER OF TIME AND STATUS DATA

Before initiating a data transfer to the module, it is necessary to check if the clock is carrying out an internal up-date cycle. An internal up-date cycle occurs once per second and lasts for a maximum of 6ms. The internal busy signal is shown on fig 3. During the update cycle a read of the I/O bus will return the value $F. This if tested for before an I/O transfer will avoid a conflict with an update cycle.

The I/O bus is a multiplexed carrying both address and time data to the internal buses. Being only 4 bits wide a double read or write is necessary to transfer the 8 bit wide contents of the clock registers, refer to fig 2. The data is returned in BCD format, tens followed by units. If an internal update request occurs during an I/O transfer the request will be held until the end of the I/O transfer which should be completed within one second. If an I/O transfer is not completed an internal update cycle is forced after a maximum of 2 seconds. See Figs 5a, 5b and 6.

IMPORTANT:

An I/O transfer consists of writing an I/O address followed by 2 read or write cycles. The data is in 4 bit byte serial BCD format, tens followed on the next read or write by units. See Ordering Data for provision of busy signal.

MULTIPLE I/O TRANSFERS:

During consecutive transfers no internal update will occur if the time between each transfer is less than 2ms. The total time taken should however be less than 1 second. If an update is required between continuous transfers as when looking for an event, the delay between transfers should be greater than 6ms.

DATA TRANSFER H VERSION:

When power is first applied to the 308H version, the state of the multiplexer is undefined. The multiplexer may be reset by activating $\overline{CS}$ twice for longer than 280ns. The multiplexer is reset automatically during the update cycle every second, but a reset is advised for situations where there may be aborted date transfers or noise on the $\overline{CS}$ line.

STOPWATCH MODE:

The Timers Registers $C to $E can be used as a 24 hour seconds resolution stop watch, under the control of bit 4 of the status word.

INTERRUPTS . . . THE ALARM AND TIMER FUNCTIONS:

Registers 8 to $B act as a time and date alarm via the $\overline{INT}$ pin under the control of bit 1 of the status word.
The timer registers $C to $E will set $\overline{IRQ}$ active when the timer data increments from 23.59.59 to 00.00.00., $\overline{IRQ}$ is flagged on bit 3 of the status word.
$\overline{IRQ}$ will remain active until the relevant flag of the status word is cleared.
The $\overline{IRQ}$ is weakly pulled up and can be wire-ored to the system interrupt without problems.
See Fig. 7 for a typical interrupt handling procedure.

Typical Program Sequence in Response to $\overline{IRQ}$
$\overline{CS}$ = $A000

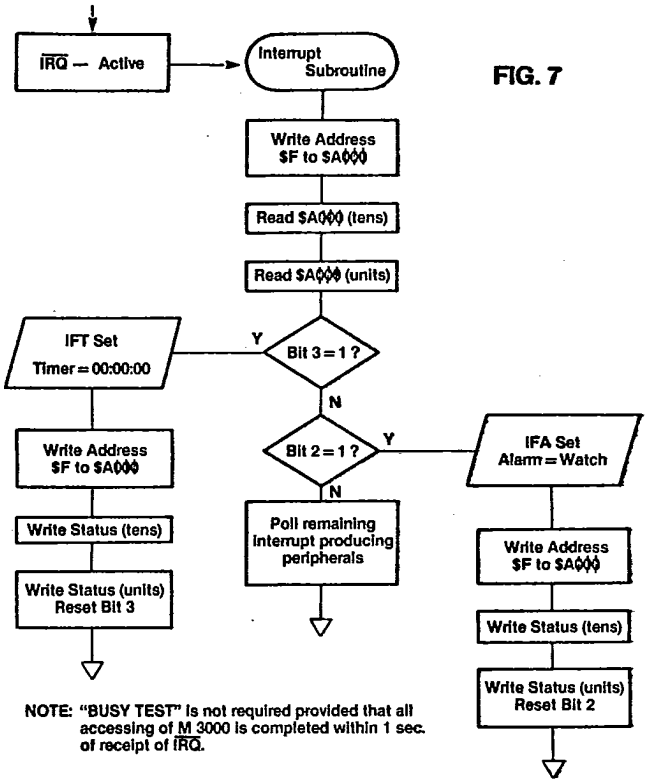


FIG. 7

NOTE: "BUSY TEST" is not required provided that all accessing of M 3000 is completed within 1 sec. of receipt of $\overline{IRQ}$.

WEEK NUMBER SPECIAL NOTE:

Week number if incremented on a seven day cycle, the maximum week number is 53. This allows implementation of the standard I.S.O. week number system.
In the I.S.O. week numbering system, week 1 is the first week containing four or more days of the new year. Monday is taken as the first day of the week. This results in some years having 53 weeks.

SYNCHRONISATION (OPTION F)

If the SYNC input is set low for longer *than* 200µs, the clock will synchronise to the falling edge of SYNC with a precision of ±2mS. The seconds register is cleared and if the second register was ≥ 30 the minutes register is incremented.

ORDERING DATA:

C3008 _ _ _ _

PINOUT	
R	RAM
E	EPROM

H	FAST ACCESS TIME
D	4.5v WRITE PROTECT
E	BUSY SIGNAL PROVIDED
F	SYNCHRONISATION

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