G12™-p 3.3 V, 4 mA, 5-Volt Tolerant, Fail-Safe, General Purpose I/O Buffers

Datasheet

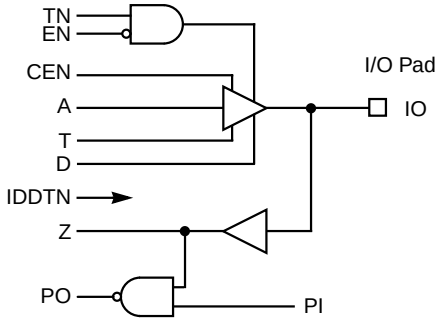
LSI Logic Corporation provides the following driver/receiver input/output (I/O) cells for use as general purpose I/O buffers:

- bd4f5fsls33
- bd4puf5fsls33
- bd4puodf5fsls33
- bd4puodf5fscls33

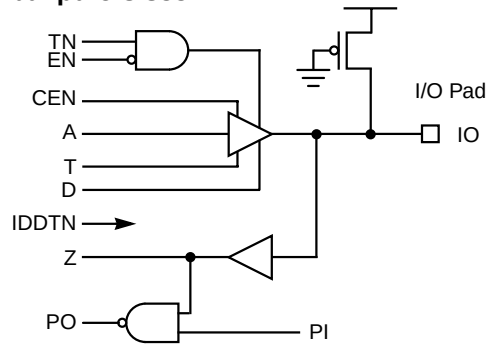
The I/O buffers provide off-chip, bidirectional I/O signaling for application-specific integrated circuit (ASIC) chips implemented in the LSI Logic G12™-p 0.13 µm process technology. Functionally similar, the I/O buffers (Figure 1) provide an ASIC application with different driver options.

Figure 1 Buffer Block Diagrams

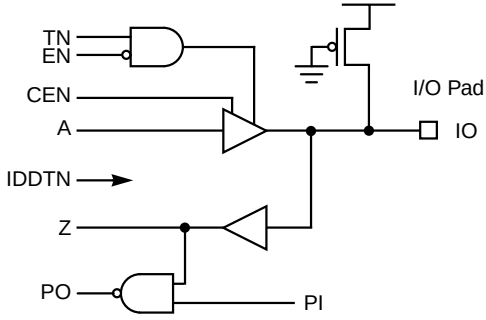
a) bd4f5fsls33



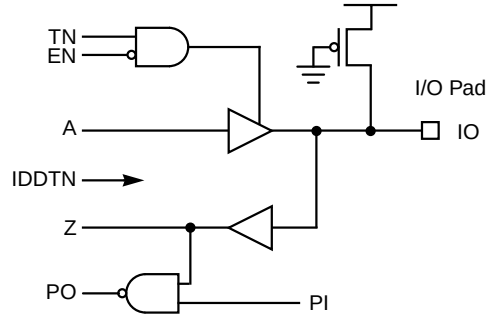
b) bd4puf5fsls33



c) bd4puodf5fsls33



d) bd4puodf5fscls33



Features and Benefits

- Up to 20 MHz, 3.3 V I/O operation
- 5-Volt tolerant
- Fail-safe at high voltages
- Feedthrough protection
- 20 µA maximum leakage current
- Minimum 4 mA current drive into a 40 pF load at 20 MHz
- 1.8 V internal signaling for reduced power consumption
- Uses one standard I/O slot

Signal Descriptions

Table 1 describes signal connections for all four buffers.

Table 1 I/O Buffer Connections

Signal	Direction	Description
A	IN	Data input to I/O buffer driver from ASIC circuitry
CEN[1]	IN	Enables I/O buffer operation after power-on
D[2]	IN	Configures driver operating mode
EN	IN	0 = Normal mode 1 = Disable I/O buffer driver
IDDTN	IN	0 = Power down entire cell[3] 1 = Normal mode
PI	IN	NAND-tree parametric test input
T[2]	IN	Configures driver operating mode
TN	IN	0 = Disable I/O buffer driver 1 = Normal mode
IO	IN/OUT	Input/output pad
PO	OUT	NAND-tree parametric test output
Z	OUT	I/O buffer receiver output to ASIC circuitry

1. Not available in bd4puodf5fscls33
2. Available only in bd4f5fsls33 and bd4puf5fsls33. Refer to Table 4 for settings.
3. Used for production IDDQ leakage test

General Description

The buffers include a receiver, driver, and NAND-tree circuitry to conform with standard LSI Logic test methodology. The buffers translate signals between the 1.8 V operating levels of the ASIC core circuitry and the 3.3 V operating levels at the I/O pad. They tolerate high DC and transient voltages at the I/O pad, are fail safe, and provide feedthrough protection.

Voltage Tolerance

The I/O buffers are 5-volt tolerant. Although the off-chip I/O signaling normally operates at 3.3 volts, external circuitry may cause higher voltages, typically upwards of 5 volts, to appear at the chip I/O pad. Circuit and process techniques ensure that such DC or transient voltages do not damage the I/O buffer circuitry.

Failure and Feedthrough Protection

In the absence of a V_{DD} supply, the I/O buffers are fail-safe and protected against voltage feedthrough. With high voltage applied to the chip I/O pad, the I/O buffers can survive without degradation for up to ten years. Furthermore, with a low, maximum 20 µA leakage current, the high voltage can not power up the ASIC through voltage feedthrough.

Functional Description of Receivers

The buffers use the same receiver circuitry. The following truth table (Table 2) describes receiver behavior.

Table 2 Receiver Truth Table

Inputs			Outputs	
IDDTN	**IO**	**PI**	**Z**	**PO**
0 [1]	High Impedance	1	1	0
1	0	0	0	1
1	1	0	1	1
1	1	1	1	0

1. Factory IDDQ test setting

Functional Description of Drivers

The buffers use similar driver circuitry that produces a minimum of 4 mA of output drive. The buffers provide options for selecting the driver output configuration and power-up mode (Table 3). All the buffers except bd4f5fsls33 have internal pull-up resistor devices. Preset power-up modes avoid unpredictable output behavior.

Table 3 I/O Buffer Driver Characteristics

I/O Buffer Cell	Driver Mode	Pull-Up	Power-Up Mode	Application
bd4f5fsls33	Dynamically programmable open-drain, open-source, or totem-pole output	None	3-State	General
bd4puf5fsls33	Dynamically programmable open-drain, open-source, or totem-pole output	Yes, internal	3-State	General
bd4puodf5fsls33	Open-drain output	Yes, internal	Current sinking logic level 0	Power-on reset
bd4puodf5fscls33	Open-drain output	Yes, internal	3-State	General

Driver Output Configuration

With the bd4f5fsls33 (Figure 1a) or bd4puf5fsls33 (Figure 1b) buffer, the T and D inputs set a driver output to open-drain, open-source, or totem-pole mode (Table 4). An application can hardwire the T and D inputs, or, to dynamically configure a driver output, it can supply the T and D inputs from a register.

Table 4 Driver Output Mode Selection

T	D	Output
0	0	Open drain
0	1	Totem pole
1	0	Totem pole
1	1	Open source

The bd4puodf5fsls33 (Figure 1c) and the bd4puodf5fscls33 (Figure 1d) buffers fix the output in the open-drain mode.

Pull-Up Resistor

Except for bd4f5fsls33, the buffers include a pull-up resistor, which can provide from 100 µA to 500 µA of current across the specified process, voltage, and temperature ranges.

Note: Evaluate the buffer models before simulating a design. Models provided for some third-party design environments may not correctly represent or even include the pull-up resistor.

Power-Up Modes

Each buffer has a defined power-up mode (Table 3) to avoid unpredictable output behavior. The bd4f5fsls33, bd4puf5fsls33, and bd4puodf5fsls33 buffers preset the driver output to 3-state or current-sinking mode upon power up. The bd4puodf5fscls33 buffer has no preset power-up mode.

Preset to 3-State (bd4f5fsls33 and bd4puf5fsls33)

At power up, circuitry in the bd4f5fsls33 and bd4puf5fsls33 buffers forces the IO signal at the I/O pad to the high-impedance state. To begin normal operation, the buffers require the ASIC application to assert CEN to HIGH.

Preset to Open-Drain (bd4puodf5fsls33)

At power up, circuitry in the bd4puodf5fsls33 buffer forces the driver output to open-drain mode. As the driver sinks current, it drives the IO signal at the I/O pad to LOW. Designed primarily for power-on-reset applications, the buffer holds circuits connected to the I/O pad in the LOW reset state until the ASIC application asserts CEN to HIGH, thereby releasing the buffer to operate normally.

To drive the CEN signal HIGH directly from a source external to the ASIC, connect CEN to a DDRV type I/O pad for ESD protection and apply an activation signal. Although this activation signal may reach 3.3 V, a signal limited to1.8 V better matches the normal internal signaling level, and is therefore preferable.

No Preset (bd4puodf5fscls33)

The bd4puodf5fscls33 buffer has no CEN signal to provide a separate power-up mode. However, power-up characteristics of the buffer circuitry prevent hard driving the IO signal at the I/O pad to HIGH, thereby avoiding unpredictable behavior. A relatively high-impedance pull-up device eventually drives IO to HIGH unless

- the buffer itself drives it LOW with A = EN = 0 and TN = 1, or
- another device external to the buffer drives it LOW.

Truth Tables

Table 5 describes the driver behavior for the bd4f5fsls33 and bd4puf5fsls33 buffers.

Table 5 Truth Table for bd4f5fsls33 and bd4puf5fsls33 Drivers

Inputs							Output without Pull-up Resistor[1]	Output with Pull-up Resistor[2]	Description
IDDTN	CEN	A	TN	EN	T	D			
X[3]	0	X	X	X	X	X	High Impedance	High Impedance	3-State power-up mode
0	1	X	X	X	X	X	High Impedance	High Impedance	Factory IDDQ test setting
1	1	X	X	1	X	X	High Impedance	High Impedance[4]	Disabled with EN
1	1	X	0	X	X	X	High Impedance	High Impedance[4]	Disabled with TN
1	1	0	1	0	0	0	0	0	Open-drain output
1	1	1	1	0	0	0	High Impedance	High Impedance[4]	Open-drain output
1	1	0	1	0	0	1	0	0	Totem-pole output
1	1	1	1	0	0	1	1	1	Totem-pole output
1	1	0	1	0	1	0	0	0	Totem-pole output
1	1	1	1	0	1	0	1	1	Totem-pole output
1	1	0	1	0	1	1	High Impedance	High Impedance[4]	Open-source output
1	1	1	1	0	1	1	1	1	Open-source output

1. Using bd4f5fsls33 buffer
2. Using bd4puf5fsls33 buffer. Note: SPICE type simulation may produce different behavior.
3. Don't care state, X = 0 or 1
4. In silicon, the pull-up resistor actually pulls the output HIGH. However, third-party models do not correctly represent the pull-up resistor. Therefore, the truth table shows the output in the high-impedance state.

Table 6 describes the bd4puodf5fsls33 driver behavior.

Table 6 Truth Table for bd4puodf5fsls33 Driver

Inputs					Output	
IDDTN	**CEN**	**A**	**TN**	**EN**	**IO**	**Description**
X[1]	0	X	X	X	0	Open-drain power-up mode
0	1	X	X	X	High Impedance	Factory IDDQ test setting
1	1	X	X	1	High Impedance[2]	Disabled with EN
1	1	X	0	X	High Impedance[2]	Disabled with TN
1	1	0	1	0	0	Open-drain output
1	1	1	1	0	High Impedance[2]	Open-drain output

1. Don't care state, X = 0 or 1
2. In silicon, the pull-up resistor actually pulls the output HIGH. However, third-party models do not correctly represent the pull-up resistor. Therefore, the truth table shows the output in the high-impedance state.

Table 7 describes the bd4puodf5fscls33 driver behavior.

Table 7 Truth Table for bd4puodf5fscls33 Driver

Inputs				Output	
IDDTN	**A**	**TN**	**EN**	**IO**	**Mode**
0	X[1]	X	X	High Impedance	Factory IDDQ test setting
1	X	X	1	High Impedance[2]	Disabled with EN
1	X	0	X	High Impedance[2]	Disabled with TN
1	0	1	0	0	Open-drain output
1	1	1	0	High Impedance[2]	Open-drain output

1. Don't care state, X = 0 or 1
2. In silicon, the pull-up resistor actually pulls the output HIGH. However, third-party models do not correctly represent the pull-up resistor. Therefore, the truth table shows the output in the high-impedance state.

Driver Slew Rate

The following slew rate measurement applies to the bd4f5fsls33 and bd4puf5fsls33 buffers in totem-pole mode. In the rise/fall test, the driver drives a signal across a 40 pF load capacitor (Figure 2). Table 8 shows the observed slew rate across the load capacitor measured from 0.6 V to 2.2 V.

Figure 2 Rise/Fall Test Circuit

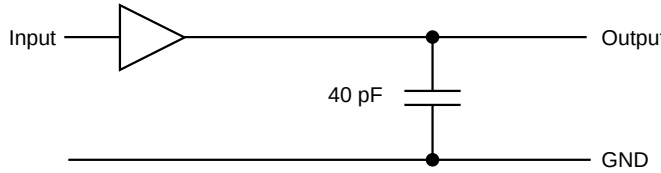


Table 8 Driver Rise/Fall Slew Rate

Min.	Typ.	Max.	Unit
–	600	–	mV/ns

Testing

The buffers include test circuitry and signals compatible with standard LSI Logic test methodology. The PI and PO NAND-tree signals provide access for parametric testing. The global IDDTN signal powers down all circuitry for IDDQ leakage testing.

IMPORTANT:

The IDDQ leakage test requires the I/O buffers in the high-impedance state. Setting IDDTN to LOW usually accomplishes this condition. However, with the I/O buffers that use CEN to preset the power-up mode, IDDQ may fail due to high leakage current unless CEN is also driven HIGH.

Specifications

The buffers adhere to the general specifications in Table 9. Table 10 describes the receiver DC characteristics. Table 11 describes the driver DC characteristics.

Table 9 General Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.97	3.30	3.63	V
T_j	Junction temperature		0	–	125	˚C
ESD	Electrostatic discharge, human body model (HBM)	MIL-STD-883C, Method 3015.7 100 pF @1.5 KΩ	2000	–	–	V
	Electrostatic discharge, charged device model (CDM)	ESD DS5.3.1-1996	500	–	–	V

Table 10 Receiver DC Characteristics[1]

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH voltage		1.5	–	2.0	V
V_{IL}	Input LOW voltage		1.0	–	1.5	V
V_H	Hysteresis		320	–	–	mV
I_{IL}	Input leakage current	$0 \le V_{PAD} \le 3.63$ V, V_{DD} = 3.3 V ±10%	–	–	10	µA
I_{LU}	Latchup current	-2 V < V_{PAD} < +8 V	–	–	±100	mA

1. Values apply over all voltage, temperature, and process conditions

Table 11 Driver DC Characteristics[1]

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	V_{OL} and high impedance output only	2.97	3.30	3.63	V
V_{OL}	Output, LOW	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	Output, HIGH	I_{OH} = –4 mA V_{DD} = 3.135 V	2.4	–	–	V
I_{OL}	Sink current	V_{OL} = 0.4 V maximum, totem-pole and open-drain mode	4	–	–	mA
I_{OH}	Source current	V_{OH} = 2.4 V minimum, totem-pole and open-source mode	–	–	–4	mA
I_{OZ}	3-Stated leakage current	$0 \le V_{PAD} \le 5.5$ V, resistors disabled, V_{DD} = 3.3 V ±10%	–	–	20	µA
I_{LU}	Latchup current	$-2\ V < V_{PAD} < +8\ V$	–	–	±100	mA

1. Values apply over all voltage, temperature, and process conditions.

System Design Guidelines

To ensure good system-level operation, LSI Logic provides the following guidelines for placing these I/O cells in the ASIC and for supplying power.

Placement

All these I/O cells have the same dimensions (Table 12) and require placement on the I/O ring using one I/O slot.

Table 12 Cell Dimensions on the I/O Ring

Width Along the I/O Ring	Length into the Chip
45.36 µm	397.53 µm

For correct placement of the I/O cells, adhere to the following guidelines:

- These I/O cells may adjoin each other. They may also adjoin a `bd4f5fs60ls33` cell.
- Separate these I/O cells from any other type of I/O function by at least one I/O slot to avoid N-channel to P-channel design rule violations. If possible, use a VDD or VSS pad for the separation.
- Because their lengths exceed the length of other standard I/O functions, these I/O cells may not use a corner I/O slot.

Power

For best system-level performance, adhere to the following power guidelines:

- Use one power/ground pad pair for every four I/O cells.
- Place an I/O cell no more than four slots away from a power pad and no more than four slots away from a ground pad.

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