High-Performance
256 KByte Asynchronous
Cache Module

AS7M32W256

PRELIMINARY

256 KByte Asynchronous Cache Module

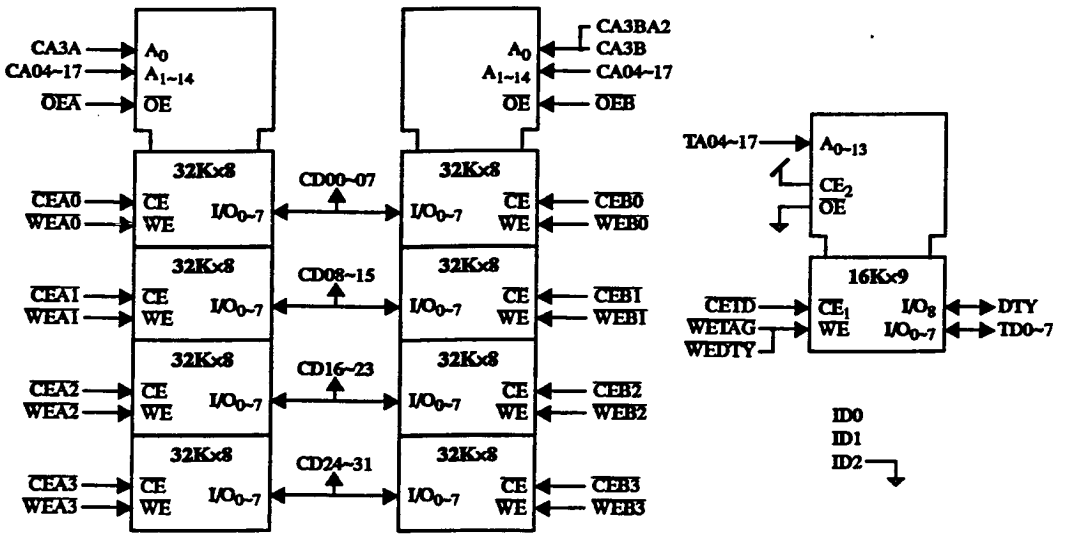
FEATURES

- 256 KByte secondary cache module
  - Bank A: 32,768 words × 32 bits
  - Bank B: 32,768 words × 32 bits
  - Tag/Dirty:16,384 words × 9 bits
- High speed
  - 15/20 ns cache address access time
  - 12/15 ns tag address access time
  - 50/33 MHz cycle frequency
- Low power
  - Active: 5.75W max (15 ns cycle)
  - Standby: 125 mW max
- 64 pin dual-readout SIMM
  - Same pinout for 128/256KB
  - No motherboard jumpers required
  - Small footprint: less than 1.2 in^2
- Supports major PC cache controllers
  - Per-byte $\overline{CE}$ and $\overline{WE}$ controls
  - Per-bank interleaved $\overline{OE}$
  - Common tag and dirty $\overline{WE}$
- TTL-compatible, three-state I/O
- High-quality 4-layer PCB

PIN ARRANGEMENT

ID0	1	65	ID1
ID2	2	66	GND
CD00	3	67	CD01
CD02	4	68	CD03
CD04	5	69	Vcc
CD06	6	70	CD05
CD08	7	71	CD07
GND	8	72	CD09
CD10	9	73	CD11
CD12	10	74	CD13
CD14	11	75	CD15
CD16	12	76	CD17
CD18	13	77	CD19
CD20	14	78	CD21
GND	15	79	GND
CD22	16	80	CD23
CD24	17	81	CD25
Vcc	18	82	Vcc
CD26	19	83	CD27
CD28	20	84	CD29
CD30	21	85	CD31
NC	22	86	NC
NC	23	87	NC
GND	24	88	GND
$\overline{CEA0}$	25	89	$\overline{CEB0}$
$\overline{CEA1}$	26	90	$\overline{CEB1}$
$\overline{CEA2}$	27	91	Vcc
$\overline{CEA3}$	28	92	$\overline{CEB2}$
GND	29	93	$\overline{CEB3}$
$\overline{OEA}$	30	94	$\overline{OEB}$
$\overline{WEA0}$	31	95	$\overline{WEB0}$
$\overline{WEA1}$	32	96	$\overline{WEB1}$
$\overline{WEA2}$	33	97	$\overline{WEB2}$
$\overline{WEA3}$	34	98	$\overline{WEB3}$
$\overline{WETAG}$	35	99	$\overline{WEDTY}$
$\overline{CETD}$	36	100	Vcc
NC	37	101	NC
NC	38	102	NC
CA3A	39	103	CA3BA2
CA02	40	104	CA3B
GND	41	105	GND
CA04	42	106	CA05
CA06	43	107	CA07
CA08	44	108	CA09
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	CA17
NC	49	113	NC
GND	50	114	GND
TA04	51	115	TA05
TA06	52	116	TA07
TA08	53	117	TA09
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	TA17
NC	58	122	NC
GND	59	123	GND
TD0	60	124	TD1
TD2	61	125	TD3
TD4	62	126	TD5
TD6	63	127	TD7
DTY	64	128	Vcc

LOGIC BLOCK DIAGRAM



SELECTION GUIDE

	7M32W256-15	7M32W256-20
Maximum cache address access time	15 ns	20 ns
Maximum tag address access time	12 ns	15 ns
Maximum operating current	1040 mA	940 mA
Maximum standby current	22.5 mA	22.5 mA

FUNCTIONAL DESCRIPTION

The AS7M32W256 is a high performance secondary cache module for 486 and other advanced computer systems. The Alliance 32D/32W family provides a plug-and-play upgradeable cache solution for motherboards based on all popular personal computer chipsets.

The 32W256 includes 256 KBytes of secondary cache, organized as two interleaved banks of 32K words by 32 bits. The module includes 16K words by 9 bits of tag/dirty storage and for cacheable main memory up to 64 MBytes.

The 32W256 is available in popular personal computer speed grades. The -15 version offers 15 ns address access time for cache data and 12 ns address access time for tag/dirty bits, to support 50 MHz system designs. The -20 version offers 20 ns address access time for cache data and 15 ns address access time for tag/dirty bits, to support 33 MHz system designs.

Alliance's industry-leading low power CMOS fast static RAM gives the 32W256 excellent power characteristics. The module dissipates less than 125 mW in standby mode, and less than 5.75W in operation at 50 MHz. Inputs and outputs are fully TTL-compatible.

The 32W256 plugs into a 64 dual readout SIMM connector which occupies less than 1.2 square inches of board space. Identification pins ID0~ID2 distinguish different members of the 32D/32W family and eliminate the need for motherboard cache configuration jumpers.

The module is fully static and requires no clocks for refresh or operation. It uses a single 5V power supply.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	V_t	-0.5	+7.0	V
Power Dissipation	P_D	—	9.0	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	°C
Temperature Under Bias	T_{bias}	-10	+85	°C
DC Output Current (per pin)	I_{out}	—	20	mA

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby (I_{SB}, I_{SB1})
L	H	H	High-Z	Output Disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

RECOMMENDED OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5*	—	0.8	V

* V_{IL} min = -3.0V for pulse width less than 10 ns.

DC OPERATING CHARACTERISTICS [1] (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Parameter	Symbol	Test Conditions	-15		-20		Unit
			Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}	—	15	—	15	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{out} = GND to V_{CC}	—	15	—	15	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}$ = V_{IL}, I_{out} = 0 mA, $f = f_{max}$	—	1040	—	940	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ = V_{IH}, $f = f_{max}$	—	100	—	100	mA
	I_{SB1}	$\overline{CE}$ > V_{CC}–0.2V, f = 0, V_{in} ≤ 0.2V *or* V_{in} ≥ V_{CC}–0.2V	—	22.5	—	22.5	mA
Output Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	—	0.4	—	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	—	2.4	—	V

CAPACITANCE [2] (f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V)

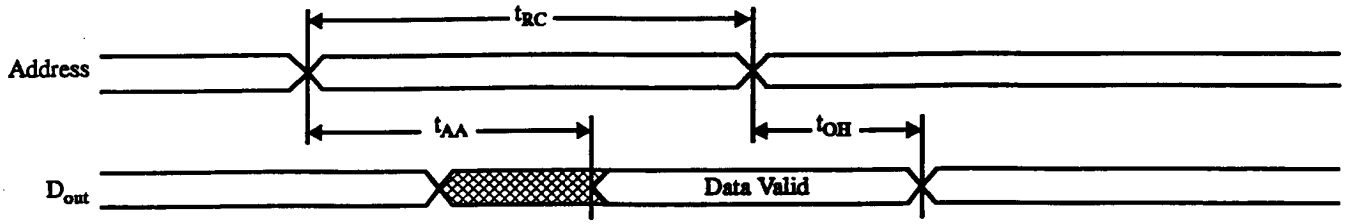
Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance: cache address	C_{IN4}	CA, $\overline{OE}$	V_{in} = 0V	70	pF
Input capacitance: tag address	C_{IN2}	TA, $\overline{CETD}$	V_{in} = 0V	10	pF
Input capacitance: control	C_{IN1}	$\overline{WE}$, $\overline{CE}$ (*except* $\overline{CETD}$)	V_{in} = 0V	10	pF
Data I/O capacitance	$C_{I/O}$	CD, TD, DTY	V_{in} = V_{out} = 0V	12	pF

READ CYCLE[3, 9]

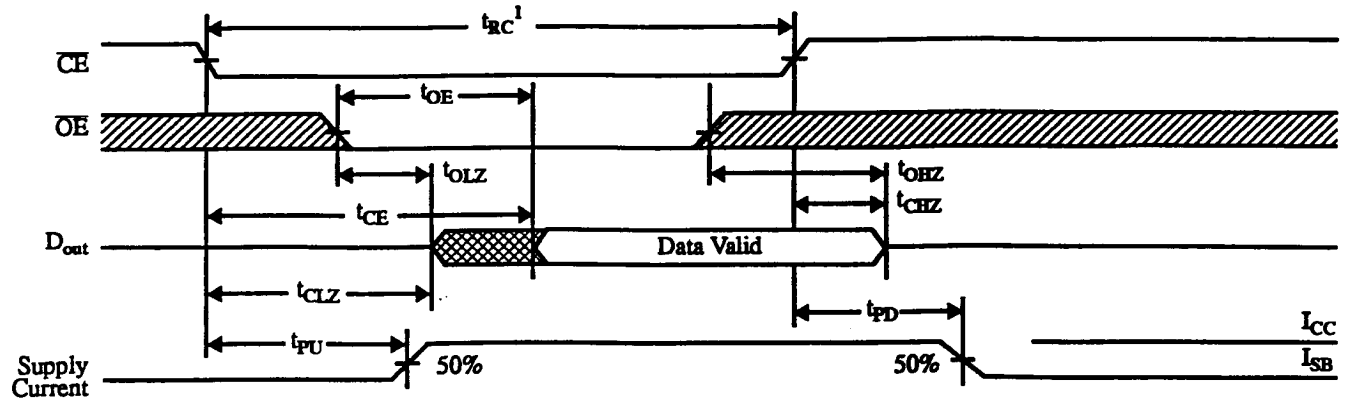
(V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Parameter	Sym	-15				-20				Units	Notes
		Cache		Tag		Cache		Tag			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	15	—	12	—	20	—	15	—	ns	
Address Access Time	t_{AA}	—	15	—	12	—	20	—	15	ns	3
Chip Enable ($\overline{CE}$) Access Time	t_{CE}	—	15	—	12	—	20	—	15	ns	3
Output Enable ($\overline{OE}$) Access Time	t_{OE}	—	4	—	—	—	5	—	—	ns	
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	3	—	ns	5
Chip Enable to Output in Low Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4, 5
Chip Disable to Output in High Z	t_{CHZ}	—	4	—	4	—	5	—	4	ns	4, 5
Output Enable to Output in Low Z	t_{OLZ}	0	—	—	—	0	—	—	—	ns	4, 5
Output Disable to Output in High Z	t_{OHZ}	—	4	—	—	—	5	—	—	ns	4, 5
Chip Enable to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns	4, 5
Chip Disable to Power Down Time	t_{PD}	—	15	—	12	—	20	—	15	ns	4, 5

TIMING WAVEFORM OF READ CYCLE 1[3, 6, 7, 9] (Address controlled)



TIMING WAVEFORM OF READ CYCLE 2[3, 6, 8, 9] ($\overline{CE}$ controlled)

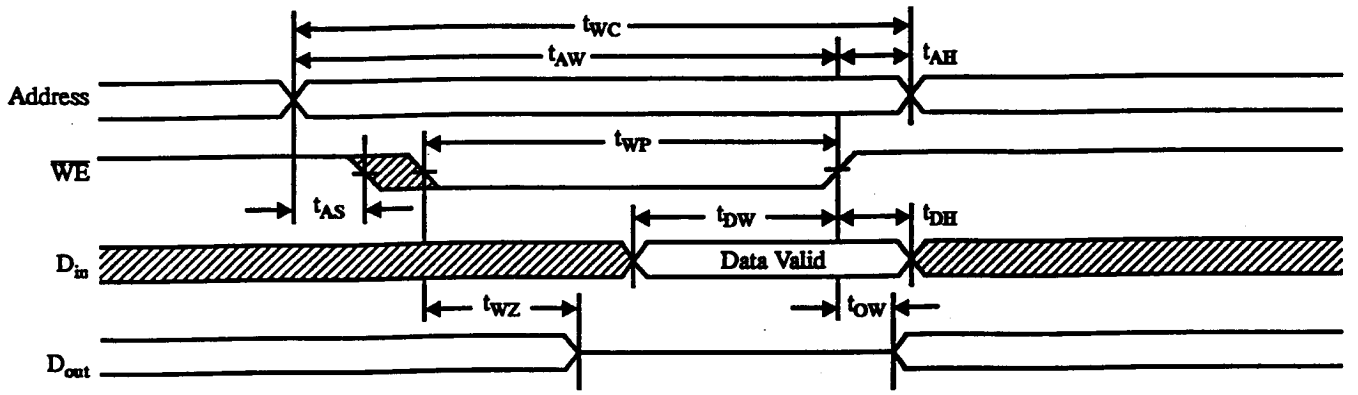


WRITE CYCLE [11]

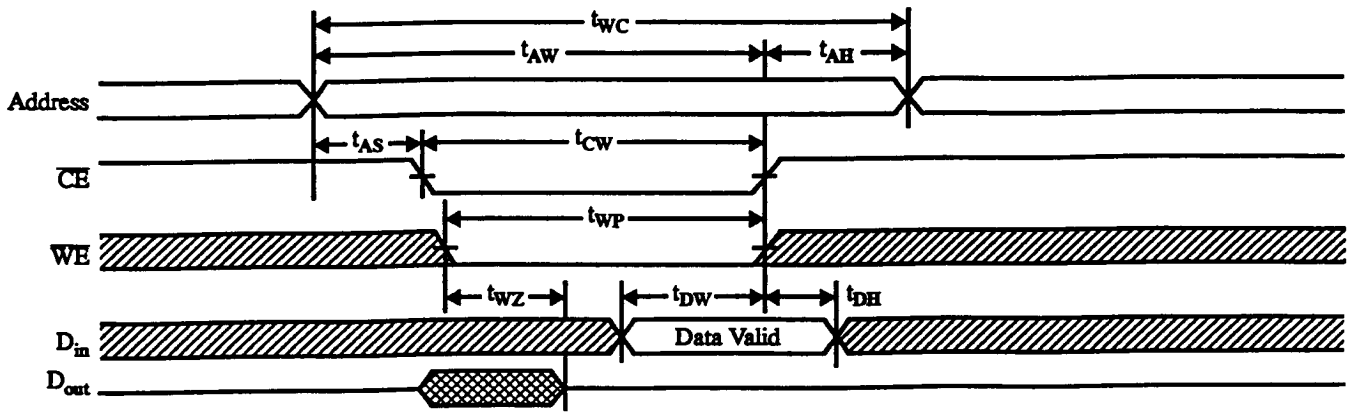
(V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Parameter	Sym	-15				-20				Units	Notes
		Cache		Tag		Cache		Tag			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	15	—	12	—	20	—	15	—	ns	
Chip Enable to Write End	t_{CW}	10	—	9	—	12	—	10	—	ns	
Address Set-up to Write End	t_{AW}	10	—	9	—	12	—	10	—	ns	
Address Set-up Time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	9	—	8	—	12	—	9	—	ns	
Address Hold From End of Write	t_{AH}	0	—	0	—	0	—	0	—	ns	
Data Valid to Write End	t_{DW}	9	—	8	—	12	—	9	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	0	—	ns	4, 5
Write Enable to Output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	ns	4, 5
Output Active from Write End	t_{OW}	3	—	3	—	3	—	3	—	ns	4, 5

TIMING WAVEFORM OF WRITE CYCLE 1 [10, 11] ($\overline{WE}$ controlled)



TIMING WAVEFORM OF WRITE CYCLE 2 [10, 11] ($\overline{CE}$ controlled)



AC TEST CONDITIONS

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

Thevenin equivalent:

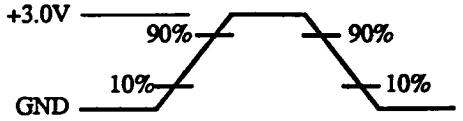


Figure A. Input Waveform

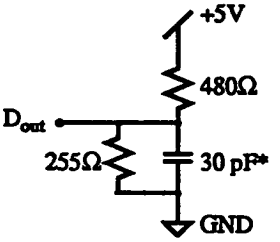


Figure B. Output Load

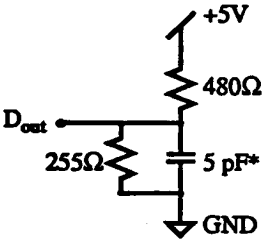


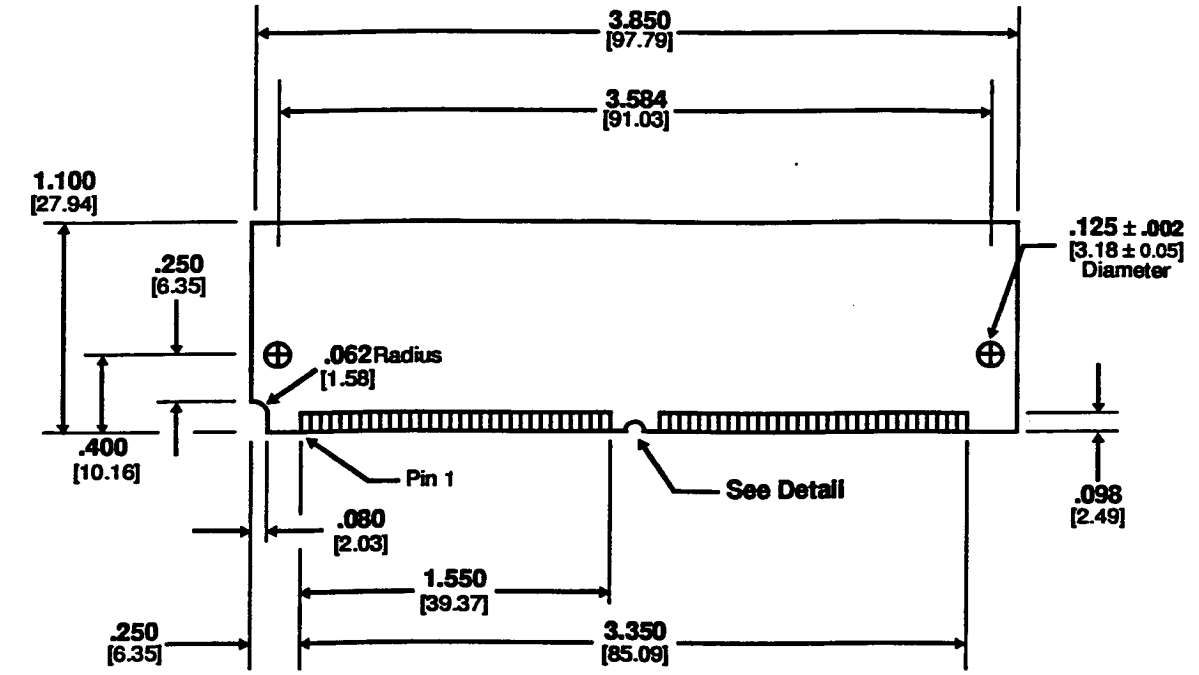
Figure C. Output Load for t_{CLZ}, t_{CHZ}

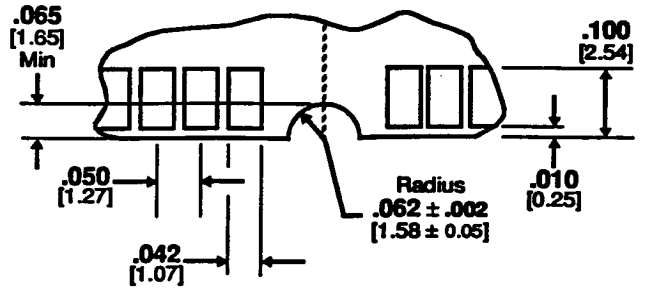
*including scope and jig capacitance

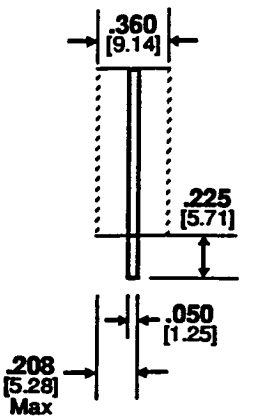
NOTES

1. During V_{cc} power-up, a pull-up resistor to V_{cc} on $\overline{CE}$ is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see AC Test Loads and Waveforms, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with CL = 5pf as in Figure C. Transition is measured 500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. $\overline{WE}$ is high for read cycle
7. $\overline{CE}$ and $\overline{OE}$ are low for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.

PHYSICAL DIMENSIONS







Dimensions in inches [millimeters].

ORDERING INFORMATION

Package	Cache Address Access Time	
	15 ns	20 ns
64 dual readout SIMM	AS7M32W256-15C	AS7M32W256-20C

REPRESENTATIVES AND DISTRIBUTORS

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