3. ELECTRICAL SPECIFICATIONS

3.1 FOR uPD70325-8, 70325-10

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test conditions	Rating	Unit
Supply voltage	V_{DD}		-0.5 to +7.0	V
	V_{TH}		-0.5 to V_{DD}+0.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Low level output current	I_{OL}	Per pin	4.0	mA
		Total, all output	50	mA
High level output current	I_{OH}	Per pin	-2.0	mA
		Total, all output	-20	mA
Operating temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

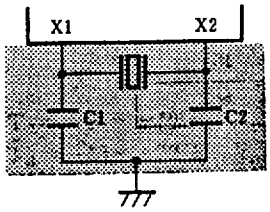
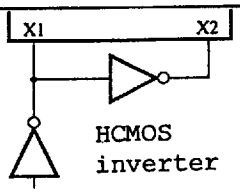
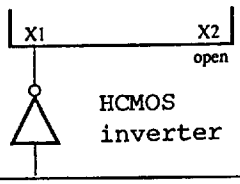
Caution 1: Do not directly connect output (or input/output) pins of IC products to each other or to V_{DD} or V_{CC} or GND. However, open drain pins and open collector pins can be connected to each other.
Direct connection can be made at an external circuit where timing design is made to avoid output collision with pins which become high impedance.

Caution 2: If one of the parameters exceeds the absolute maximum ratings even instantaneously, the product quality may be damaged. This means that the absolute maximum ratings are rated values which may physically damage the products Preferably, use the products at values less than the absolute maximum ratings.
The specifications and test conditions listed under the DC and AC characteristics are the range in which the normal operation and quality of the product are guaranteed.

Oscillator characteristics

uPD70325-8 (Ta = -10 to +70°C, V_{DD} = +5.0V±10%, V_{SS} = 0V, 0V ≤ V_{TH} ≤ V_{DD}+0.1V)

uPD70325-10 (Ta = -10 to +70°C, V_{DD} = +5.0V±5%, V_{SS} = 0V, 0V ≤ V_{TH} ≤ V_{DD}+0.1V)

Oscillator	Recommended circuit	Parameter	uPD70325-8 MIN.	uPD70325-8 MAX.	uPD70325-10 MIN.	uPD70325-10 MAX.	Unit
Ceramic oscillator or crystal resonator		Oscillation frequency (f_{XX})	4	16	4	20	MHz
External clock	①  Or ② 	X1 input frequency (f_X)	4	16	4	20	MHz
		X1 input rising, falling time (t_{XR}, t_{XF})	0	20	0	15	ns
		X1 input high, low level width (t_{WXH}, t_{WXL})	20		16		ns

Remarks 1: Place the oscillation circuit as near the X1 and X2 pins as possible.

2: Do not pass other signal lines through the shaded area.

Recommended oscillation circuit constant

(1) The following are recommended for ceramic resonators and external capacitance.

Manufacturer	Product Name	Recommended Constant	
		C1 [pF]	C2 [pF]
Murata Mfg.	CSA16.00MX040	30	30
	CSA20.00MX040	10	10
TDK	FCR16.0M2G	30	30

(2) The following are recommended for crystal resonators and external capacitance.

Manufacturer	Product Name	Recommended Constant	
		C1[pF]	C2[pF]
Kinseki	HC-49/U (KR-100)	22	22
	HC-49/U (KR-160)	22	22
	HC-49/U (KR-200)	22	22

Remarks: For such as characteristics of each oscillator, confirm to the each maker.

Capacitance (Ta = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C=1 MHz Pins other than the measured pin: 0V			10	pF
Output capacitance	C_O				20	pF
Input/output capacitance	C_{IO}				20	pF

DC characteristics

uPD70325-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)
uPD70325-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Input voltage low	V_{IL}			0		0.8	V
Input voltage high	V_{IH1}	Other than $\overline{RESET}$, P10/NMI, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P10/NMI, X1, X2		0.8 V_{DD}		V_{DD}	V
Output voltage low	V_{OL}	I_{OL}=1.6 mA				0.45	V
Output voltage high	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-1.0			V
Input current	I_I	$\overline{EA}$, P10/NMI; $0 \leq V_I \leq V_{DD}$				±20	uA
Input leakage current	I_{LI}	Other than $\overline{EA}$ and P10/NMI; $0 \leq V_I \leq V_{DD}$				±10	uA
Output leakage current	I_{LO}	$0 \leq V_O \leq V_{DD}$				±10	uA
V_{TH} current	I_{TH}	$0\ V \leq V_{TH} \leq V_{DD}$			0.5	1.0	mA
V_{DD} supply	I_{DD1}	Operating model	uPD70325-8		65	120	mA
			uPD70325-10		95	130	mA
	I_{DD2}	HALT mode	uPD70325-8		25	50	mA
			uPD70325-10		30	55	mA
	I_{DD3}	STOP mode			10	30	uA

AC characteristics

(1) uPD70325-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		62	250	ns
X1 input high/low level width	t_{WXH}, t_{WXL}		20		ns
X1 input rising/falling time	t_{XR}, t_{XF}			20	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T=t_{CYK}	125	2000	ns
CLKOUT output high/low level width	t_{WKH}, t_{WKL}		0.5T-15		ns
CLKOUT output rising/falling time	t_{KR}, t_{KF}			15	ns
Input rising/falling time	t_{IR}, t_{IF}	Other than $\overline{RESET}$, NMI, X1 and X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{RESET}$, NMI		30	ns
Output rising/falling time	t_{OR}, t_{OF}	Other than CLKOUT		20	ns
Address delay time from CLKOUT	t_{DKA}		15	90	ns
Data input delay time from address	t_{DADR}			(n+1.5)T-70	ns
Data delay time from $\overline{MREQ}\downarrow$	t_{DMRD}			(n+1)T-60	ns
Data delay time from $\overline{MSTB}\downarrow$	t_{DMSD}			(n+0.5)T-60	ns
$\overline{MSTB}\downarrow$ delay time from $\overline{MREQ}\downarrow$	t_{DMRMS}		0.5T-35	0.5T+35	ns
$\overline{MREQ}$ low level width	t_{WMRL}		(n+1)T-30	(n+1)T+30	ns
Address hold time (from $\overline{MREQ}\downarrow$)	t_{HMA}		0.5T-30		ns

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Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Data input hold time (from $\overline{MREQ}\downarrow$)	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Data output delay time from address	t_{DADW}		0.5T-35	0.5T+50	ns
Address setup time (to $\overline{MREQ}\downarrow$)	t_{DAMR}		0.5T-30		ns
Address setup time (to $\overline{MSTB}\downarrow$)	t_{DAMS}		T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL}		(n+0.5)T-30	(n+0.5)T+30	ns
Data output setup time (to $\overline{MSTB}\downarrow$)	t_{SDM}		(n+1)T-50		ns
Data output hold time (to $\overline{MSTB}\downarrow$)	t_{HMDW}		0.5T-30		ns
$\overline{IOSTB}$ Address setup time (to $\overline{IOSTB}\downarrow$)	t_{DAIS}		0.5T-30		ns
Data delay time from $\overline{IOSTB}\downarrow$	t_{DISD}			(n+1)T-60	ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-30		ns
Address hold time (from $\overline{IOSTB}\downarrow$)	t_{HISA}		0.5T-30		ns
Data input hold time (from $\overline{IOREQ}\downarrow$)	t_{HISDR}		0		ns
Data output setup time (to $\overline{IOSTB}\uparrow$)	t_{SDIS}		(n+1)T-50		ns
Data output hold time (from $\overline{IOSTB}\uparrow$)	t_{HISDW}		0.5T-30		ns
$\overline{DMARQ}$ setup time (to $\overline{MREQ}\downarrow$)	t_{SDADQ}	Demand release mode, n ≥ 2		(n-1)T-50	ns
$\overline{DMARQ}$ hold time (from $\overline{DMAAK}\downarrow$)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}	Read operation	(n+1.5)T-30		ns
$\overline{TC}\downarrow$delay time from $\overline{DMAAK}\downarrow$	t_{DDATC}			0.5T+50	ns
$\overline{TC}$ low level width	t_{WTCL}		(n+2)T-30		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}	Write operation	(n+1)T-30		ns

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Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{\text{REFRQ}}\downarrow$)	t_{DARF}		0.5T-30		ns
$\overline{\text{REFRQ}}$ low level width	t_{WRFL}		(n+1)T-30		ns
Address hold time (from $\overline{\text{REFRQ}}\downarrow$)	t_{HRFA}		0.5T-30		ns
$\overline{\text{RESET}}$ low level width	t_{WRSL1}	STOP mode release/power ON reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time (to $\overline{\text{MREQ}}\downarrow$, $\overline{\text{IOSTB}}\downarrow$)	t_{SCRYO}	$n \geq 2$		T-100	ns
	t_{SCRY}	$n \geq 3$		(n-1)T-100	ns
READY hold time (from $\overline{\text{MREQ}}\uparrow$, $\overline{\text{IOSTB}}\uparrow$)	t_{HCRYO}	$n = 2$	T		ns
	t_{HCRY}	$n \geq 3$	(n-1)T		ns
	t_{HCRY1}	$n \geq 3$	(n-2)T		ns
HLDRQ setup time (to CLKOUT$\downarrow$)	t_{SHQK}		30		ns
$\overline{\text{HLDAK}}\downarrow$ delay time from CLKOUT$\downarrow$	t_{DKHA}		15	80	ns
$\overline{\text{HLDAK}}\downarrow$ delay time from bus float	t_{CFHA}		T-50		ns
Bus output delay time from $\overline{\text{HLDAK}}\downarrow$	t_{DHAC}		T-50		ns
$\overline{\text{HLDAK}}\downarrow$ delay time from HLDRQ$\downarrow$	t_{DHQHA}			3T+160	ns
Bus output delay time from HLDRQ$\downarrow$	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{\text{HLDAK}}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time (to CLKOUT$\downarrow$)	t_{SIQK}		30		ns
INT, DMARQ high/ low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{\text{POLL}}$ setup time (to CLKOUT$\downarrow$)	t_{SPLK}		2T		ns
NMI high/low level width	t_{WNIH}, t_{WNIL}		5		us

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Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
CTS low level width	t_{WCTL}		2T		ns
INT setup time (to CLKOUT↓)	t_{SIRK}		30		ns
$\overline{INTAK}$↓ delay time from CLKOUT↓	t_{DKIA}		15	80	ns
INT hold time (from $\overline{INTAK}$)	t_{HIAIQ}		0		ns
$\overline{INTAK}$ low level width	t_{WIAL}		2T-30		ns
$\overline{INTAK}$ high level width	t_{WIAH}		T-30		ns
Data delay time from $\overline{INTAK}$↓	t_{DIAD}			2T-130	ns
Data hold time (from $\overline{INTAK}$↑)	t_{HIAD}		0	0.5T	ns
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns
$\overline{SCKO}$ high/low level width	t_{WSTH}, t_{WSTL}		450		ns
TxD delay time from $\overline{SCKO}$↓	t_{DTKD}			210	ns
TxD hold time (from $\overline{SCKO}$↓)	t_{HTKD}		20		ns
$\overline{CTSO}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTSO}$ high/low level width	t_{WSRH}'', t_{WSRL}		420		ns
RxD setup/hold time (to/from $\overline{CTSO}$↓)	t_{SRDK}'', t_{HKRD}		80		ns

Remarks: n indicates the number of wait states. No wait is "n = 0".

(2) uPD70325-10 (Ta = -10 to +70°C, V_{DD} = +5.0 V±5%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		49	250	ns
X1 input high/low level width	t_{WXH}, t_{WXL}		16		ns
X1 input rising/falling time	t_{XR}, t_{XF}			15	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T=t_{CYK}	100	2000	ns
CLKOUT output high/low level width	t_{WKH}, t_{WKL}		0.5T-12		ns
CLKOUT output rising/falling time	t_{KR}, t_{KF}			12	ns
Input rising/falling time	t_{IR}, t_{IF}	Other than $\overline{RESET}$, NMI, X1 and X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{RESET}$, NMI		30	ns
Output rising/falling time	t_{OR}, t_{OF}	Other than CLKOUT		15	ns
Address delay time from CLKOUT	t_{DKA}		15	75	ns
Data input delay time from address	t_{DADR}			(n+1.5)T-60	ns
Data delay time from $\overline{MREQ}\downarrow$	t_{DMRD}			(n+1T)-50	ns
Data delay time from $\overline{MSTB}\downarrow$	t_{DMSD}			(n+0.5)T-50	ns
$\overline{MSTB}\downarrow$ delay time from $\overline{MREQ}\downarrow$	t_{DMRMS}		0.5T-20	0.5T+30	ns
$\overline{MREQ}$ low level width	t_{WMRL}		(n+1)T-25	(n+1)T+25	ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Address hold time (from $\overline{MREQ}\downarrow$)	t_{HMA}		0.5T-30		ns
Data input hold time (from $\overline{MREQ}\downarrow$)	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Data output delay time from address	t_{DADW}		0.5T-30	0.5T+50	ns
Address setup time (to $\overline{MREQ}\downarrow$)	t_{DAMR}		0.5T-30		ns
Address setup time (to $\overline{MSTB}\downarrow$)	t_{DAMS}		T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL}		(n+0.5)T-25	(n+0.5)T+25	ns
Data output setup time (to $\overline{MSTB}\downarrow$)	t_{SDM}		(n+1)T-50		ns
Data output hold time (from $\overline{MSTB}\downarrow$)	t_{HMDW}		0.5T-30		ns
Address setup time (to $\overline{IOSTB}\downarrow$)	t_{DAIS}		0.5T-30		ns
Data delay time from $\overline{IOSTB}\downarrow$	t_{DISD}			(n+1)T-50	ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-25		ns
Address hold time (from $\overline{IOSTB}\downarrow$)	t_{HISA}		0.5T-30		ns
Data input hold time (from $\overline{IOREQ}\downarrow$)	t_{HISDR}		0		ns
Data output setup time (to $\overline{IOSTB}\downarrow$)	t_{SDIS}		(n+1)T-50		ns
Data output hold time (from $\overline{IOSTB}\downarrow$)	t_{HISDW}		0.5T-30		ns
$\overline{DMARQ}$ setup time (to $\overline{MREQ}\downarrow$)	t_{SDADQ}	Demand release mode, $n \geq 2$		(n-1)T-50	ns

(to be continued)

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Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{DMARQ}$ hold time (from $\overline{DMAAK}\downarrow$)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}	Read operation	(n+1.5)T-25		ns
$\overline{TC}\downarrow$ delay time from $\overline{DMAAK}\downarrow$	t_{DDATC}			0.5T+35	ns
$\overline{TC}$ low level width	t_{WTCL}		(n+2)T-25		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}	Write operation	(n+1)T-25		ns
Address setup time (to $\overline{REFRQ}\downarrow$)	t_{DARF}		0.5T-30		ns
$\overline{REFRQ}$ low level width	t_{WRFL}		(n+1)T-25		ns
Address hold time (from $\overline{REFRQ}\downarrow$)	t_{HRFA}		0.5T-30		ns
$\overline{RESET}$ low level width	t_{WRSL1}	STOP mode release/power ON reset	30		ms
	t_{WRSL2}	System reset	5		us
READY setup time (to $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{SCRY0}	$n \geq 2$		T-80	ns
	t_{SCRY}	$n \geq 3$		(n-1)T-80	ns
READY hold time (from $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{HCRY0}	$n = 2$	T		ns
	t_{HCRY}	$n \geq 3$	(n-1)T		ns
	t_{HCRY1}	$n \geq 3$	(n-2)T		ns
HLDRQ setup time (to CLKOUT$\downarrow$)	t_{SHQK}		25		ns
$\overline{HLDAK}\downarrow$ delay time from CLKOUT$\uparrow$	t_{DKHA}		15	70	ns
$\overline{HLDAK}\uparrow$ delay time from bus float	t_{CFHA}		T-35		ns

(to be continued)

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Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Bus output delay time from $\overline{HLDAK}\downarrow$	t_{DHAC}		T-35		ns
$\overline{HLDAK}\downarrow$ delay time from HLDRQ $\downarrow$	t_{DHQHA}			3T+160	ns
Bus output delay time from HLKRQ $\downarrow$	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{HLDAK}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time (to CLKOUT$\downarrow$)	t_{SIQK}		25		ns
INT, DMARQ high/ low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{POLL}$ setup time (to CLKOUT$\downarrow$)	t_{SPLK}		25		ns
NMI high/low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{CTS}$ low level width	t_{WCTL}		2T		ns
INT setup time (to CLKOUT$\downarrow$)	t_{SIRK}		25		ns
$\overline{INTAK}\downarrow$ delay time from CLKOUT $\downarrow$	t_{DKIA}		15	70	ns
INT hold time (from $\overline{INTAK}\downarrow$)	t_{HIAIQ}		0		ns
$\overline{INTAK}$ low level width	t_{WIAL}		2T-25		ns
$\overline{INTAK}$ high level width	t_{WIAH}		T-25		ns
Data delay time from $\overline{INTAK}\downarrow$	t_{DIAD}			2T-100	ns
Data hold time (from $\overline{INTAK}\uparrow$)	t_{HIAD}		0	0.5T	ns
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns

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Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{SCK0}$ high/low level width	t_{WSTH}, t_{WSTL}		450		ns
TxD delay time from $\overline{SCK0}\downarrow$	t_{DTKD}			210	ns
TxD hold time (from $\overline{SCK0}\downarrow$)	t_{HTKD}		20		ns
$\overline{CTS0}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTS0}$ high/low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup/hold time (to/from $\overline{CTS0}\downarrow$)	t_{SRDK}, t_{HKRD}		80		ns

Remarks: n indicates the number of wait states. No wait is "n = 0".

Comparator characteristics

uPD70325-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)
uPD70325-10 (Ta=-10 to +70°C, V_{DD}=+5.0V±5%)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}+0.1	V
Comparison time	t_{COMP}		64		65	t_{CYK}
PT input voltage	V_{IPT}		0		V_{DD}	V

Data Memory STOP Mode Low Supply Voltage Data Holding Characteristics (Ta=-10 to +70°C)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising/falling time	t_{RVD}, t_{FVD}		200		us

3.2 FOR uPD70325(A)-9

Absolute maximum Ratings (Ta = 25°C)

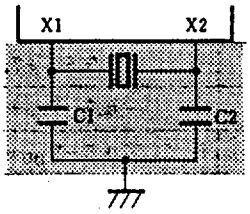
Parameter	Symbol	Test condition	Rating	Unit
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	V_{TH}		-0.5 to V_{DD}+0.5	V
Input voltage	V_I		-0.5 to V_{DD}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output current low	I_{OL}	1 pin	4.0	mA
		Total, all pins	50	mA
Output current high	I_{OH}	1 pin	-2.0	mA
		Total, all pins	-20	mA
Oprating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution 1: Do not directly connect output (or input/output) pins of IC products to each other or to V_{DD} or V_{CC} or GND. However, open drain pins and open collector pins can be connected to each other.
Direct connection can be made at an external circuit where timing design is made to avoid output collision with pins which become high impedance.

Caution 2: If one of the parameters exceeds the absolute maximum ratings even instantaneously, the product quality may be damaged. This means that the absolute maximum ratings are rated values which may physically damage the products. Preferably, use the products at values less than the absolute maximum ratings.
The specifications and test conditions listed under the DC and AC characteristics are the range in which the normal operation and quality of the product are guaranteed.

Oscillator Characteristics

uPD70325(A)-9 (Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%, V_{SS} = 0 V, 0 V ≦ V_{TH} ≦ V_{DD}+0.1 V)

Resonator	Recommanded circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_{XX})	4	18	MHz
External clock	① X1 X2 HCMOS inverter Or ② X1 X2 open HCMOS inverter	X1 input frequency (f_X)	4	18	MHz
		X1 input rising, falling time (t_{XR}, t_{XF})	0	15	ns
		X1 high, low level width (t_{WXH}, t_{WXL})	17		ns

Remarks 1: Place the oscillation circuit as near the X1 and X2 pins as possible.

2: Do not pass other signal lines through the shaded area.

Capacitance (Ta = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

DC Characteristics

uPD70325(A)-9 (Ta = -40 ro +85°C, V_{DD} = +5.0 V±5%)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input voltage low	V_{IL}		0		0.8	V
Input voltage high	V_{IH1}	Other than $\overline{RESET}$, P10/NMI, X1, X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P10/NMI, X1, X2	0.8 V_{DD}		V_{DD}	V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output voltage high	V_{OH}	I_{OH} = -0.4 mA	V_{DD} -1.0			V
Input current	I_I	$\overline{EA}$, P10/NMI; 0 ≤ V_I ≤ V_{DD}			±20	uA
Input leakage current	I_{LI}	Other than $\overline{EA}$, P10/NMI; 0 ≤ V_I ≤ V_{DD}			±10	uA
Output leakage current	I_{LO}	0 ≤ V_O ≤ V_{DD}			±10	uA
V_{TH} current	I_{TH}	0 V ≤ V_{TH} ≤ V_{DD}		0.5	1.0	mA
V_{DD} supply current	I_{DD1}	Operating mode		95	130	mA
	I_{DD2}	HALT mode		30	55	mA
	I_{DD3}	STOP mode		15	35	uA

AC Characteristics

uPD70325(A)-9 (Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
X1 input cycle time	t_{CYX}		55	250	ns
X1 input high/low level width	t_{WXH}, t_{WXL}		17		ns
X1 input rising/falling time	t_{XR}, t_{XF}			15	ns
CLKOUT output cycle time	t_{CYK}	$f_X/2$, T = t_{CYK}	111	2000	ns
CLKOUT output high/low level width	t_{WKH}, t_{WKL}		0.5T-12		ns
CLKOUT output rising/falling time	t_{KR}, t_{KF}			12	ns
Input rising/falling time	t_{IR}, t_{IF}	Other than $\overline{\text{RESET}}$, NMI, X1 and X2		20	ns
	t_{IRS}, t_{IFS}	$\overline{\text{RESET}}$, NMI		30	ns
Output rising/falling time	t_{OR}, t_{OF}	Other than CLKOUT		15	ns
Address delay time from CLKOUT	t_{DKA}		15	80	ns
Data input delay time from address	t_{DADR}			(n+1.5)T-60	ns
Data delay time from $\overline{\text{MREQ}}$↓	t_{DMRD}			(n+1)T-50	ns
Data delay time from $\overline{\text{MSTB}}$↓	t_{DMSD}			(n+0.5)T-50	ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{MSTB}\downarrow$ delay time from $\overline{MREQ}\downarrow$	t_{DMRMS}		0.5T-30	0.5T+30	ns
$\overline{MREQ}$ low level width	t_{WMRL}		(n+1)T-25	(n+1)T+25	ns
Address hold time (from $\overline{MREQ}\uparrow$)	t_{HMA}		0.5T-35		ns
Data input hold time (from $\overline{MREQ}\uparrow$)	t_{HMDR}		0		ns
Control signal recovery time	t_{RVC}		T-25		ns
Data output delay time from address	t_{DADW}			0.5T+50	ns
Address setup time (to $\overline{MREQ}\downarrow$)	t_{DAMR}		0.5T-35		ns
Address setup time (to $\overline{MSTB}\downarrow$)	t_{DAMS}		T-30		ns
$\overline{MSTB}$ low level width	t_{WMSL}		(n+0.5)T-25	(n+0.5)T+25	ns
Data output setup time (to $\overline{MSTB}\uparrow$)	t_{SDM}		(n+1)T-50		ns
Data output hold time (from $\overline{MSTB}\uparrow$)	t_{HMDW}		0.5T-35		ns
Address setup time (to $\overline{IOSTB}\downarrow$)	t_{DAIS}		0.5T-35		ns
Data delay time from $\overline{IOSTB}\downarrow$	t_{DISD}			(n+1)T-50	ns
$\overline{IOSTB}$ low level width	t_{WISL}		(n+1)T-25		ns
Address hold time (from $\overline{IOSTB}\uparrow$)	t_{HISA}		0.5T-30		ns
Data input hold time (from $\overline{IOREQ}\uparrow$)	t_{HISDR}		0		ns
Data output setup time (to $\overline{IOSTB}\uparrow$)	t_{SDIS}		(n+1)T-50		ns
Data output hold time (from $\overline{IOSTB}\uparrow$)	t_{HISDW}		0.5T-35		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{DMARQ}$ setup time (to $\overline{MREQ}\downarrow$)	t_{SDADQ}	Demand release mode, n ≥ 2		(n-1)T-50	ns
$\overline{DMARQ}$ hold time (from $\overline{DMAAK}\downarrow$)	t_{HDADQ}	Demand release mode	0		ns
$\overline{DMAAK}$ output low level width	t_{WDMRL}	Read operation	(n+1.5)T-25		ns
$\overline{TC}\downarrow$ delay time from $\overline{DMAAK}\downarrow$	t_{DDATC}			0.5T+35	ns
$\overline{TC}$ low level width	t_{WTCL}		(n+2)T-25		ns
$\overline{DMAAK}$ output low level width	t_{WDMWL}	Write operation	(n+1)T-25		ns
Address setup time (to $\overline{REFRQ}\downarrow$)	t_{DARF}		0.5T-35		ns
$\overline{REFRQ}$ low level width	t_{WRFL}		(n+1)T-25		ns
Address hold time (from $\overline{REFRQ}\uparrow$)	t_{HRFA}		0.5T-35		ns
$\overline{RESET}$ low level width	t_{WRSL1}	STOP mode release/power ON reset	30		ns
	t_{WRSL2}	System reset	5		us
READY setup time (to $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{SCRYO}	n ≥ 2		T-80	ns
	t_{SCRY}	n ≥ 3		(n-1)T-80	ns
READY hold time (from $\overline{MREQ}\downarrow$, $\overline{IOSTB}\downarrow$)	t_{HCRYO}	n = 2	T		ns
	t_{HCRY}	n ≥ 3	(n-1)T		ns
	t_{HCRY1}	n ≥ 3	(n-2)T		ns
HLDRQ setup time (to CLKOUT$\downarrow$)	t_{SHQK}		25		ns
$\overline{HLDAK}\downarrow$ delay time from CLKOUT$\downarrow$	t_{DKHA}		15	75	ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
$\overline{HLDAK}\downarrow$ delay time from bus float	t_{CFHA}		T-35		ns
Bus output delay time from $\overline{HLDAK}\downarrow$	t_{DHAC}		T-35		ns
$\overline{HLDAK}\downarrow$ delay time from HLDRQ$\downarrow$	t_{DHQHA}			3T+160	ns
Bus output delay time from HLDRQ	t_{DHQC}		3T+30		ns
HLDRQ low level width	t_{WHQL}		1.5T		ns
$\overline{HLDAK}$ low level width	t_{WHAL}		T		ns
INT, DMARQ setup time (to CLKOUT$\downarrow$)	t_{SIQK}		25		ns
INT, DMARQ high/ low level width	t_{WIQH}, t_{WIQL}		8T		ns
$\overline{POLL}$ setup time (to CLKOUT$\downarrow$)	t_{SPLK}		25		ns
NMI high/low level width	t_{WNIH}, t_{WNIL}		5		us
$\overline{CTS}$ low level width	t_{WCTL}		2T		ns
INT setup time (to CLKOUT$\downarrow$)	t_{SIRK}		25		ns
$\overline{INTAK}\downarrow$ delay time from CLKOUT$\downarrow$	t_{DKIA}		15	75	ns
INT hold time (from $\overline{INTAK}\downarrow$)	t_{HAIQ}		0		ns
$\overline{INTAK}$ low level width	t_{WIAL}		2T-25		ns
$\overline{INTAK}$ high level width	t_{WIAH}		T-25		ns
Data delay time from $\overline{INTAK}\downarrow$	t_{DIAD}			2T-100	ns
Data hold time (from $\overline{INTAK}\downarrow$)	t_{HIAD}		0	0.5T	ns
$\overline{SCKO}$ cycle time	t_{CYTK}		1000		ns
$\overline{SCKO}$ high/low level width	t_{WSTH}, t_{WSTL}		450		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
TxD delay time from $\overline{SCK0}\downarrow$	t_{DTKD}			210	ns
TxD hold time (from $\overline{SCK0}\downarrow$)	t_{HTKD}		20		ns
$\overline{CTS0}$ cycle time	t_{CYRK}		1000		ns
$\overline{CTS0}$ high/low level width	t_{WSRH}, t_{WSRL}		420		ns
RxD setup/hold time (to/from $\overline{CTS0}\uparrow$)	t_{SRDK}, t_{HKRD}		80		ns

Remarks: n indicates the number of wait states. No wait is "n = 0".

Comparator Characteristics

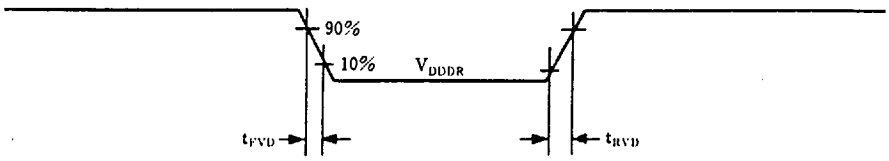
uPD70325(A)-9 (Ta = -40 to +85°C, V_{DD} = +5.0 V ±5%)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Comparator accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD} +0.1	V
Compare time	t_{COMP}		64		65	t_{CYK}
PT input voltage	V_{IPT}		0		V_{DD}	V

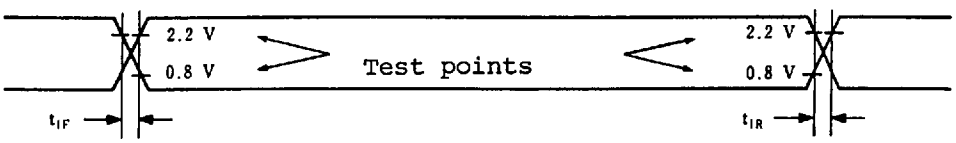
Data Memory STOP Mode Low Supply Voltage Data Holding Characteristics (Ta = -40 to +85°C)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising/falling time	t_{RVD}' t_{FVD}		200		us

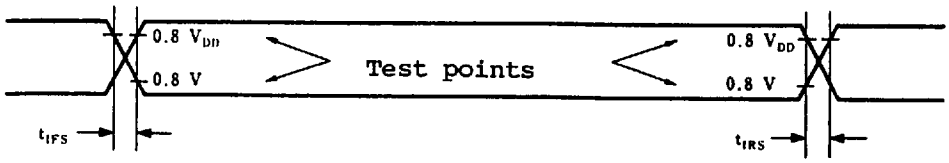
Data Hold Timing



AC Test Input Waveform (except $\overline{\text{RESET}}$, NMI, X1 and X2)

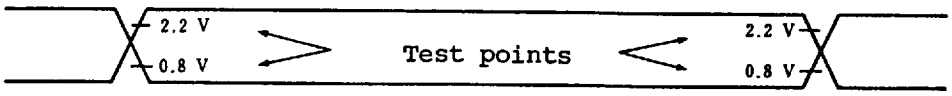


AC Test Input Waveform ($\overline{\text{RESET}}$, NMI, X1 and X2)

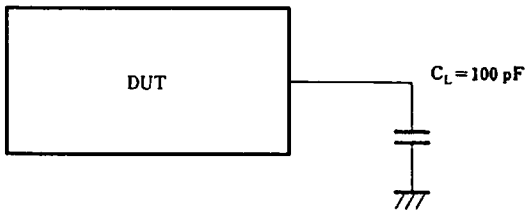


AC Test Output Test Points

Output load condition: 100 pF

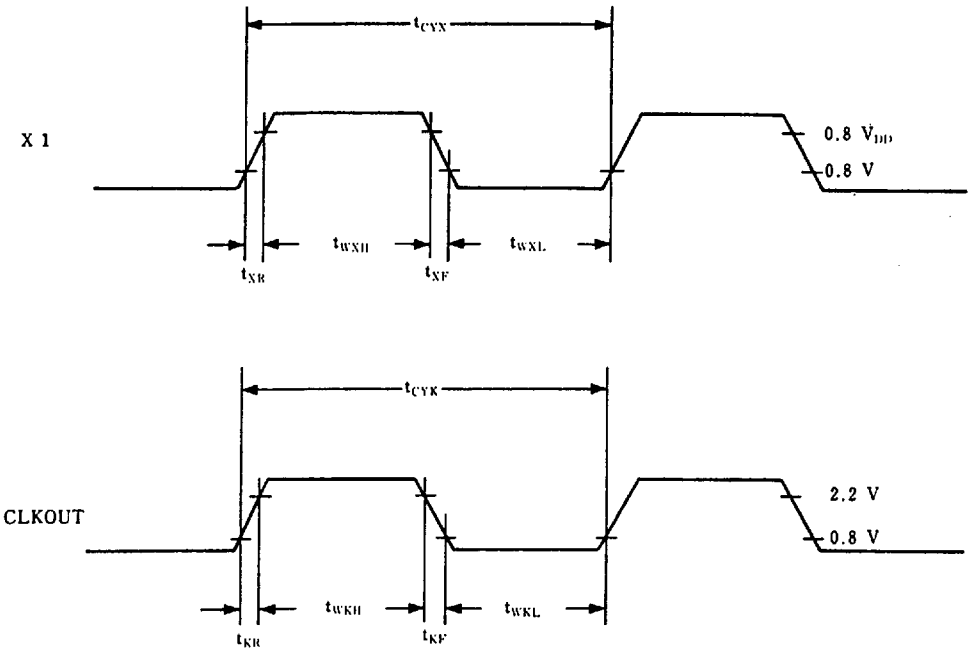


Load Conditions

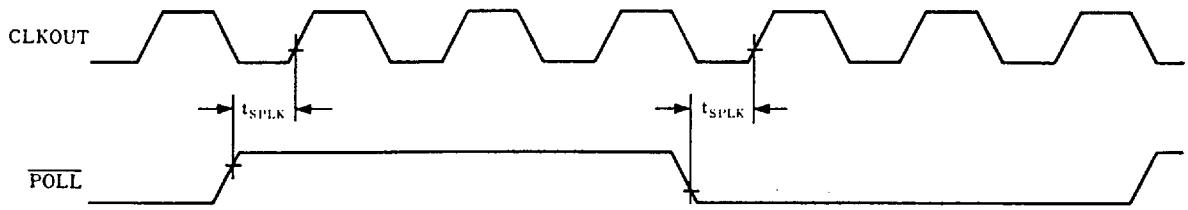


Note: If the load capacitance exceeds 100pF because of ciucuit configuration, decrease the load capacitance of this device to less than 100pF by inserting a buffer.

Clock Timing

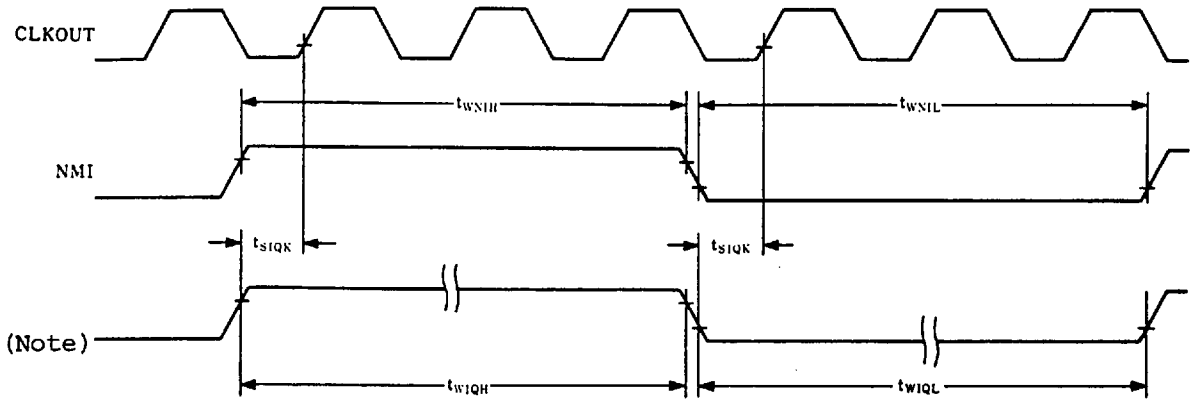


$\overline{\text{POLL}}$ Input Timing



$\overline{\text{CTS0}}$ and $\overline{\text{CTS1}}$ Input Timing

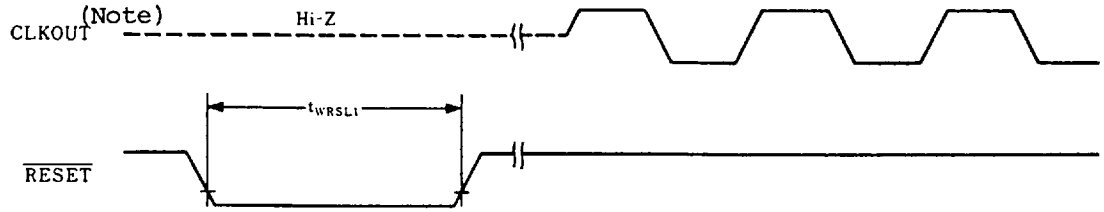
Interrupt Input/DMA Input Timing



Note: $\overline{\text{INTP0}}$ to $\overline{\text{INTP2}}$, DMARQ0 to DMARQ1

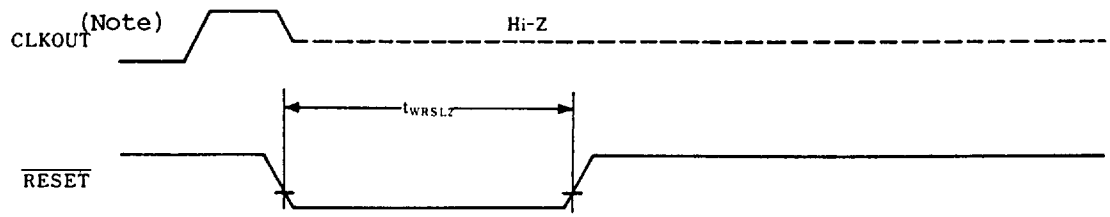
$\overline{\text{RESET}}$ Input Timing

When STOP mode is released/power-on is reset:



Note: The CLKOUT signal is output after being set to CLKOUT output.

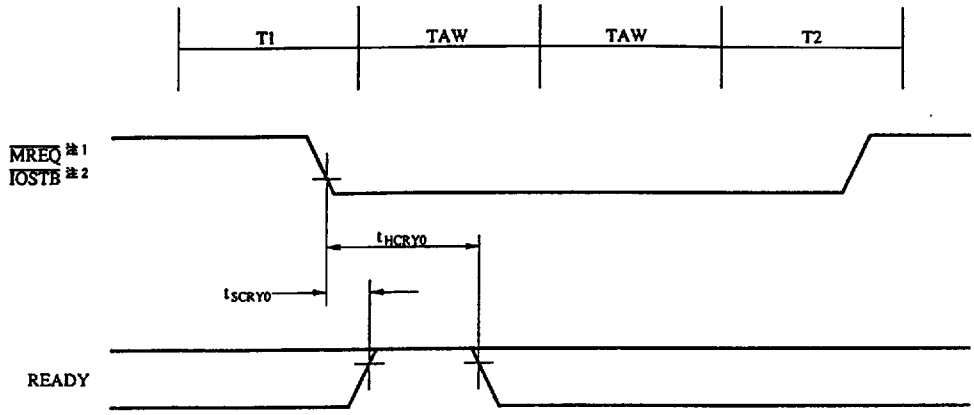
When system is reset:



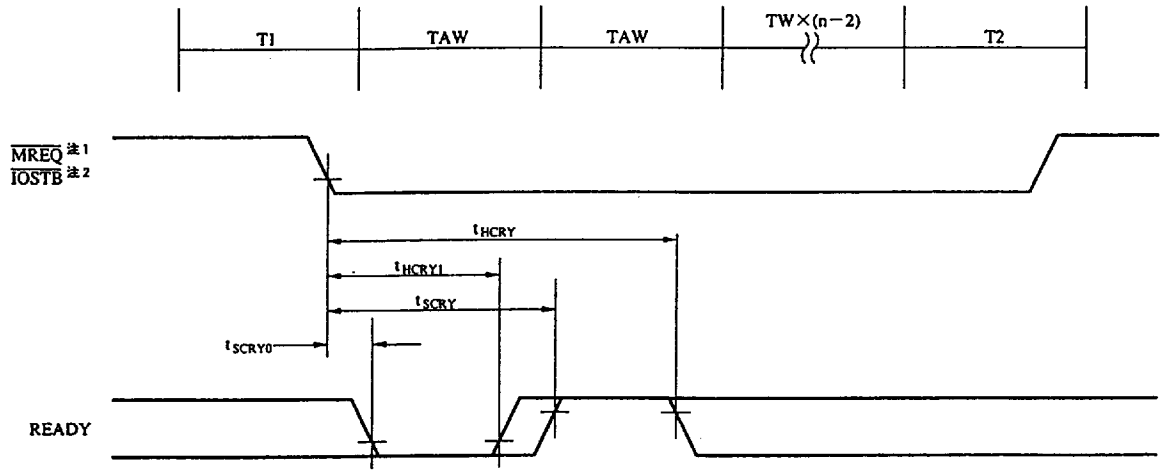
Note: The CLKOUT output is set to an input port to $\overline{\text{RESET}}$ input.

Ready Timing

When 2 wait states are inserted:



When an extra (n-2) wait state is inserted [n ≥ 3]:

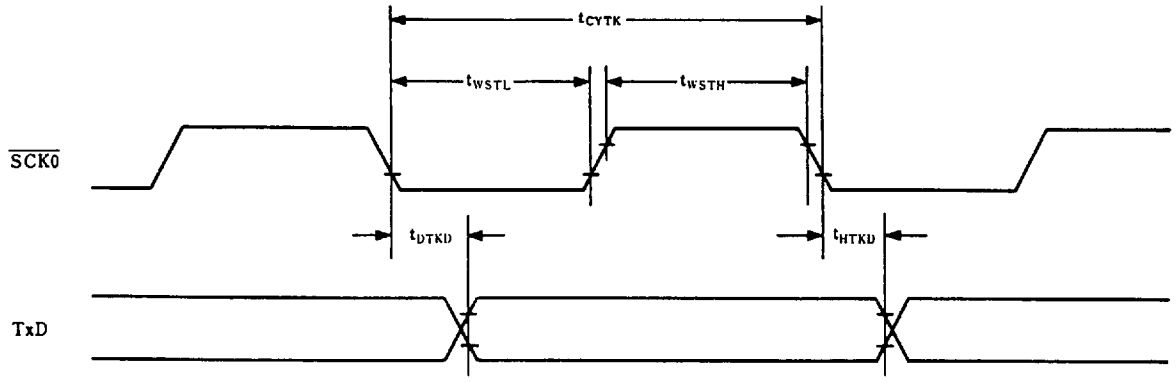


Note1: Memory cycle
2: I/O cycle

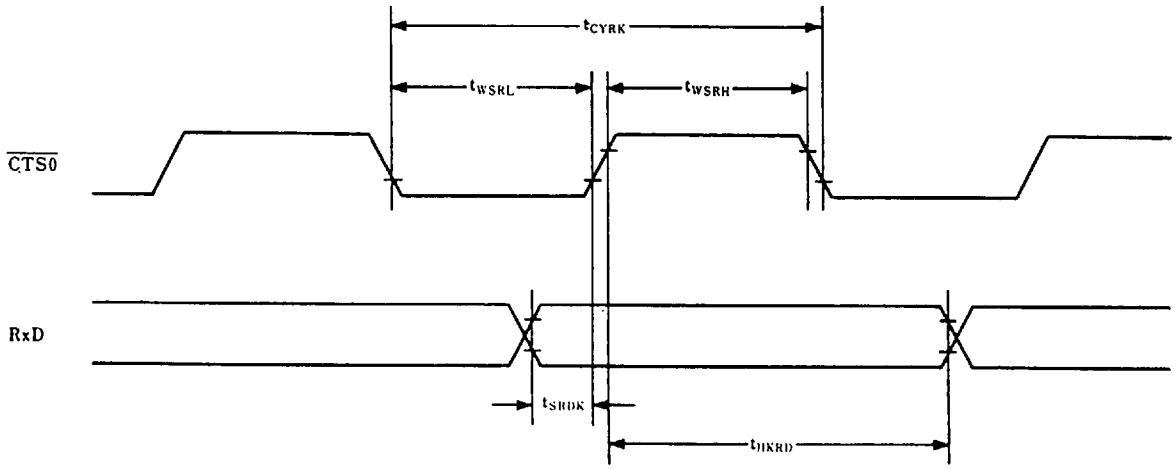
Remarks: The wait control register (WTC) value must be set to "11" (2 wait + insert state using READY pin) for wait state insertion by the external READY signal.

Serial Operation

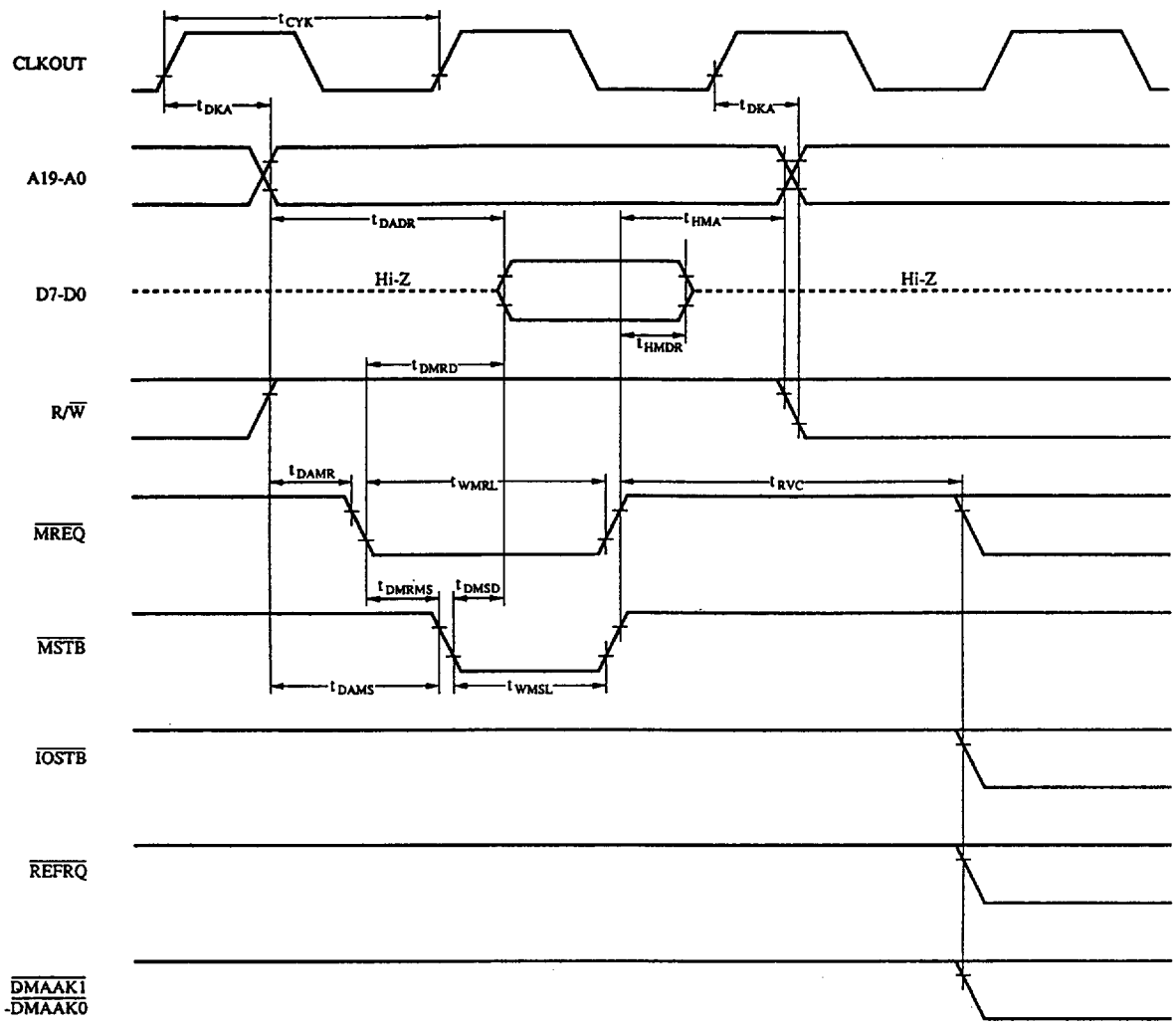
When transmitting data in I/O interface mode



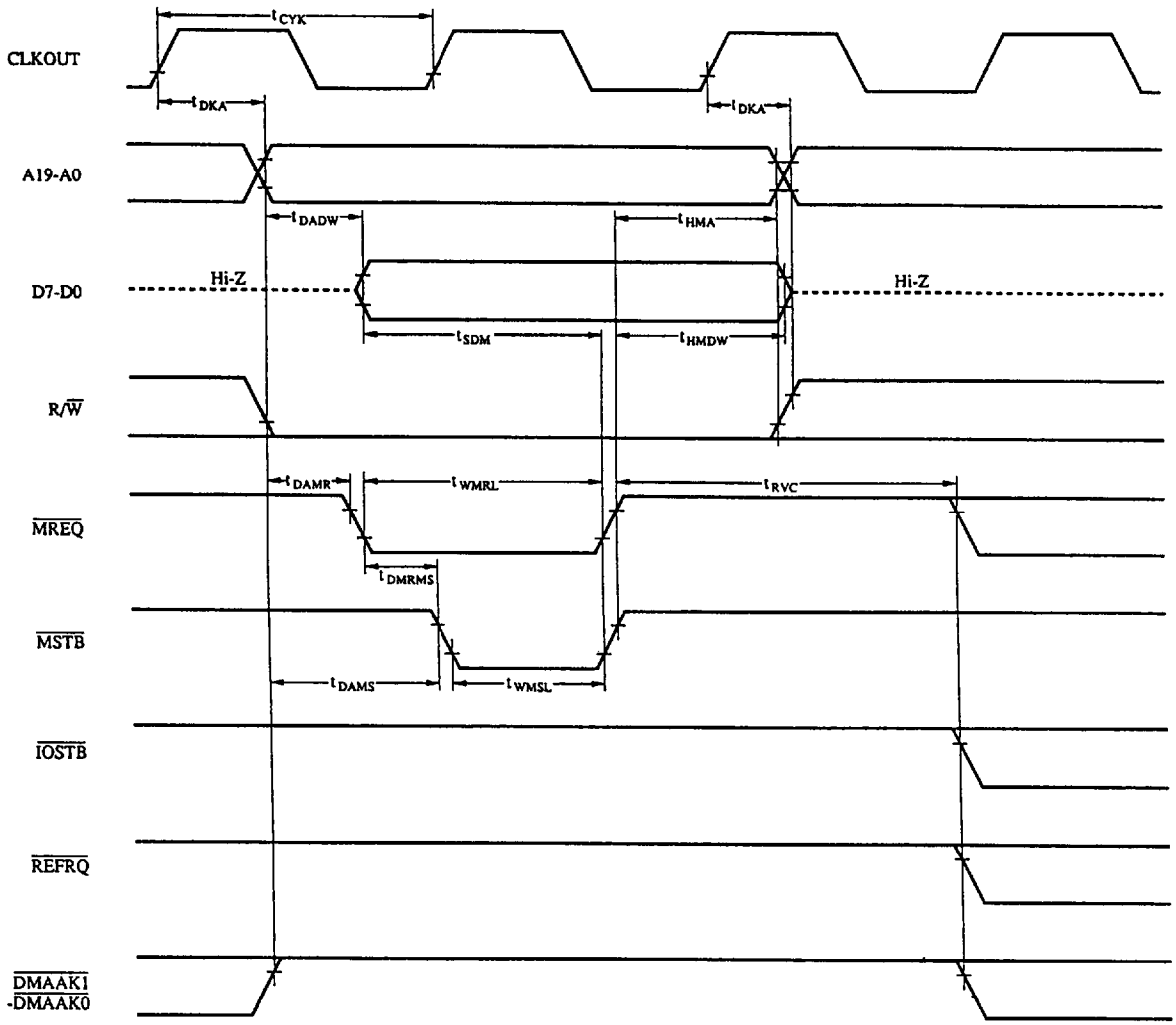
When receiving data in I/O interface mode



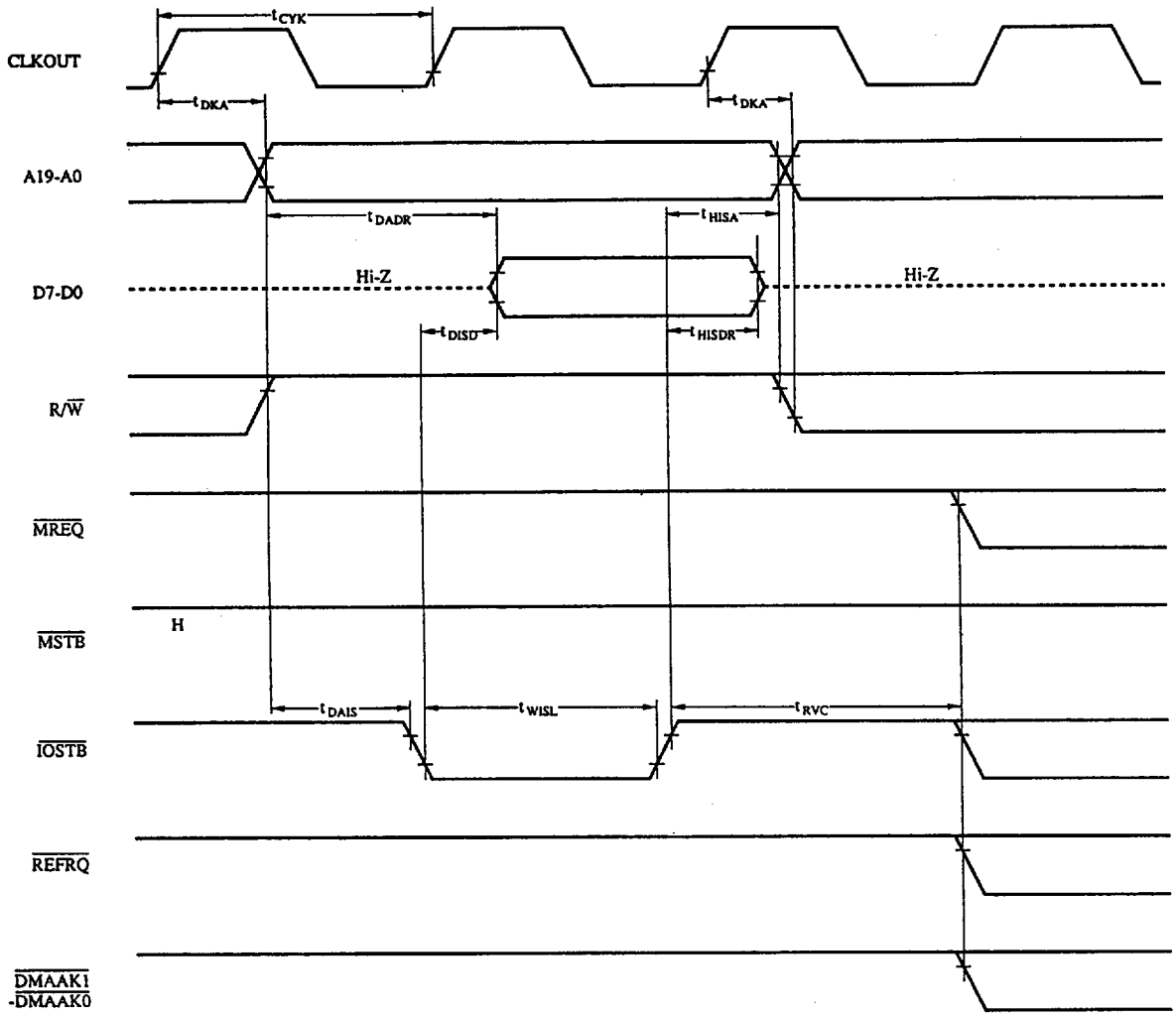
Read Operation



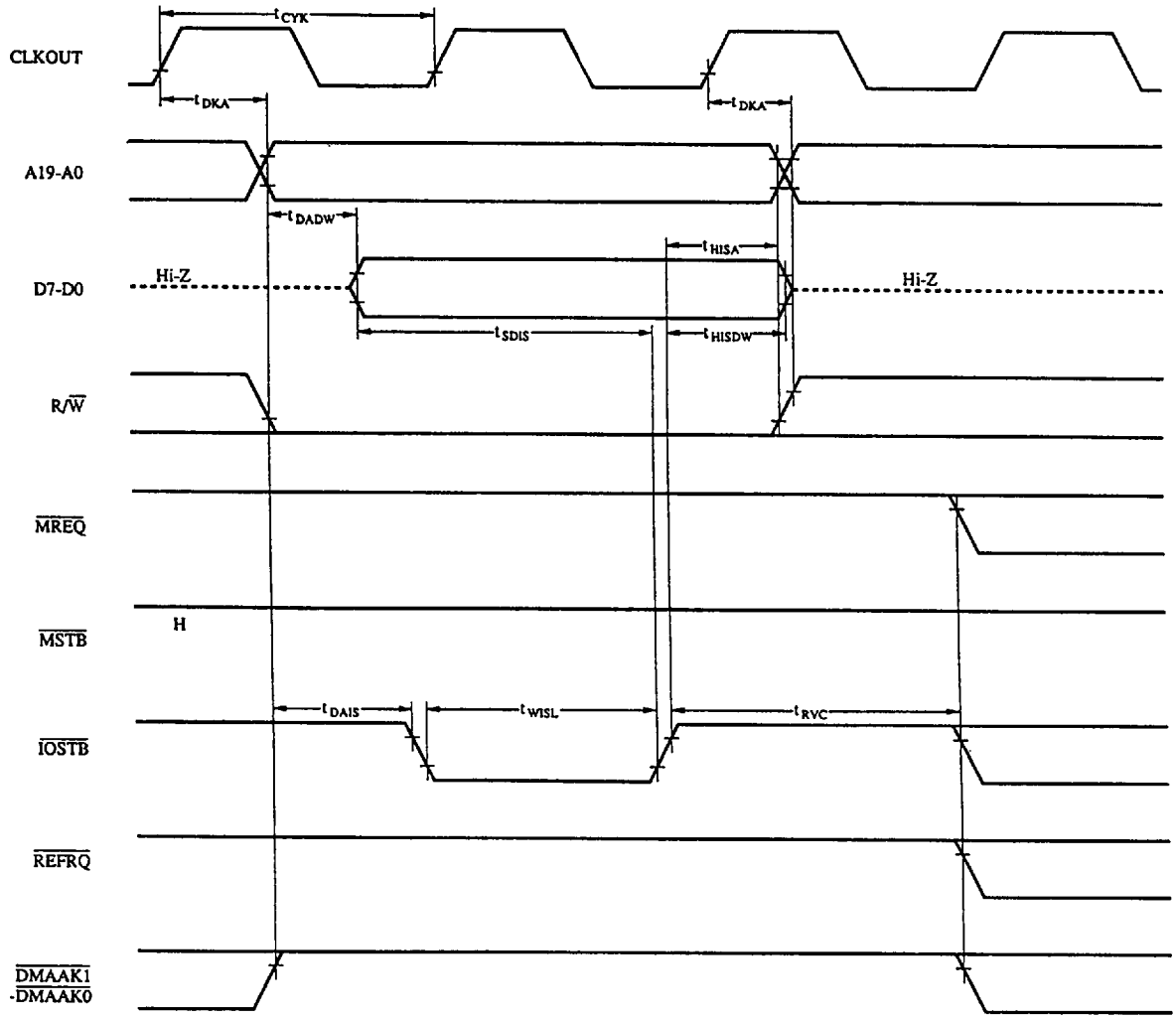
Write Operation



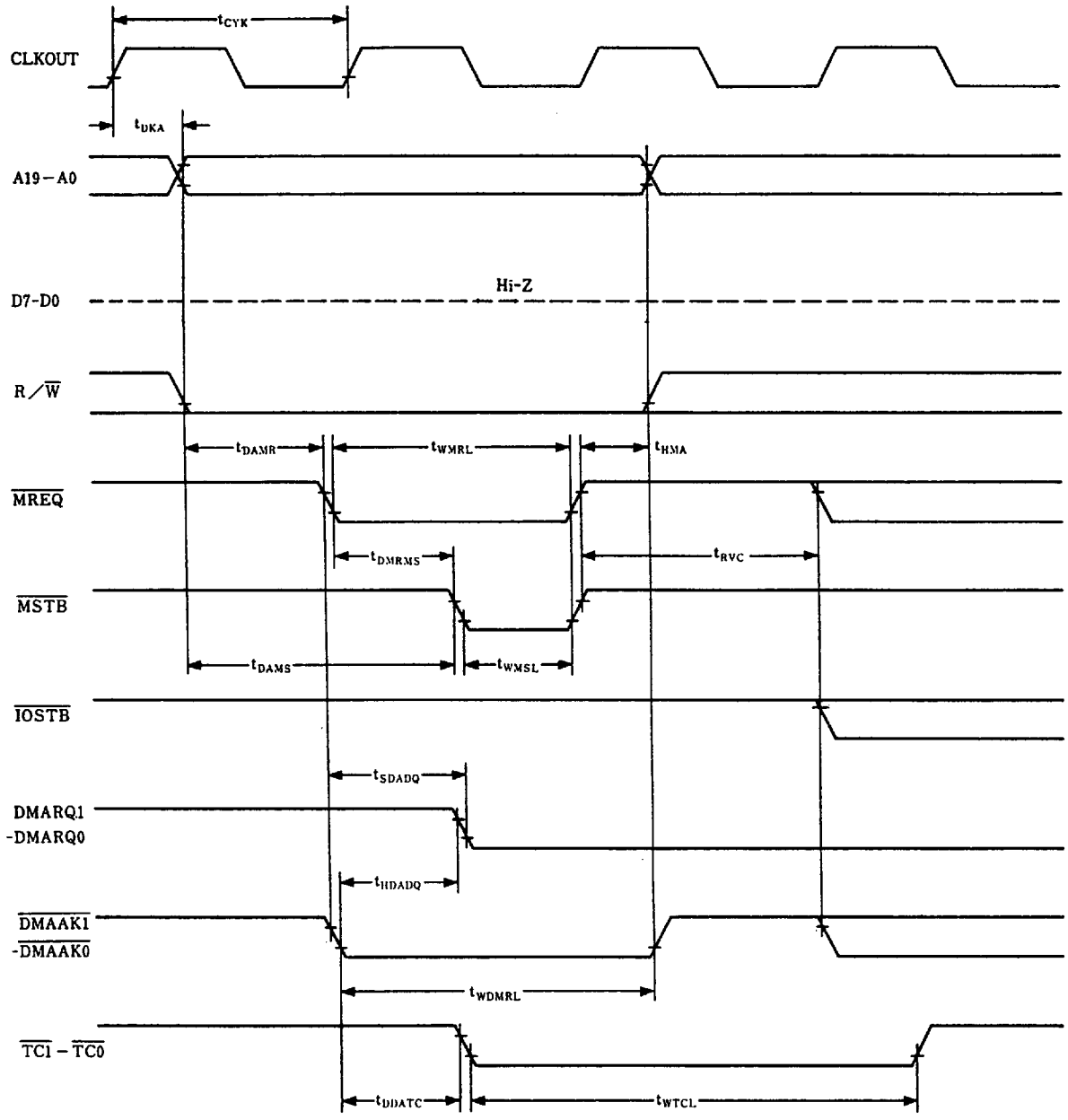
I/O Read Timing



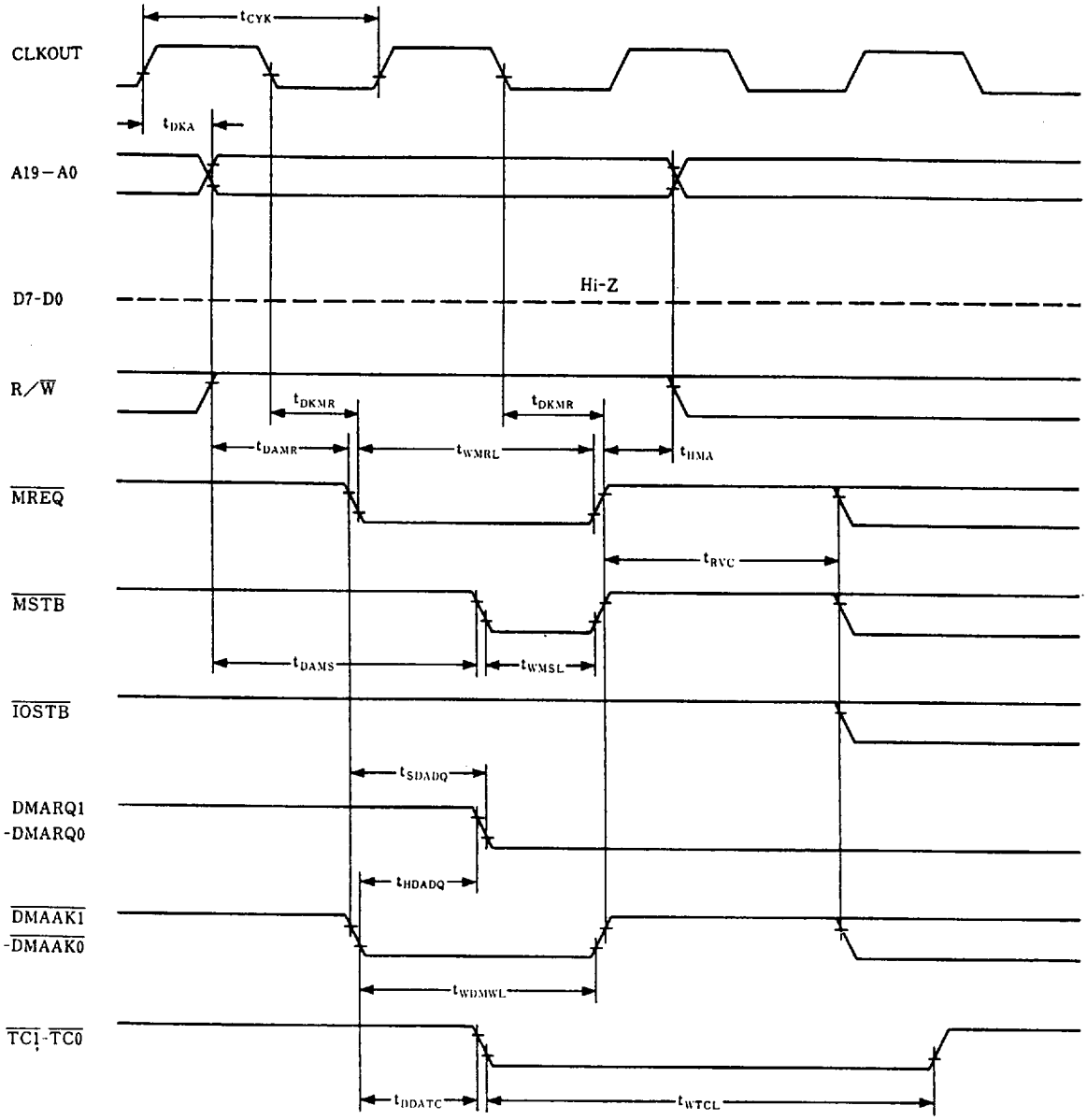
I/O Write Timing



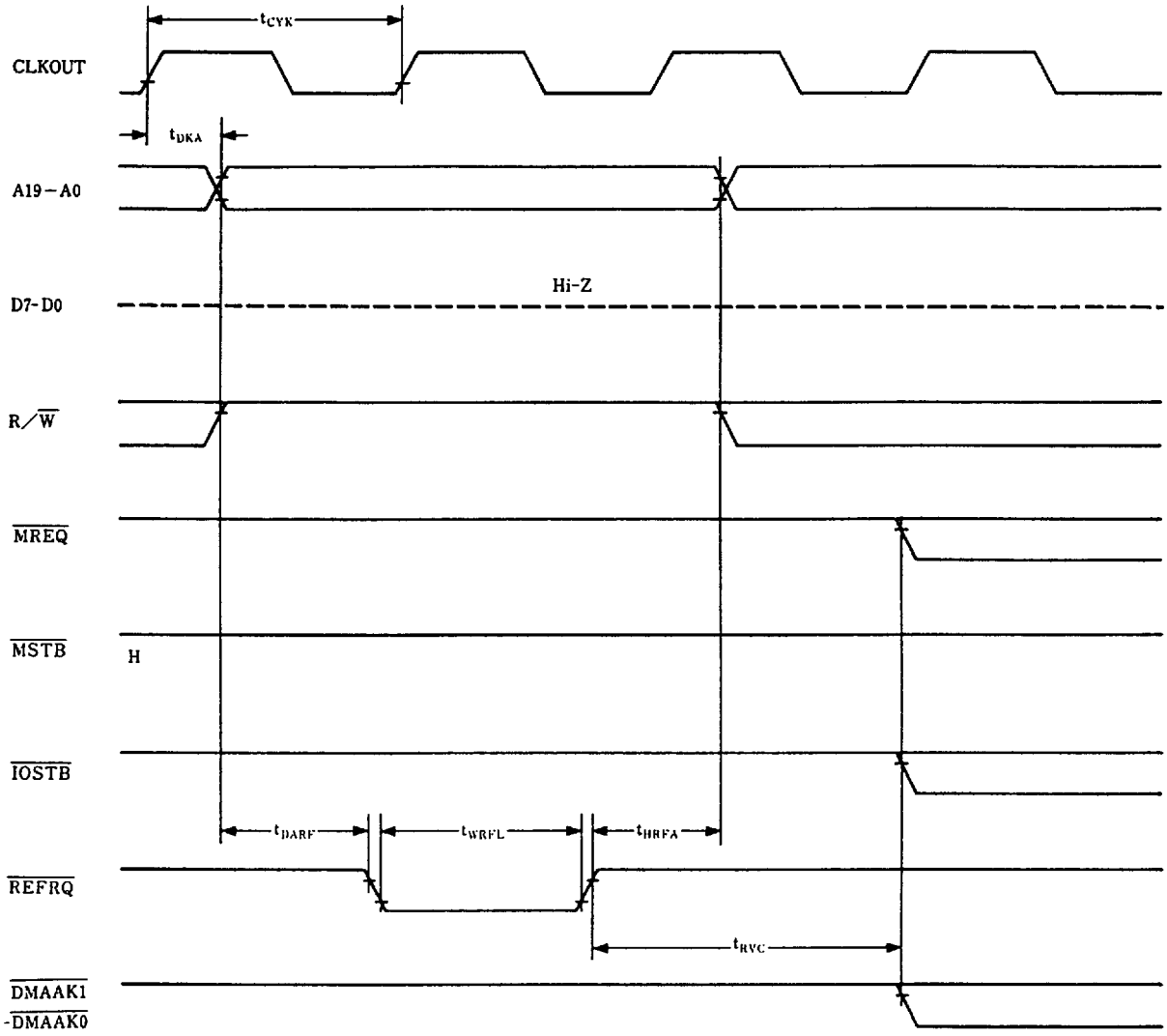
DMA (I/O ⟶ Memory) Timing



DMA (Memory → I/O) Timing

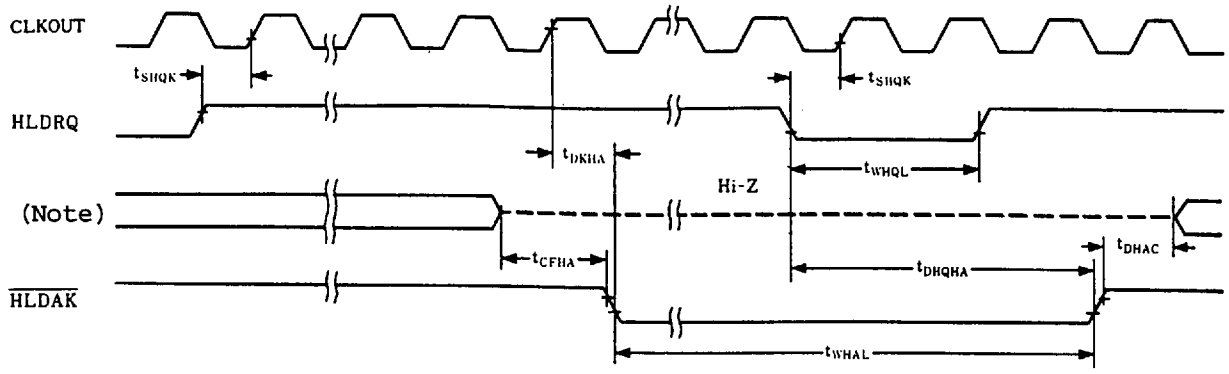


Refresh Timing

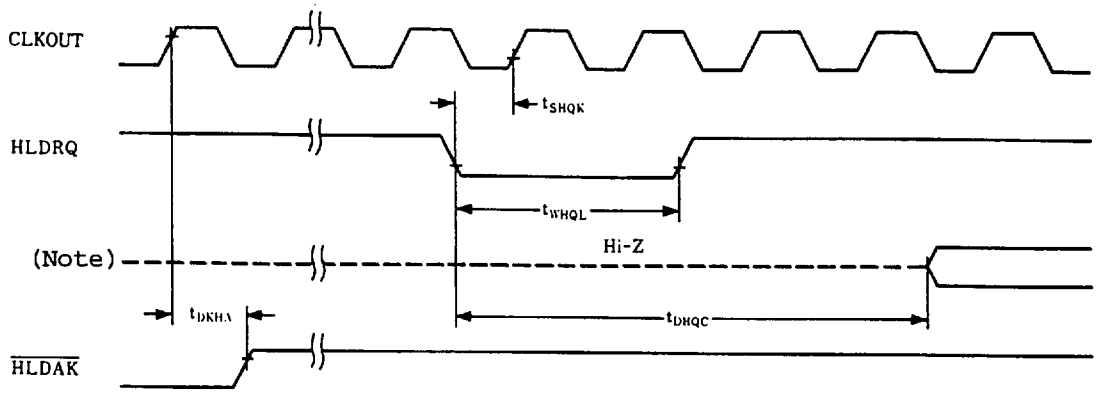


Hold Request/Acknowledge Timing

Normal mode

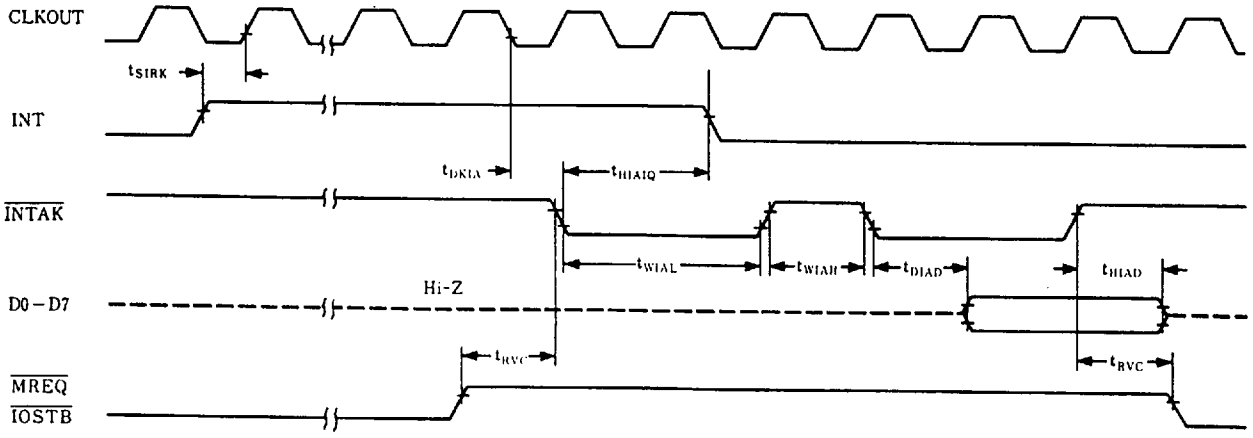


HOLD mode release at refresh



Note: A19 to A0, D7 to D0, $\overline{MREQ}$, $\overline{MSTB}$, $\overline{IOSTB}$, R/$\overline{W}$

External Interrupt Request/Acknowledge Timing



3.3 Clock Synchronization Timing

The V25 family is designed to generate access signals to the memory and I/O from the $\overline{MREQ}$ and $\overline{IOSTB}$ signals. In connecting to the memory or I/O, design can be made even if there is no AC characteristic of clock reference. The clock synchronization timing listed below is provided for accurate READY input control with the system clock.

(1) uPD70325-8 (Ta=-10 to +70°C, V_{DD}=+5.0V±10%)

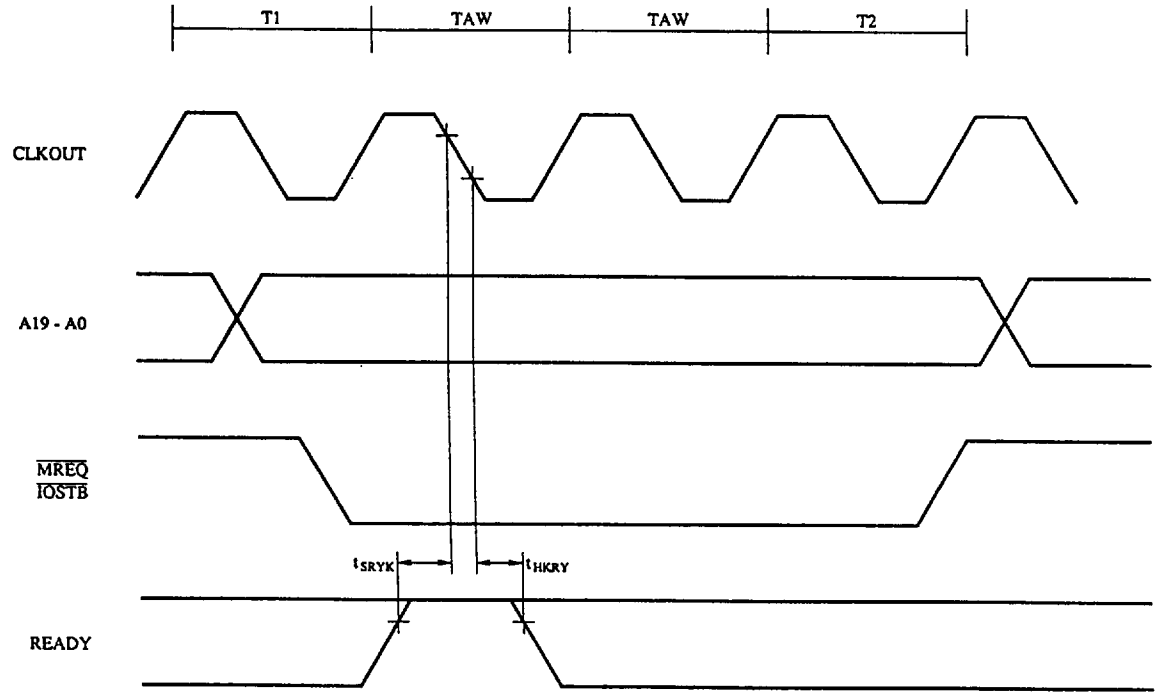
Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Address delay time from CLKOUT	t_{DKD}		65	115	ns
Data input setup time	t_{SDK}		15		ns
Data input hold time	t_{HKD}		40		ns
$\overline{MREQ}$ delay time	t_{DKMR}		10	55	ns
$\overline{IOSTB}$ delay time	t_{DKIS}		10	55	ns
READY setup time	t_{SRYK}		20		ns
READY hold time	t_{HKRY}		40		ns

(2) uPD70325-10 (Ta=-10 to +70°C, V_{DD}=5.0V±5%)
uPD70325(A)-9 (Ta=-40 to 85°C, V_{DD}=5.0V±5%)

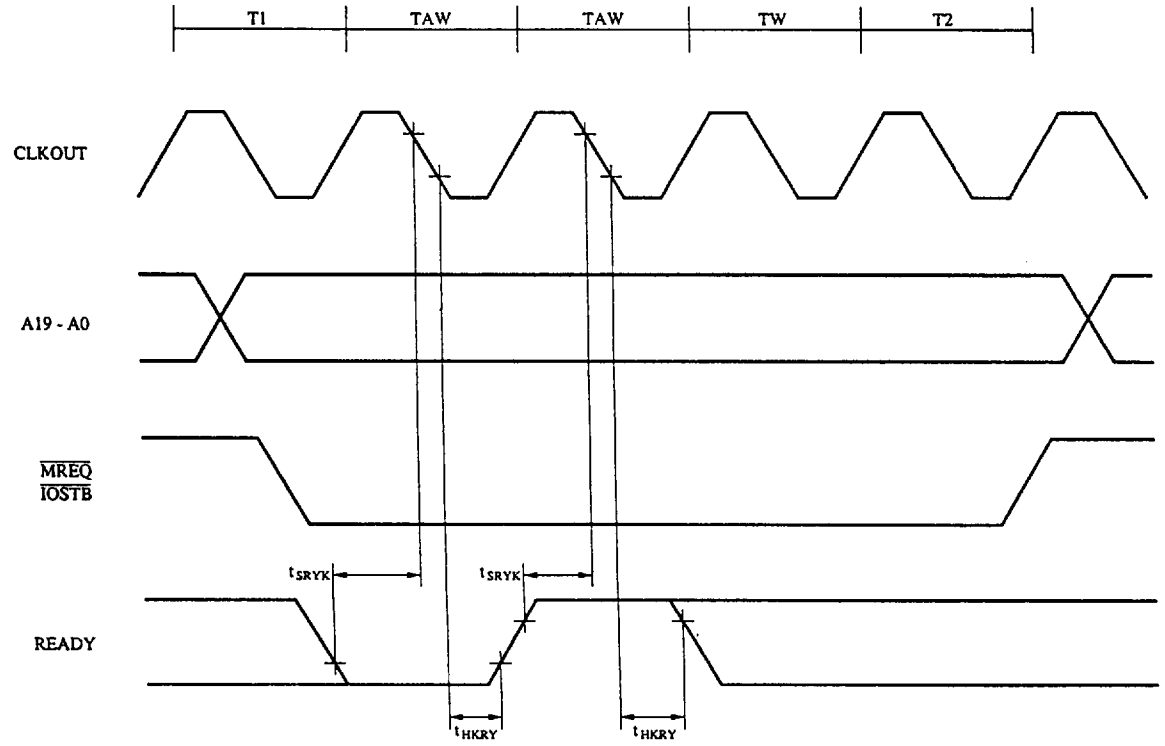
Parameter	Symbol	Test condition	MIN.	MAX.	Unit
Address delay time from CLKOUT	t_{DKD}		60	110	ns
Data input setup time	t_{SDK}		10		ns
Data input hold time	t_{HKD}		35		ns
$\overline{MREQ}$ delay time	t_{DKMR}		10	55	ns
$\overline{IOSTB}$ delay time	t_{DKIS}		10	55	ns
READY setup time	t_{SRYK}		15		ns
READY hold time	t_{HKRY}		40		ns

Ready Timing

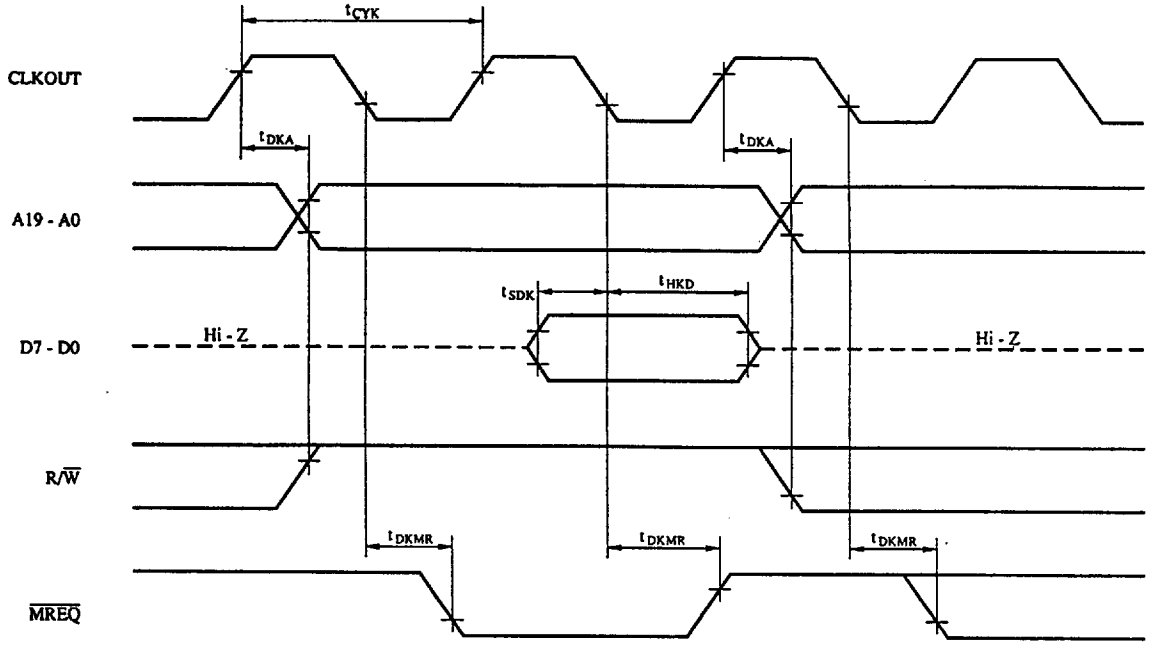
When 2 wait states are inserted:



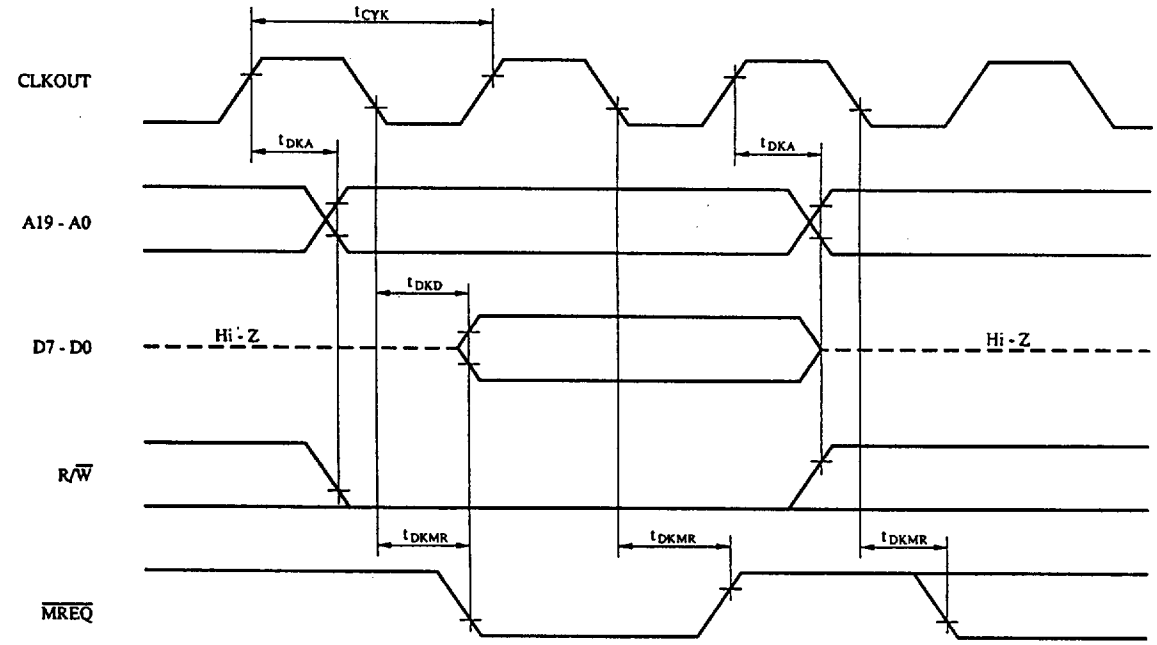
When an extra 1 wait stake is inserted:



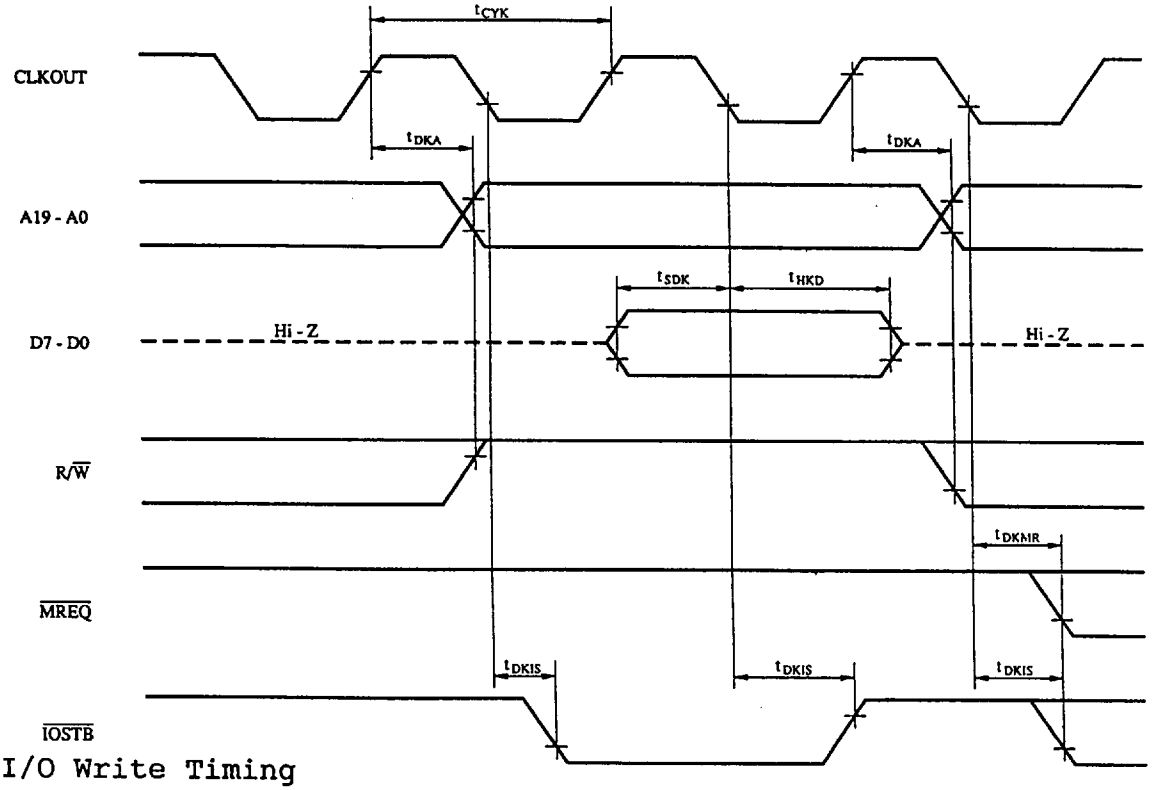
Memory Read Operation



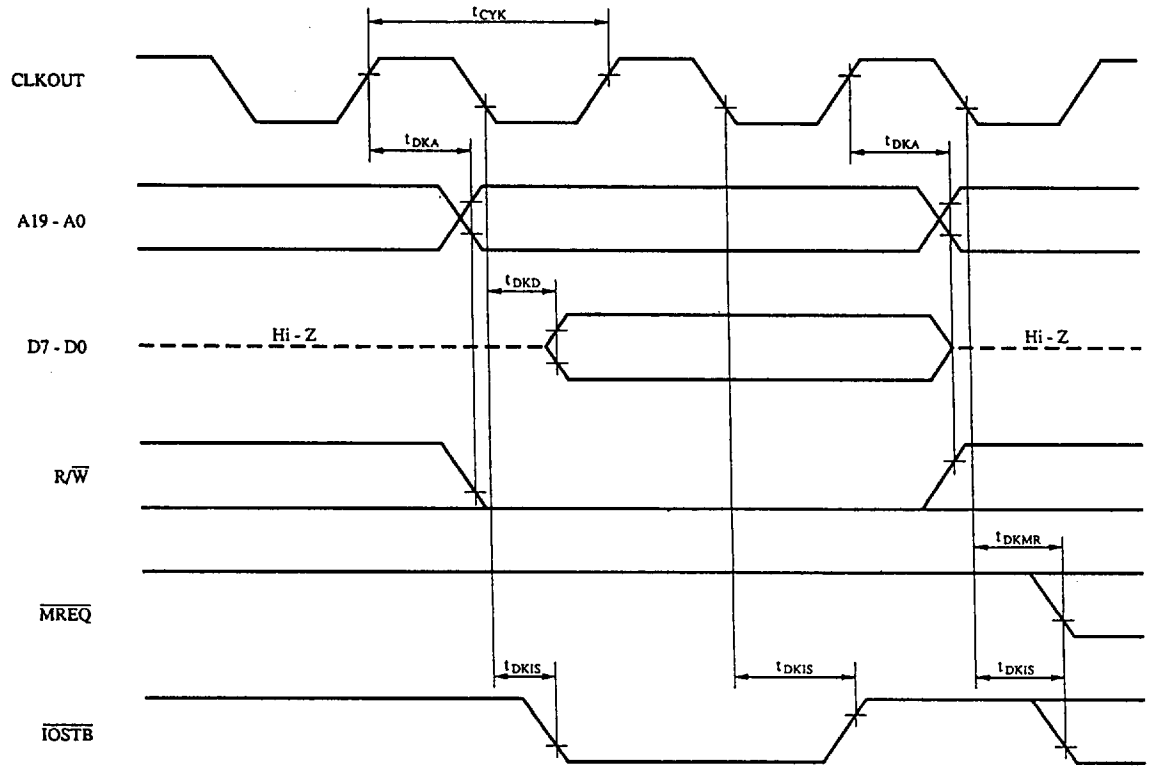
Memory Write Operation



I/O Read Timing

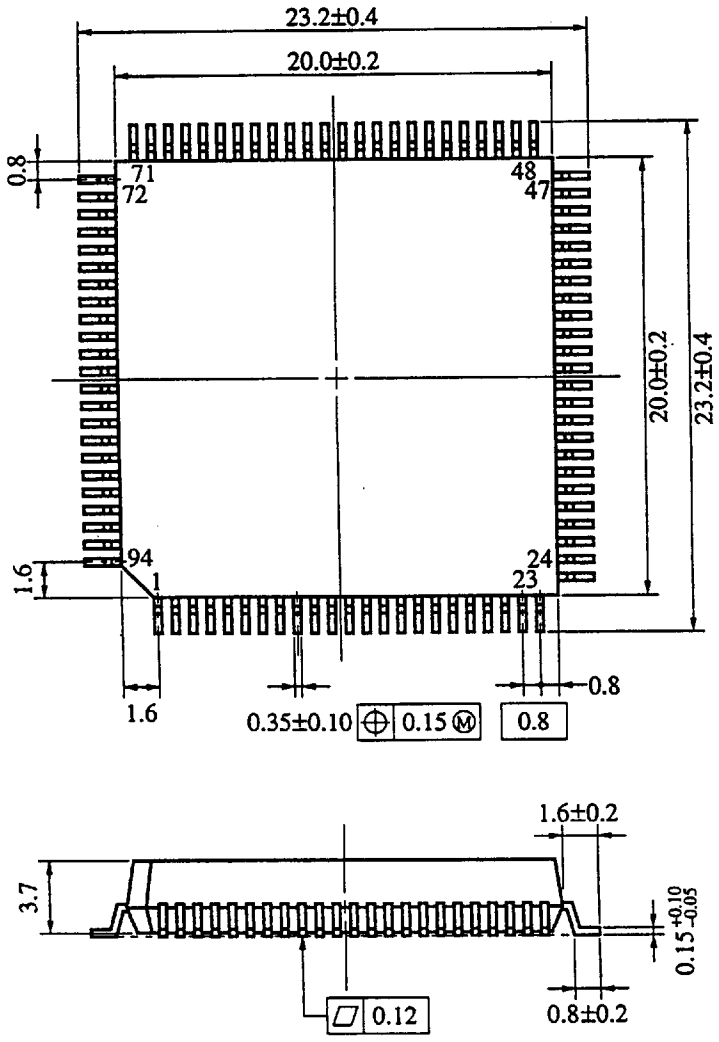


I/O Write Timing

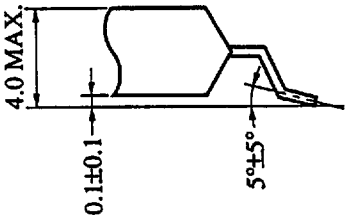


4. PACKAGE INFORMATION

94-pin Plastic QFP (□ 20) (Unit: mm)

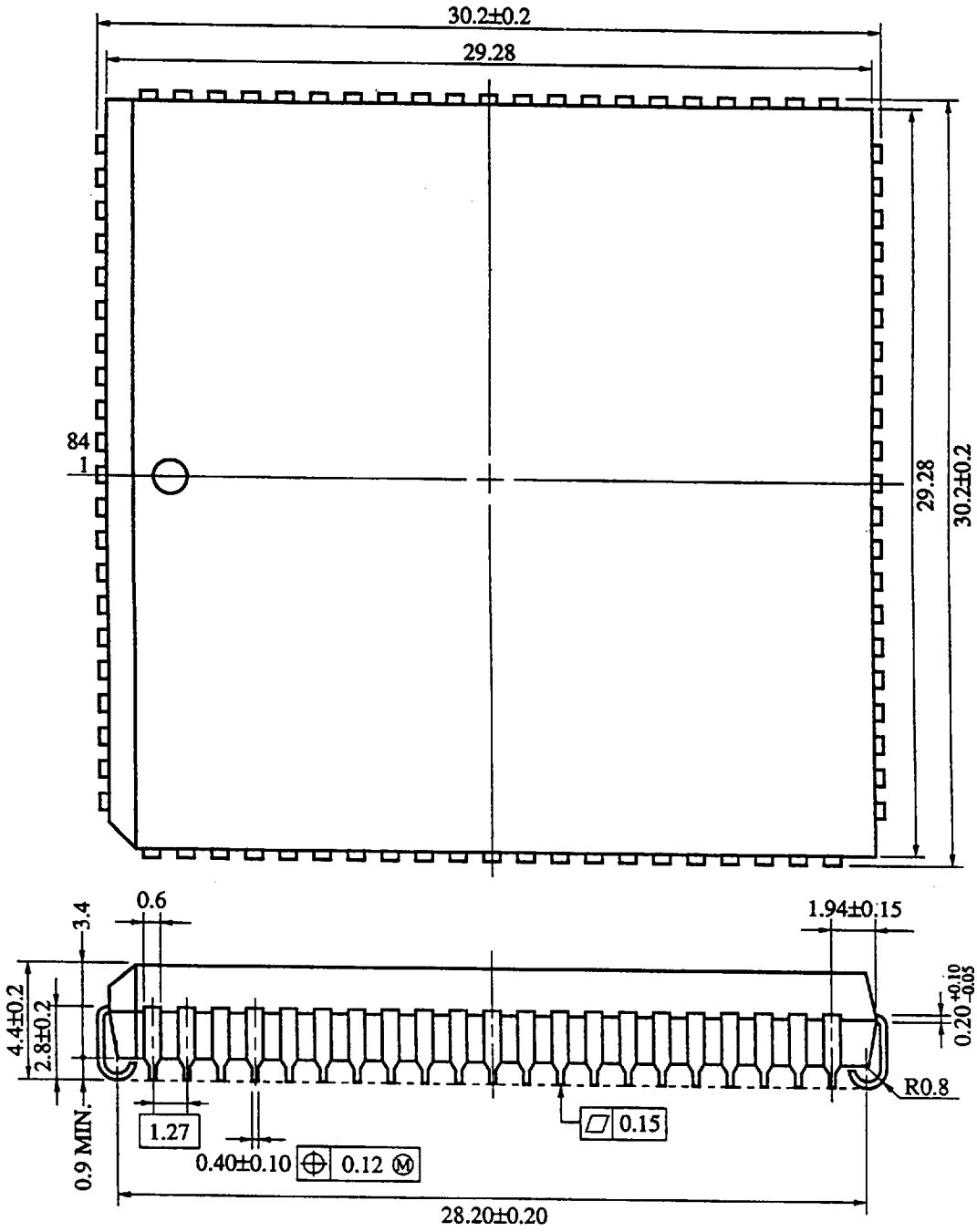


Detailed Drawing of Pin Tip Shape



S94GJ-80-5BG-2

84-Pin Plastic QFJ (□ 1150) (Unit: mm)



P84L-50A3-2