EPSON

SRM20V512SLMX7

512K-Bit Static RAM

Low Voltage Operation Products

- Wide Temperature Range
- Low Supply Current
- Access Time 70ns
- 65,536 words×8 bit Asynchronous

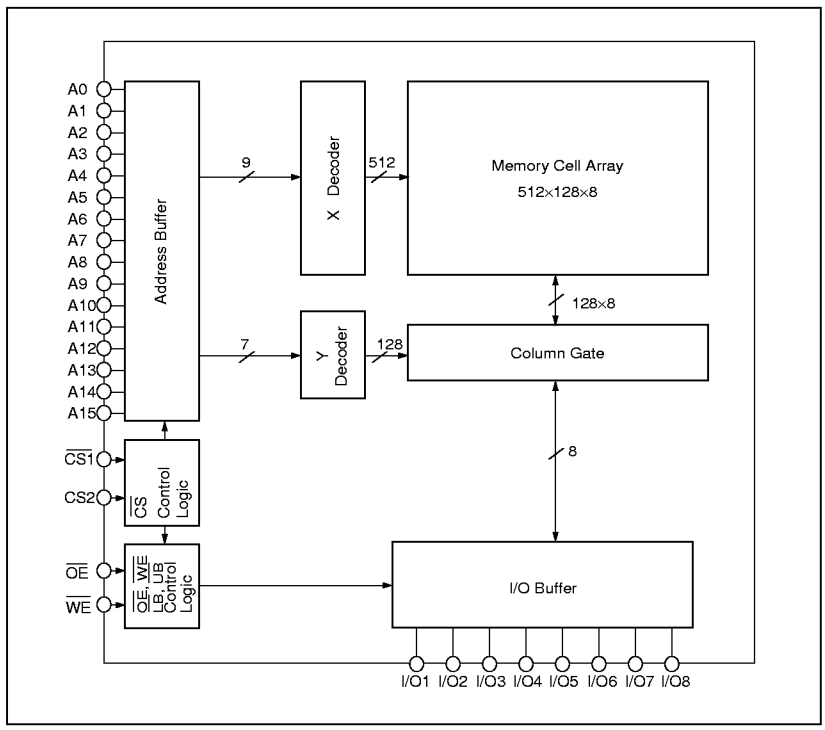
■ DESCRIPTION

The SRM20V512SLMX7 is a 65,536 words×8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. And –25 to +85°C operating tempereture range makes it ideal for portable equipment. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

■ FEATURES

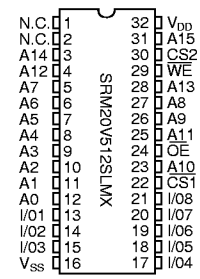
- Wide temperature range ..... –25 to 85°C
- Fast Access time SRM20V512SLMX7 70ns
- Low supply current ..... standby : 0.3µA (Typ.)
  operation :8mA/1MHz (Typ.)
- Completely static ..... No clock required
- Single power supply ..... 2.7V to 3.6V
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries.
- Package ..... SRM20V512SLMX7 SOP6-32pin (plastic)
  SRM20V512SLTX7 TSOP (I)-32pin (plastic)
  SRM20V512SLRX7 TSOP (I)-32pin-R1 (plastic)
  SRM20V512SLKX7 Slim-TSOP (I)-32pin (plastic)
  SRM20V512SLYX7 Slim-TSOP (I)-32pin-R1 (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

(SOP6)



(TSOP/Slim-TSOP)

(TSOP-R1/Slim-TSOP-R1)

■ PIN DESCRIPTION

A0 to A15	Address Input
WE	Write Enable
OE	Output Enable
CS1	Chip Select 1
CS2	Chip Select 2
I/O1 to 8	Data I/O
VDD	Power Supply (2.7V to 3.6V)
VSS	Power Supply (0V)
N. C.	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 4.6	V
Input voltage	V_I	–0.5* to V_{DD}+0.3	V
Input/Output voltage	$V_{I/O}$	–0.5* to V_{DD}+0.3	V
Power dissipation	P_D	0.5	W
Operating temperature	T_{opr}	–25 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

* V_I, $V_{I/O}$ (Min.) = –3.0V when Pulse width is less or equal 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

(Ta = –25 to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{DD}+0.3	V
	V_{IL}	–0.3*	—	0.4	V

* If pulse width is less than 50ns, it is –3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –25 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Input Leakage	I_{LI}	V_I = 0 to V_{DD}	–1	—	1	µA
Output teakage	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{IO} = 0 to V_{DD}	–1	—	1	µA
High level output voltage	V_{OH}	V_{DD}≥3V, I_{OH} = –2.0mA	2.4	—	—	V
		I_{OH}= –100µA	V_{DD}–0.2	—	—	
Low level output voltage	V_{OL}	V_{DD}≥3V, I_{OL} = –2.0mA	—	—	0.4	V
		I_{OL} = 100µA	—	—	0.2	
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	—	1.0	mA
	I_{DDS1}	$\overline{CS1}$ = CS2≥V_{DD}–0.2V or CS2≤0.2V	—	0.3	30	µA
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{cyc} = Min.	—	20	35	mA
	I_{DDA1}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{cyc} = 1us	—	8	15	mA
Operating supply current	I_{DDO}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA	—	8	15	mA

* Typical values are measured at Ta = 25°C and V_{DD} = 3.0V

● Terminal Capa citance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C_{ADD}	V_{ADD} = 0V	—	—	8	pF
Input Capacitance	C_I	V_I = 0V	—	—	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

Note ••• This parameter is made by the inspection data of sample, not of all products.

● AC Electrical Characteristics

❍ Read Cycle

(V_{SS} = 0V, V_{DD} = 2.7V to 3.6V, Ta = –25 to 85°C)

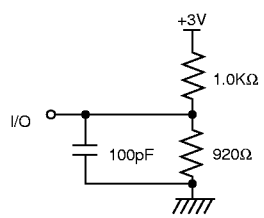
Parameter	Symbol	Conditions	SRM20V512SLMX7		Unit
			Min.	Max.	
Read cycle time	t_{RC}	1	70	—	ns
Address access time	t_{ACC}	1	—	70	ns
Chip select 1 access time	t_{ACS1}	1	—	70	ns
Chip select 2 access time	t_{ACS2}	1	—	70	ns
Output enable access time	t_{OE}	1	—	40	ns
Chip select 1 output set time	t_{CLZ1}	2	5	—	ns
Chip select 1 output floating	t_{CHZ1}	2	—	30	ns
Chip select 2 output set time	t_{CLZ2}	2	5	—	ns
Chip select 2 output floating	t_{CHZ2}	2	—	30	ns
Output enable output set time	t_{OLZ}	2	0	—	ns
Output enable output floating	t_{OHZ}	2	—	30	ns
Output hold time	t_{OH}	1	10	—	ns

❍ Write Cycle

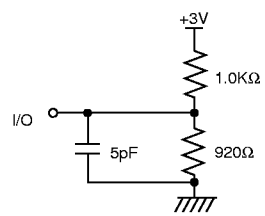
(V_{SS} = 0V, V_{DD} = 2.7V to 3.6V, Ta = –25 to 85°C)

Parameter	Symbol	Conditions	SRM20V512SLMX7		Unit
			Min.	Max.	
Write cycle time	t_{WC}	1	70	—	ns
Chip select time 1	t_{CW1}	1	60	—	ns
Chip select time 2	t_{CW2}	1	60	—	ns
Address enable time	t_{AW}	1	60	—	ns
Address setup time	t_{AS}	1	0	—	ns
Write pulse width	t_{WP}	1	55	—	ns
Address hold time	t_{WR}	1	0	—	ns
Input data setup time	t_{DW}	1	30	—	ns
Input data hold time	t_{DH}	1	0	—	ns
$\overline{WE}$ Output floating	t_{WHZ}	2	—	30	ns
WE Output setup time	t_{OW}	2	5	—	ns

*1 Test Conditions
1. Input pulse level : 0.4V to 2.4V
2. $t_r = t_f$ = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L = 100pF

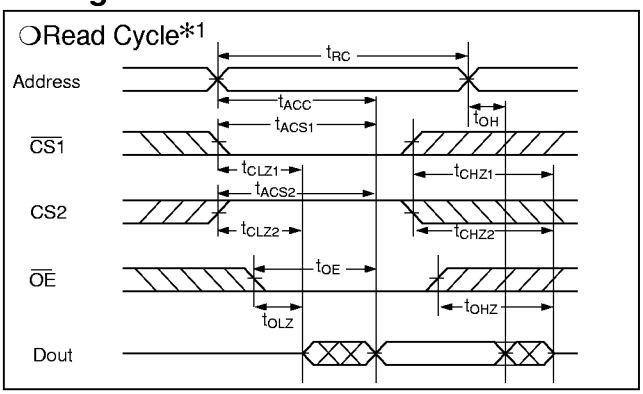


*2 Test Conditions
1. Input pulse level : 0.4V to 2.4V
2. $t_r = t_f$ = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels :
   ±200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF

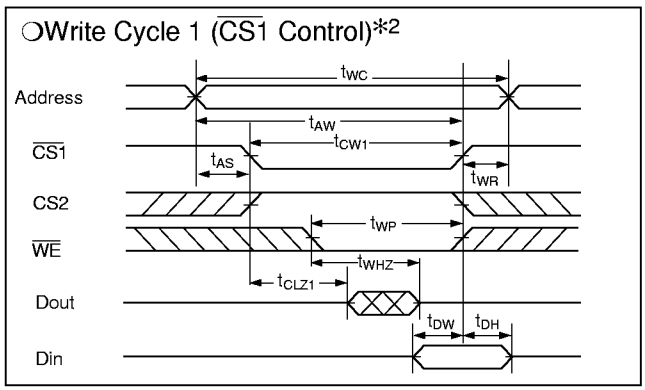


● Timing Chart

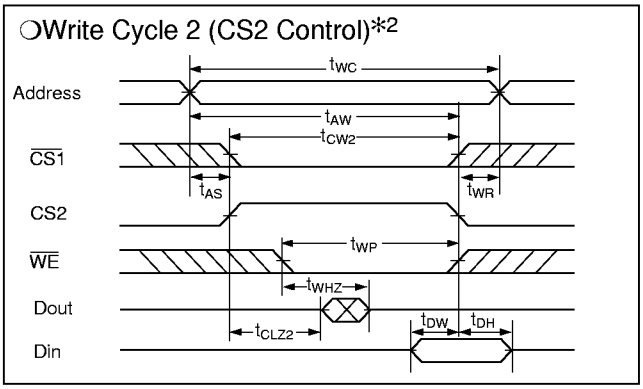
❍Read Cycle*1



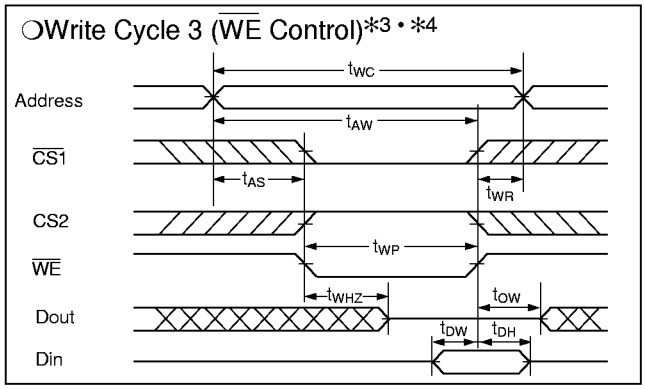
❍Write Cycle 1 (CS1 Control)*2



❍Write Cycle 2 (CS2 Control)*2



❍Write Cycle 3 (WE Control)*3 • *4



Note) *1 During read cycle time, WE is to be "H" level.

*2 During write cycle time that is controlled by CS1 or CS2, Input/output Buffer is in high impedance state whether OE level is "H" or "L".

*3 During write cycle time that is controlled by WE, Input/output Buffer is high impedance state if OE is "H" level.

*4 When I/O terminals are output mode, be careful that do not give the epposite signals to the I/O terminals.

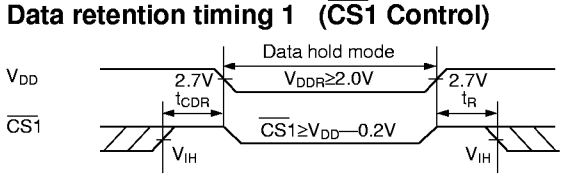
● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS} = 0V, Ta = –25 to 85°C)

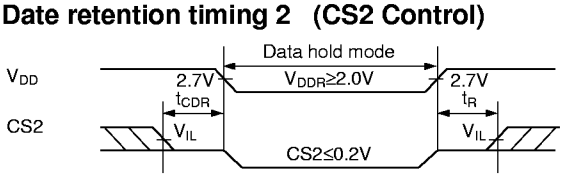
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDR}		2.0	—	3.6	V
Data retention current	I_{DDR}	V_{DD} = 2.7V CS1 = CS2≥V_{DD}0.2V or CS2≤0.2V	—	0.25	25	µA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		5	—	—	ms

* : Ta = 25°C

Data retention timing 1 (CS1 Control)



Date retention timing 2 (CS2 Control)



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DATA I/O	MODE	I_{DD}
H	X	X	X	Hi–Z	Unselected	I_{DDS}, I_{DDS1}
X	L	X	X	Hi–Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Input data	Write	I_{DDA}, I_{DDA1}
L	H	L	H	Ouput data	Read	I_{DDA}, I_{DDA1}
L	H	H	H	Hi–Z	Output disable	I_{DDA}, I_{DDA1}

X : "H" or "L"

● Reading data

Data is able to be read when the address is setted while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since Data I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing data

There are the following four ways of writing data into the memory.

(1) Hold CS2 = "H", $\overline{WE}$ = "L", set addresses and give "L" pulse to $\overline{CS1}$.

(2) Hold $\overline{CS1}$ = "L", $\overline{WE}$ = "L", set addresses and give "H" pulse to CS2.

(3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to $\overline{WE}$.

(4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

Anyway, data on the Data I/O terminals are latched up into the chip at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$ = "H" , or CS2 = " L" , the contention on the data bus can be avoided.

● Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level, the chip is in the standby mode which has retaning data operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When CS1 and $\overline{CS2}$ level are in the range over V_{DD}-0.2V, or CS2 level is in the range under 0.2V, in the chip there is almost no current flow except through the high resistance parts of the memory.

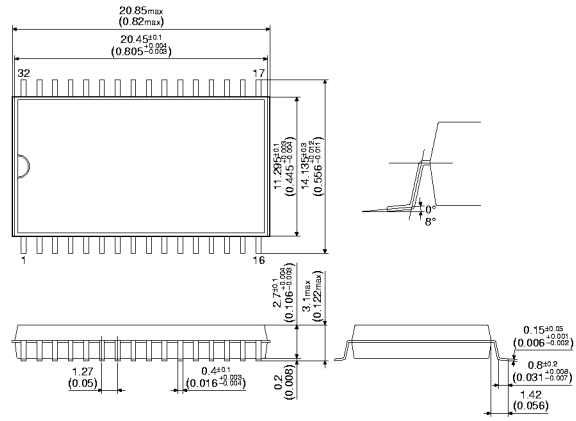
● Data Retention at low Voltage Power Supply

During standby mode in which the data is retentive, the supply voltage (V_{DD})can be in low voltage until V_{DD} = V_{DDR}.

At this mode data reading and writing are impossible.

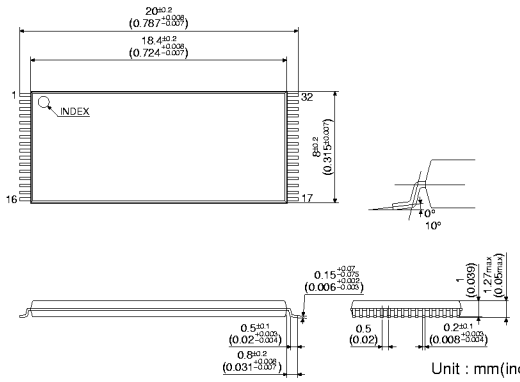
■ PACKAGE DIMENSIONS

Plastic SOP6-32pin



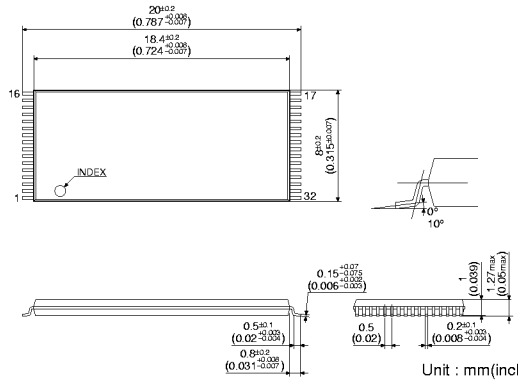
Unit : mm
(inch)

Plastic TSOP (I) -32pin



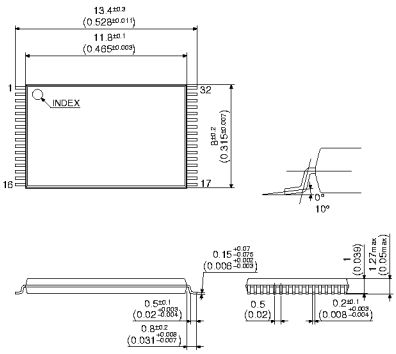
Unit : mm(inch)

Plastic TSOP (I) -32pin-R1



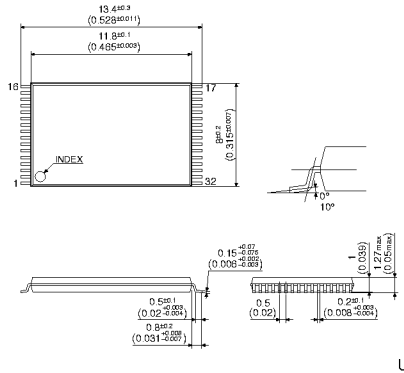
Unit : mm(inch)

Plastic Slim-TSOP (I) -32pin



Unit : mm(inch)

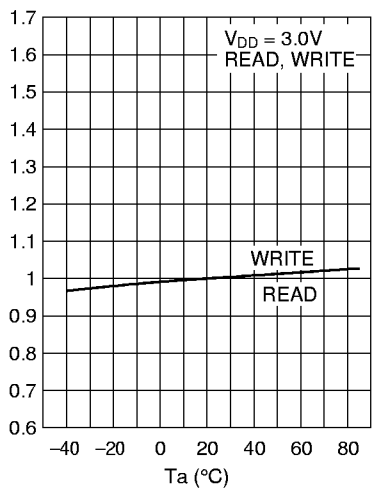
Plastic Slim-TSOP (I) -32pin-R1



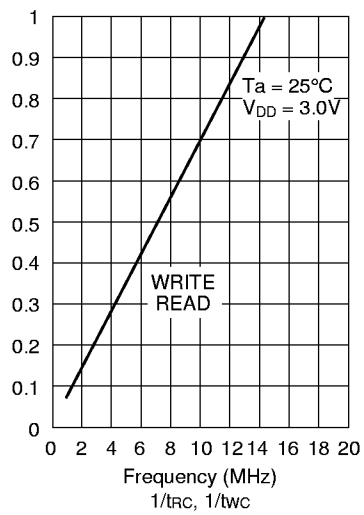
Unit : mm(inch)

■ CHARACTERISTICS CURVES

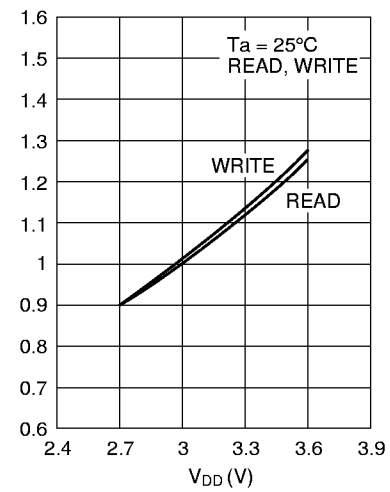
Normalized I_{DDA}–Ta



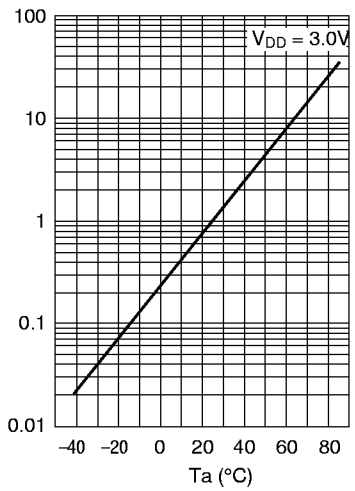
Normalized I_{DDA}–Frequency



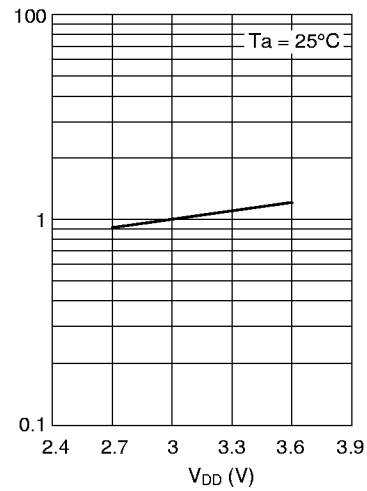
Normalized I_{DDA}–V_{DD}



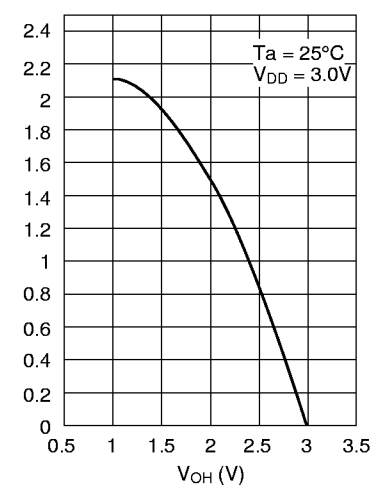
Normalized I_{DDS1}–Ta

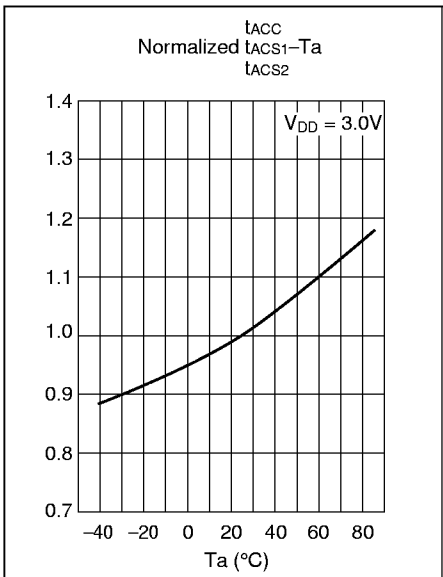


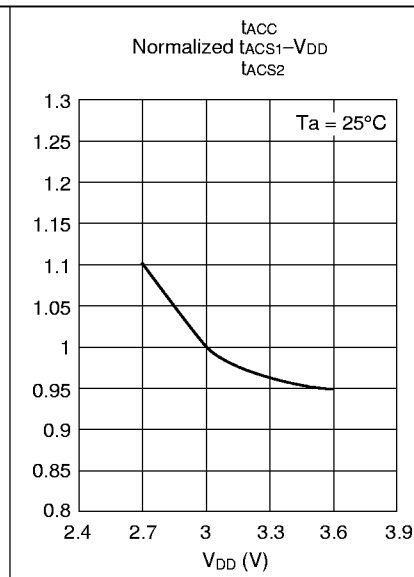
Normalized I_{DDS1}–V_{DD}

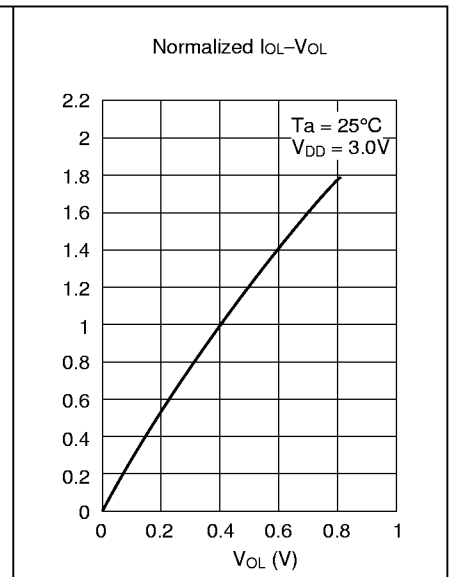


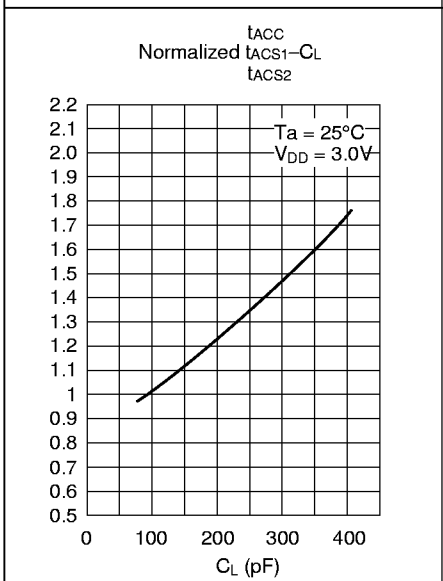
Normalized I_{OH}–V_{OH}

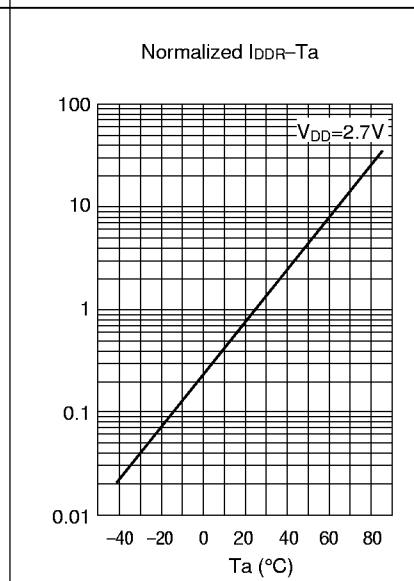



tACC
Normalized tACS1–Ta
tACS2
VDD = 3.0V
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
–40 –20 0 20 40 60 80
Ta (°C)


tACC
Normalized tACS1–VDD
tACS2
Ta = 25°C
1.3
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
2.4 2.7 3 3.3 3.6 3.9
VDD (V)


Normalized IOL–VOL
Ta = 25°C
VDD = 3.0V
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0 0.2 0.4 0.6 0.8 1
VOL (V)


tACC
Normalized tACS1–CL
tACS2
Ta = 25°C
VDD = 3.0V
2.2
2.1
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0 100 200 300 400
CL (pF)


Normalized IDDR–Ta
VDD=2.7V
100
10
1
0.1
0.01
–40 –20 0 20 40 60 80
Ta (°C)