Advanced Information
Datasheet

OV9665 Color CMOS SXGA (1.3 MegaPixel) CAMERACHIP™ Sensor with OmniPixel2™ Technology

General Description

The OV9665 CAMERACHIP™ image sensor is a low voltage CMOS device that provides the full functionality of a single-chip SXGA (1280x1024) camera and image processor in a small footprint package. The OV9665 provides full-frame, sub-sampled, scaled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) in SXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defect pixel canceling, noise canceling, and more, are also programmable through the SCCB interface. In addition, OmniVision sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable color image.

Note: The OV9665 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable applications
- Standard SCCB interface
- Supports image sizes: SXGA, VGA, CIF, scaled down and windowed outputs with Raw RGB, RGB565/555/444, YUV (4:2:2) and YCbCr (4:2:2) formats
- VarioPixel® method for sub-sampling
- Automatic image control functions including Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defect pixel canceling, noise canceling, and 50/60 Hz luminance detection

Ordering Information

Product	Package
OV09665-VL9A (Color, lead-free)	26-pin CSP2

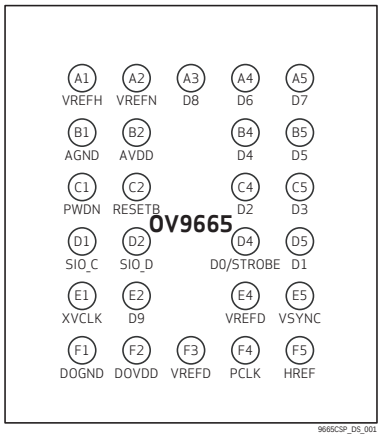
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

	Active Array Size	1304 x 1036
Power Supply	**Analog**	2.45 to 3.0VDC
	I/O	1.71V to 3.0V
Power Requirements	**Active**	80 mW typical (15fps)
	Standby	15 µA typical
Temperature Range	**Operation**	-30°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB565/555/444 • Raw RGB Data
	Lens Size	1/5.5"
	Chief Ray Angle	25° non-linear
Maximum Image Transfer Rate	**SXGA**	15 fps
	VGA and down scaling	30 fps
	Sensitivity	450 mV/(Lux • sec)
	S/N Ratio	40 dB
	Dynamic Range	55 dB
	Scan Mode	Progressive
	Maximum Exposure Interval	1052 x t_{ROW}
	Gamma Correction	Programmable
	Pixel Size	2.0 µm x 2.0 µm
	Dark Current	3 mV/sec @ 60°C
	Well Capacity	13 Ke
	Fixed Pattern Noise	1% of $V_{PEAK-TO-PEAK}$
	Image Area	2608 µm x 2072 µm
	Package Dimensions	4485 µm x 4985 µm

Figure 1 OV9665 Pin Diagram (Top View)[1]



[1] OV9665 pin diagram © 2008 OmniVision Technologies, Inc.

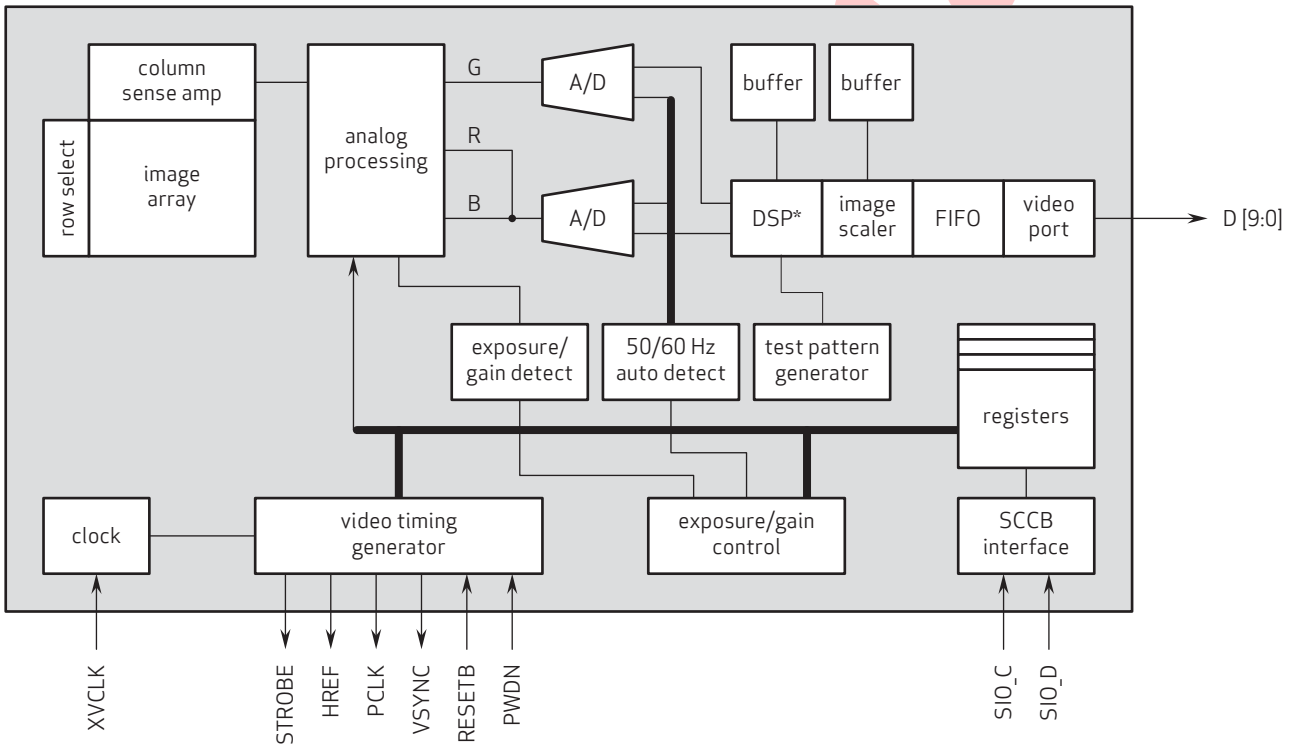
Version 1.1, October 10, 2007

Functional Description

Figure 2 shows the functional block diagram of the OV9665 image sensor. The OV9665 includes:

- Image Sensor Array (1304 x 1036 active image array)
- Analog Signal Processor
- A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram



note 1 DSP* (lens shading correction, de-noise, defect pixel correction, auto white balance, etc.)

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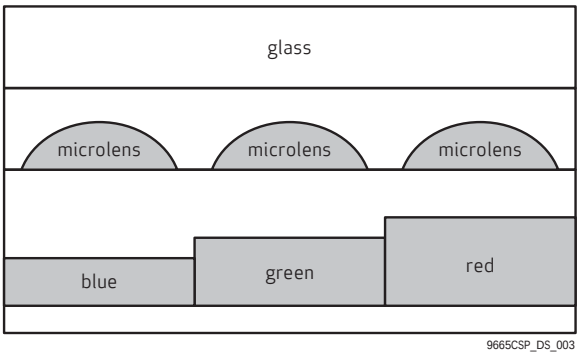
Image Sensor Array

The OV9665 sensor has an active image array of 1304 columns by 1036 rows (1,350,944 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs Automatic Gain Control (AGC).

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to two 10-bit analog-to-digital (A/D) converters, one for the G channel and one shared by the BR channels. These A/D converters operate at speeds up to 27 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Automatic White Balance (AWB)
- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit
- Defect pixel canceling
- De-noise

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Strobe Mode

The OV9665 has a Strobe mode that allows it to work with an external flash and LED.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description[1]

Table 1 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	VREFH	Reference	Internal analog voltage reference - connect to analog ground through a 0.1µF capacitor
A2	VREFN	Reference	Internal analog voltage reference - connect to analog ground through a 0.1µF capacitor
A3	D8	Output	Video output bit[8]
A4	D6	Output	Video output bit[6]
A5	D7	Output	Video output bit[7]
B1	AGND	Power	Ground for analog circuit
B2	AVDD	Power	Power for analog circuit
B4	D4	Output	Video output bit[4]
B5	D5	Output	Video output bit[5]
C1	PWDN	Input	Power down function (active high) with internal pull-down resistor
C2	RESETB	Input	Reset function (active low) with internal pull-up resistor
C4	D2	Output	Video output bit[2]
C5	D3	Output	Video output bit[3]
D1	SIO_C	Input	SCCB serial interface clock input without internal pull-up/pull-down resistor
D2	SIO_D	I/O	SCCB serial interface data I/O
D4	D0/STROBE	Output	Video output bit[0] when in 10-bit output mode or Strobe output when in 8-bit output mode.
D5	D1	Output	Video output bit[1]
E1	XVCLK	Input	System clock input without internal pull-up/pull-down resistor
E2	D9	Output	Video output bit[9]
E4	VREFD	Reference	Digital reference - connect to digital ground through a 0.1µF capacitor and connect with pin F3
E5	VSYNC	Output	Vertical sync output
F1	DOGND	Power	Ground for digital / video port
F2	DOVDD	Power	Power for digital / video port
F3	VREFD	Reference	Digital reference - connect to digital ground through a 0.1µF capacitor and connect to pin E4
F4	PCLK	Output	Pixel clock output
F5	HREF	Output	Horizontal reference output

NOTE:
D[9:2] for 8-bit YUV or RGB565/RGB555 (D[9] MSB, D[2] LSB)
D[9:0] for 10-bit Raw RGB data (D[9] MSB, D[0] LSB)

[1] OV9665 pin description list © 2008 OmniVision Technologies, Inc.

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+0.5V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – analog	–	2.45	2.8	3.0	V
V_{DD-IO}	DC supply voltage – I/O	–	1.71	1.8	3.0	V
I_{DDA}	Active (operating) current	See Note [a]		17 + 18[b]	50	mA
$I_{DDS-SCCB}$	Standby current	See Note [c]		1	2	mA
$I_{DDS-PWDN}$	Standby current			15	30	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V

a. At 25°C, V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V
$I_{DDA} = \Sigma\{I_{DD-A} + I_{DD-IO}\}$, f_{CLK} = 24MHz at 15 fps YCbCr output with typical loading

b. I_{DD-IO} = 17mA, I_{DD-A} = 18mA, with typical loading

c. At 25°C, V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

Table 4 Functional and AC Characteristics (-30°C < T_A < 70°C)

Symbol	Parameter		Min	Typ	Max	Unit
Functional Characteristics						
	A/D Differential non-linearity			± 1/2		LSB
	A/D Integral non-linearity			± 1		LSB
Inputs (PWDN, XVCLK and RESETB)						
f_{CLK}	Input clock frequency	With PLL	10	24	27	MHz
		Without PLL	10	24	54	MHz
$t_{CLK:DC}$	Clock duty cycle		45	50	55	%
$t_{S:RESETB}$	Setting time after software/hardware reset				1	ms
$t_{S:REG}$	Settling time for register change				300	ms
SCCB Timing (see Figure 4)						
f_{SIO_C}	Clock frequency				400	KHz
t_{LOW}	Clock low period		1.3			µs
t_{HIGH}	Clock high period		600			ns
t_{AA}	SIO_C low to data out valid		100		900	ns
t_{BUF}	Bus free time before new START		1.3			µs
$t_{HD:STA}$	START condition hold time		600			ns
$t_{SU:STA}$	START condition setup time		600			ns
$t_{HD:DAT}$	Data in hold time		0			µs
$t_{SU:DAT}$	Data in setup time		100			ns
$t_{SU:STO}$	STOP condition setup time		600			ns
t_{R}, t_{F}	SCCB rise/fall times				300	ns
t_{DH}	Data out hold time		50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0] (see Figure 5, Figure 6, and Figure 7)						
t_{PDV}	PCLK[↓] to data out valid				5	ns
t_{SU}	D[9:0] setup time		15			ns
t_{HD}	D[9:0] hold time		8			ns
t_{PHH}	PCLK[↓] to HREF[↑]		0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]		0		5	ns
AC Conditions:	• V_{DD}: V_{DD-A} = 2.8V, V_{DD-IO} = 1.8V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 20pF • f_{CLK}: 24MHz					

Timing Specifications

Note: Timing may vary depending on register settings.

Figure 4 SCCB Timing Diagram

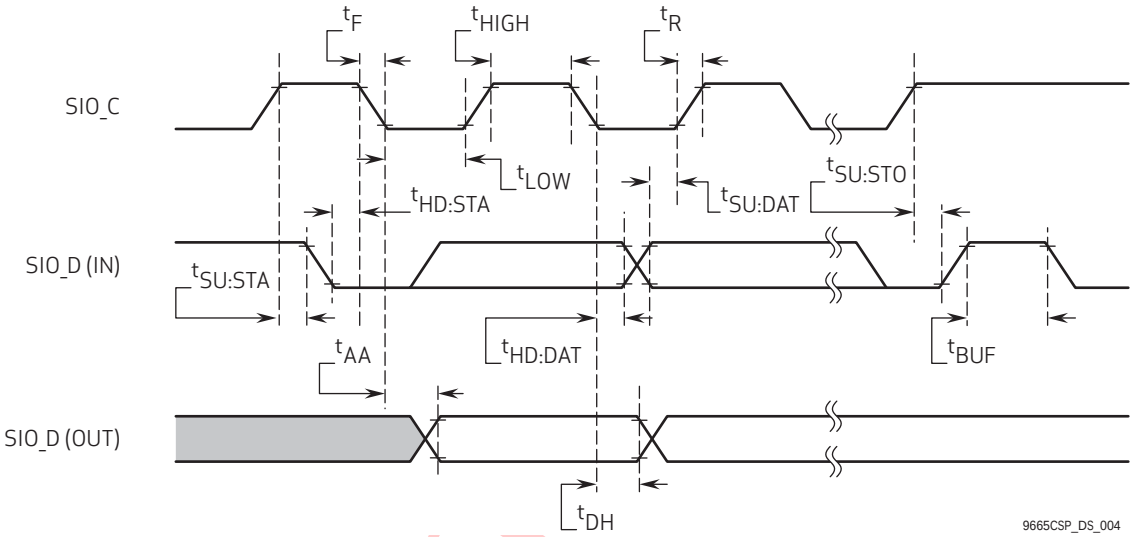


Figure 5 Horizontal Timing

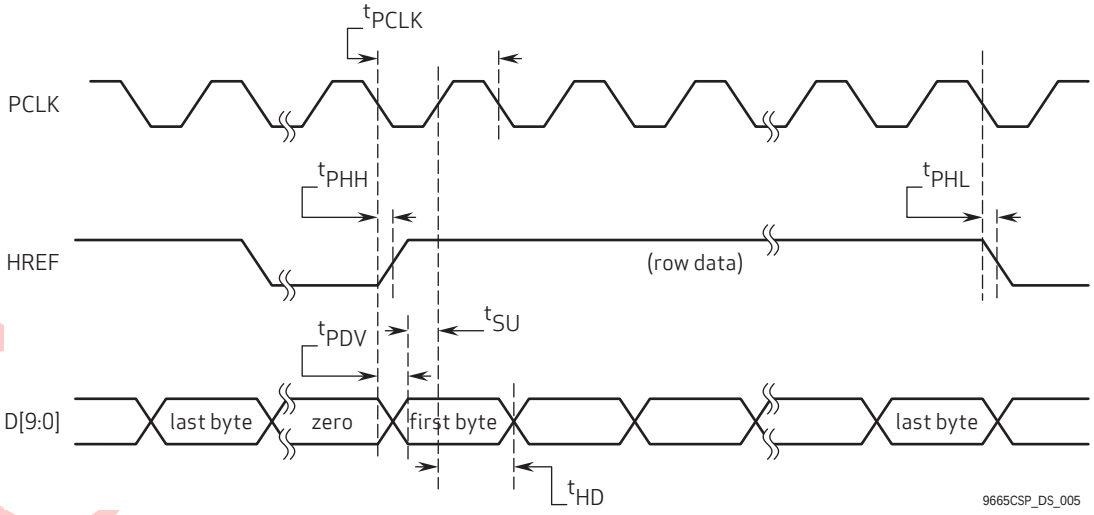
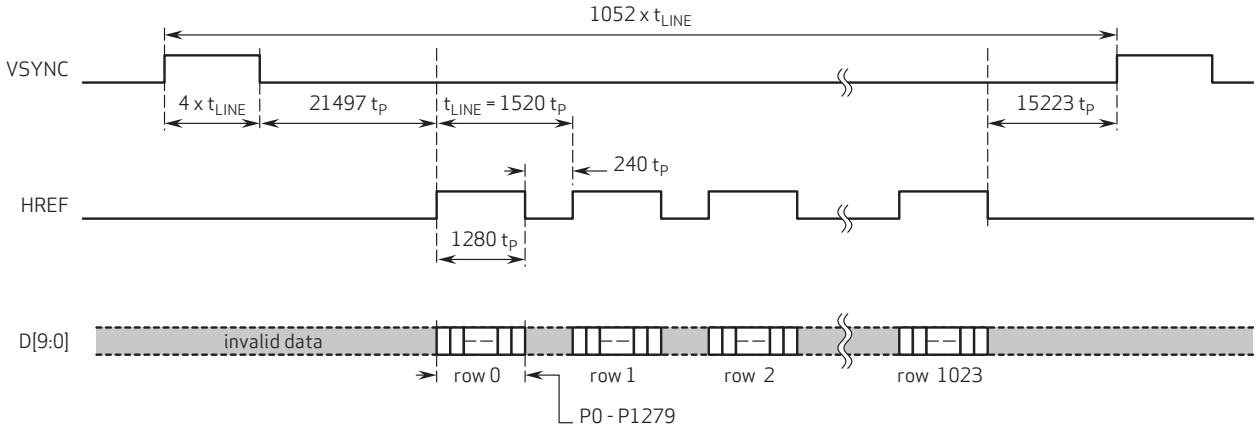


Figure 6 SXGA Frame Timing



note1 for raw data, t_P = internal pixel clock

note2 for YUV/RGB, t_P = 2 x internal pixel clock

note3 this timing diagram is for reference only; different settings will result in different timing values

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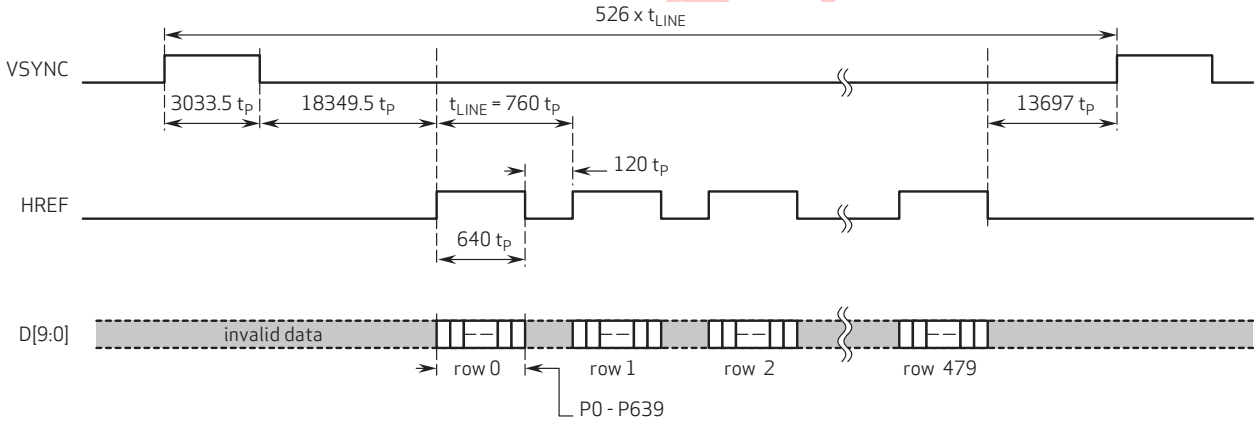
Figure 7 VGA 30 Frame Timing



note1 for raw data, t_P = internal pixel clock

note2 for YUV/RGB, t_P = 2 x internal pixel clock

note3 this timing diagram is for reference only; different settings will result in different timing values

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Figure 8 RGB 565 Output Timing Diagram

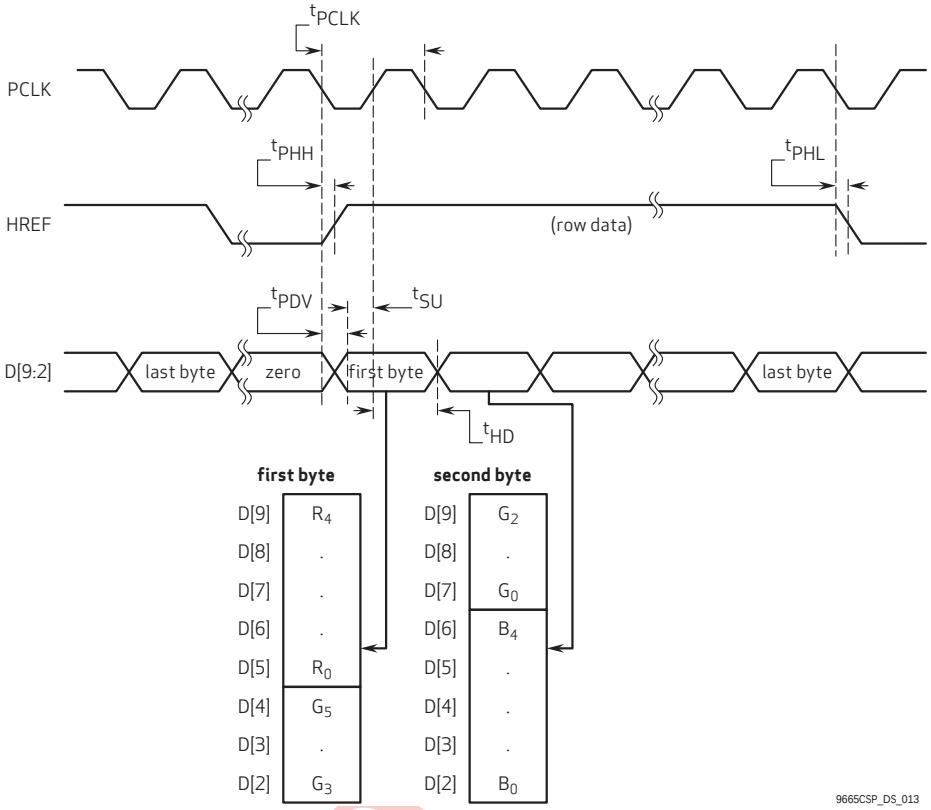


Figure 9 RGB 555 Output Timing Diagram

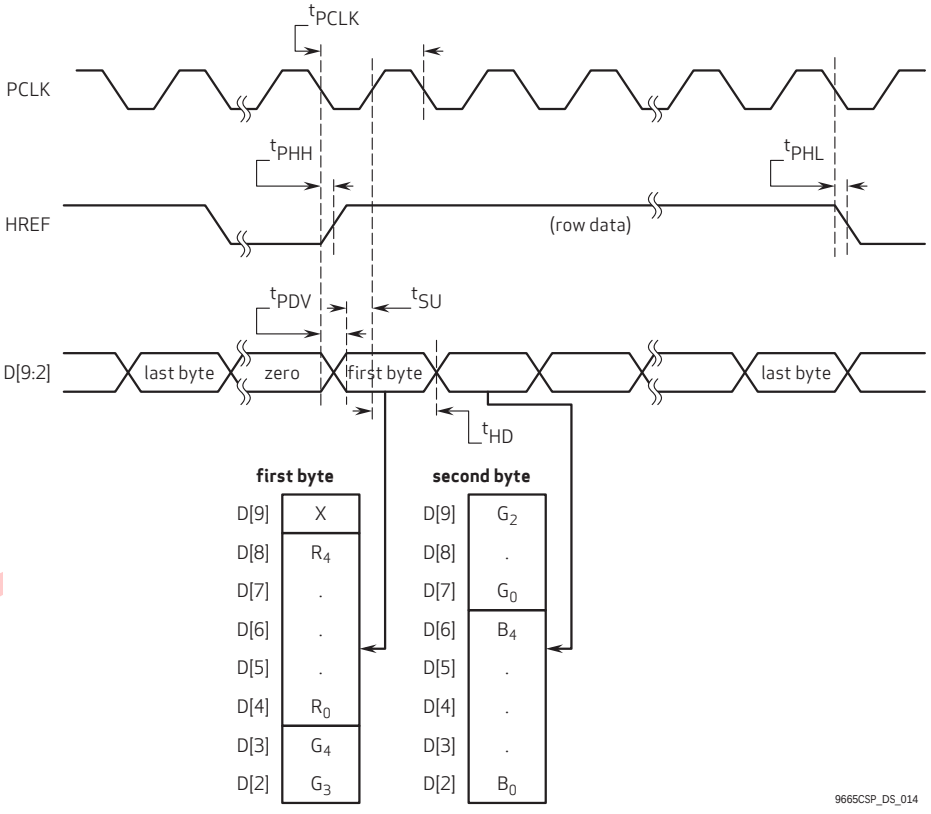
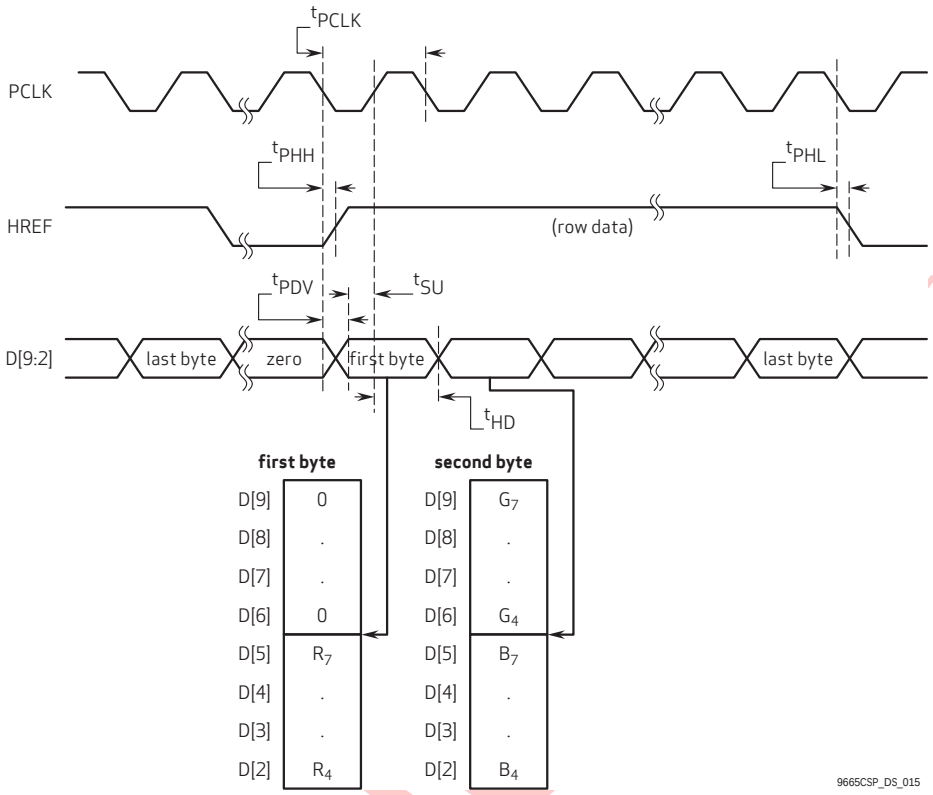


Figure 10 RGB 444 Output Timing Diagram



Register Table

Table 5 provides a list and description of the Device Control registers contained in the OV9665. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x60 for write and 0x61 for read.

Note: Reserved registers or register bits may be non-functional, special function or sensitive to the sensor. Please refer to OmniVision's recommended register settings.

Table 5 Device Control Register List (Sheet 1 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:0]: Gain setting • Range: 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0])/16) ***NOTE**: Set COM8[2] = 0 to disable AGC.*
01	BLUE	40	RW	Blue Gain Control
02	RED	40	RW	Blue Gain Control
03	COM1	03	RW	Common Control 1 Bit[7:6]: Dummy frame control - effective when register bit COM6[3] = 1 (0x0F) (night mode enable) 00: Not used 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs (see register VEND for 8 MSBs) Bit[1:0]: Vertical window start line control 2 LSBs (see register VSTRT for 8 MSBs)
04	REG04	28	RW	Register 04 Bit[7]: Horizontal mirror (effective when register bit REG33[3] = 1 (0x33) Bit[6]: Vertical flip Bit[5:2]: Reserved Bit[1:0]: AEC low 2 LSBs – AEC[1:0] (see register AEC for AEC[9:2] and register REG45[5:0] for AEC[15:10])
05	REG05	00	RW	Register 05 Bit[7:3]: Reserved Bit[2:0]: UV adjust slope[5:3] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG60[2:0] (0x60).

Table 5 Device Control Register List (Sheet 2 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
06	REG06	10	RW	Register 06 Bit[7:6]: Dummy line insertion beginning gain 00: 2x 01: 4x 10: 8x 11: 8x Bit[5:0]: Reserved
07	REG07	A4	RW	Register 07 Bit[7]: Reserved Bit[6:4]: VS start point Bit[3]: Reserved Bit[2:0]: VS width
08	RSVD	XX	–	Reserved
09	COM2	00	RW	Common Control 2 Bit[7:5]: Always precharge Bit[4]: Sleep mode enable (SCCB standby enable) 0: Normal mode 1: Sleep mode Bit[3]: Pin D0 output control 0: D0 1: STROBE Bit[2]: Reserved Bit[1:0]: Output drive current select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PID	96	R	Product ID Number MSB (Read only)
0B	VER	63	R	Product ID Number LSB (Read only)
0C	COM3	38	RW	Common Control 3 Bit[7:3]: Reserved Bit[2]: Manually set banding 0: 60 Hz 1: 50 Hz Bit[1]: Auto set banding Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	REG0D	80	RW	Register 0D Bit[7:5]: Reserved Bit[4]: DSP clock selection 0: For SXGA mode 1: For VGA 30 mode Bit[3:0]: Reserved

Table 5 Device Control Register List (Sheet 3 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0E	RSVD	XX	–	Reserved
0F	COM6	46	RW	Common Control 6 Bit[7:4]: Reserved Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2:0]: Reserved
10	AEC	00	RW	Automatic Exposure Control - AEC[9:2] (see register REG45[5:0] for AEC[15:10] and register REG04 for AEC[1:0]) AEC[15:0]: Exposure time TEX = tLINE x AEC[15:0] ***NOTE**: The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period*
11	CLKRC	80	RW	Clock Rate Control Bit[7:6]: Reserved Bit[5:0]: Clock divider for frame rate adjustment CLK = XVCLK / (decimal value of CLKRC[5:0] + 1)
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation Bit[6:5]: Resolution selection 00: SXGA (full size) mode 01: Not used 10: VGA mode 11: Not used Bit[4:3]: Reserved Bit[2]: Zoom mode Bit[1:0]: Reserved

Table 5 Device Control Register List (Sheet 4 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	E7	RW	Common Control 8 Bit[7]: Reserved Bit[6]: AEC step size limit Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s or 1/100s Bit[4:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	COM9	40	RW	Common Control 9 Bit[7:5]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: Not used 110: Not used 111: Not used Bit[4]: Reserved Bit[3]: Exposure time can be less than limitation of banding filter (1/120s or 1/100s) when light is too strong Bit[2]: Data output format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than the exposure gap Bit[0]: Reserved
15	COM10	00	RW	Common Control 10 Bit[7:6]: Reserved Bit[5]: PCLK output selection (works on row data output) 0: PCLK always output 1: PCLK output qualified by HREF Bit[4:2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: Reserved
16	GREEN	40	RW	Green Gain Control

Table 5 Device Control Register List (Sheet 5 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
17	HREFST	0D	RW	Horizontal Window Start 8 MSBs (3 LSBs in register REG32[2:0]) Bit[10:0]: Select beginning of horizontal window, each LSB represents two pixels
18	HREFEND	5D	RW	Horizontal Window End 8 MSBs (3 LSBs in register REG32[5:3]) Bit[10:0]: Select end of horizontal window, each LSB represents two pixels
19	VSTRT	01	RW	Vertical Window Line Start 8 MSBs (2 LSBs are in register COM1[1:0]) Bit[9:0]: Select start of vertical window, each LSB represents two scan lines
1A	VEND	82	RW	Vertical Window Line End 8 MSBs (2 LSBs are in register COM1[3:2]) Bit[9:0]: Select end of vertical window, each LSB represents two scan lines
1B	RSVD	XX	–	Reserved
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	REG1E	F9	RW	Register 1E Bit[7]: White defect pixel correction 0: Disable 1: Enable Bit[6]: Black defect pixel correction 0: Disable 1: Enable Bit[5:0]: Reserved
1F-23	RSVD	XX	–	Reserved
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC value decreases in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC value increases in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds (effective only in AEC/AGC fast mode) Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
27-29	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 6 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	REG2A	00	RW	Common Control 2A Bit[7:4]: Line interval adjustment value 4 MSBs (see register REG2B[7:0] for 8 MSBs) Bit[3:2]: HSYNC timing end point adjustment 2 MSBs (see register HEDY for 8 LSBs) Bit[1:0]: HSYNC timing start point adjustment 2 MSBs (see register HSDY for 8 LSBs)
2B	REG2B	00	RW	Common Control 2B Bit[7:0]: Line interval adjustment value 8 LSBs (see register REG2A[7:4] for 4 MSBs) The frame rate will be adjusted by changing the line interval. Each LSB will add 1/1520 Tframe in SXGA and 1/760 Tframe in VGA mode to the frame period.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width 8 LSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x tline. Each LSB count will add 1 x tline to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse Width 8 MSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x tline. Each MSB count will add 256 x tline to the VSYNC active period.
2F	YAVG	00	R	Luminance Average (this register will auto update)
30	HSDY	08	RW	HSYNC Position and Width Start 8 LSBs This register and register REG2A[1:0] define the HSYNC start position. Each LSB will shift the HSYNC starting point by a 2 pixel period.
31	HEDY	20	RW	HSYNC Position and Width End 8 LSBs This register and register REG2A[3:2] define the HSYNC end position. Each LSB will shift the HSYNC starting point by a 2 pixel period.
32	REG32	24	RW	Common Control 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position 3 LSBs (8 LSBs in register HREFEND) Bit[2:0]: Horizontal window start position 3 LSBs (8 LSBs in register HREFST)
33	REG33	C0	RW	Register 33 Bit[7:4]: Reserved Bit[3]: Mirror function (used with register bit REG04[7] (0x04)) Bit[2:0]: Reserved
34-35	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 7 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
36	REG36	94	RW	Register 36 Bit[7:6]: Reserved Bit[5]: Auto de-noise divider value 0: 128 1: 64 Bit[4:0]: Reserved
37-3A	RSVD	XX	–	Reserved
3B	REG3B	00	RW	Power Control 3B Bit[7:4]: Reserved Bit[3]: Bypass internal regulator 0: Use internal regulator to generate V_{DD-D} power 1: Bypass internal regulator (V_{DD-D} power needs to be provided by an external source) Bit[2:0]: Reserved
3C	RSVD	XX	–	Reserved
3D	REG3D	3C	RW	Common Control 3D Bit[7:6]: Reserved Bit[5:0]: PLL divider f_{CLK} = XCLK × (0x40 – REG3D[5:0]) / 8 / (CLKRC[5:0] + 1)
3E	REG3E	50	RW	Register 3E Bit[7]: PLL bypass option 0: Enable PLL 1: Bypass PLL Bit[6:0]: Reserved
3F-40	RSVD	XX	–	Reserved
41	REG41	00	RW	Register 41 Bit[7:5]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG5B[4:2] (0x5B). Bit[4:0]: Reserved
42	RSVD	XX	–	Reserved
43	REG43	00	RW	Register 43 Bit[7]: 9-zone average AEC option 0: Full size and VGA30 1: Other size Bit[6:0]: Reserved

Table 5 Device Control Register List (Sheet 8 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
44	REG44	00	RW	Register 44 Bit[7]: Reserved Bit[6]: Vertical line divider - works in scaling mode 0: No divider 1: Divider Bit[5:4]: Reserved Bit[3]: Vertical line divider number - works in scaling mode 0: Divide vertical line by 2 1: Divide vertical line by 4 Bit[2:0]: Reserved
45	REG45	00	RW	Register 45 Bit[7:6]: AGC[9:8], AGC highest gain control Bit[5:0]: AEC[15:10], AEC 6 MSBs (see register AEC for AEC[9:2] and register REG04 for AEC[1:0]).
46	FLL	00	RW	Frame Length Adjustment 8 LSBs Each bit will add 1 horizontal line timing in frame
47	FLH	00	RW	Frame Length Adjustment 8 MSBs Each bit will add 256 horizontal lines timing in frame
48-4A	RSVD	XX	–	Reserved
4B	COM22	00	RW	Common Control 22 Bit[7:0]: Flash light control
4C-4D	RSVD	XX	–	Reserved
4E	COM25	05	RW	Common Control 25 Bit[7:6]: 50 Hz banding AEC 2 MSBs Bit[5:4]: 60 Hz banding AEC 2 MSBs Bit[3:0]: Reserved
4F	BD50	9E	RW	50 Hz Banding AEC 8 LSBs (see register COM25[7:6] for 2 MSBs)
50	BD60	84	RW	60 Hz Banding AEC 8 LSBs (see register COM25[5:4] for 2 MSBs)
51-59	RSVD	XX	–	Reserved
5A	REG5A	57	RW	Register 5A Bit[7:4]: 50 Hz banding maximum AEC step Bit[3:0]: 60 Hz banding maximum AEC step
5B	REG5B	20	RW	Register 5B Bit[7:5]: Reserved Bit[4:2]: UV adjust offset value[5:3] between gain threshold 1 and gain threshold 2. For others, refer to register REG41[7:5] (0x41). Bit[1:0]: Reserved

Table 5 Device Control Register List (Sheet 9 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
5C	REG5C	00	RW	Register 5C Bit[7]: Average AEC option 0: 9-zone average AEC 1: Full average AEC Bit[6:0]: Reserved
5D	REG5D	55	RW	9-zone Average Weight Option - AVGsel[7:0]
5E	REG5E	55	RW	9-zone Average Weight Option - AVGsel[15:8]
5F	REG5F	21	RW	Register 5F Bit[7:2]: Reserved Bit[1:0]: 9-zone average weight option - AVGsel[17:16]
60	REG60	80	RW	Register 60 Bit[7:3]: Reserved Bit[2:0]: UV adjust slope[2:0] between gain threshold 1 and gain threshold 2. For others, refer to registers COM1[5:4] (0x03) and REG05[2:0] (0x05).
61	HISTO_LOW	80	RW	Histogram Algorithm Low Level Bit[7:0]: Histogram algorithm low level
62	HISTO_HIGH	90	RW	Histogram Algorithm High Level Bit[7:0]: Histogram algorithm high level
63	REG63	01	RW	Register 63 Bit[7:6]: Reserved Bit[5]: Raw data output format (valid when register REG07[1:0] is 2'b11) 0: DSP function (AWB and Gamma) works on Raw output data 1: DSP functions do not work on Raw output data Bit[4:0]: Reserved
64	REG64	20	RW	Register 64 Bit[7]: BLC line select 0: SXGA 1: Other resolution Bit[6:0]: Reserved
65	REG65	10	RW	Register 65 Bit[7:2]: Reserved Bit[1:0]: UV adjustment gain threshold 2 value[4:3]
66	REG66	00	RW	Register 66 Bit[7:5]: UV adjustment gain threshold 2 value[2:0] Bit[4:0]: Reserved
67-69	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 10 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6A	REG6A	24	RW	Register 6A Bit[7:5]: Reserved Bit[4]: FIFO manual option (works with scaling function) 0: Auto mode 1: Manual mode Bit[3:0]: Reserved
6B-74	RSVD	XX	–	Reserved
75	REG75	D0	RW	Histogram-based AEC Lower Limit of Probability - LPH
76	REG76	D0	RW	Histogram-based AEC Upper Limit of Probability - UPL
77	REG77	F0	RW	Histogram-based AEC Probability Threshold for LRL - TPL
78	REG78	90	RW	Histogram-based AEC Probability Threshold for HRL - TPH
79	REG79	E5	RW	Register 79 Bit[7:2]: High nibble of luminance thrreshold for AEC/AGC speed control Bit[3:0]: Low nibble of luminance threshold for AEC/AGC speed control
7A-7B	RSVD	XX	–	Reserved
7C	REG7C	05	RW	Register 7C Bit[7]: AEC option 0: Average-based AEC 1: Histogram-based AEC Bit[6:0]: Reserved
7D	REG7D	00	RW	Lens Correction Center Coordinates X Bit[7]: Sign bit Bit[6:0]: X-coordinate for lens correction center
7E	REG7E	00	RW	Lens Correction Center Coordinates Y Bit[7]: Sign bit Bit[6:0]: Y-coordinate for lens correction center
7F	REG7F	18	RW	Radius of the Circular Section Where Lens Correction Is Not Needed
80	REG80	04	RW	Lens Correction Blue Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
81	REG81	04	RW	Lens Correction Red Gain Parameter - this register is valid when register LC7[2] (0x83) = 1
82	REG82	04	RW	Lens correction Green Gain Parameter

Table 5 Device Control Register List (Sheet 11 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
83	LC7	06	RW	Bit[7:3]: Reserved Bit[2]: Lens correction control select 0: Use register REG82 (0x82) for gain parameter for R, G, and B channels 1: Use register REG82 (0x82) for green gain parameter, register REG80 (0x80) for blue gain parameter, and register REG81 (0x81) for red gain parameter Bit[1]: Reserved Bit[0]: Lens correction enable switch 0: Disable 1: Enable
84	REG84	86	RW	De-noise Level
85	REG85	E7	RW	Register 85 Bit[7:5]: Reserved Bit[4]: RAW/YUV (only works when register bits REGD7[1:0] (0xD7) = 0'b10) Bit[3]: FIFO enable (works with scaling function) Bit[2]: Gamma enable option 0: Disable 1: Enable Bit[1]: AWB gain Bit[0]: AWB
86-87	RSVD	XX	–	Reserved
88	REG08	A2	RW	Register 88 Bit[7:5]: AWB option 0: Advanced AWB 1: Simple AWB Bit[6:0]: Reserved
89-9A	RSVD	XX	–	Reserved
9B	GAM1	04	RW	Gamma Curve Segment 1 End Point
9C	GAM2	07	RW	Gamma Curve Segment 2 End Point
9D	GAM3	10	RW	Gamma Curve Segment 3 End Point
9E	GAM4	28	RW	Gamma Curve Segment 4 End Point
9F	GAM5	36	RW	Gamma Curve Segment 5 End Point
A0	GAM6	44	RW	Gamma Curve Segment 6 End Point
A1	GAM7	52	RW	Gamma Curve Segment 7 End Point
A2	GAM8	60	RW	Gamma Curve Segment 8 End Point
A3	GAM9	6C	RW	Gamma Curve Segment 9 End Point
A4	GAM10	78	RW	Gamma Curve Segment 10 End Point
A5	GAM11	8C	RW	Gamma Curve Segment 11 End Point

Table 5 Device Control Register List (Sheet 12 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
A6	GAM12	9E	RW	Gamma Curve Segment 12 End Point
A7	GAM13	BB	RW	Gamma Curve Segment 13 End Point
A8	GAM14	D2	RW	Gamma Curve Segment 14 End Point
A9	GAM15	E5	RW	Gamma Curve Segment 15 End Point
AA	SLOP	24	RW	Gamma Curve Segment 15 Slope
AB	REGAB	E7	RW	Register AB Bit[7:4]: Reserved Bit[3]: Scaling enable option 0: Disable 1: Enable Bit[2]: Sharpness enable option 0: Disable 1: Enable Bit[1]: De-noise enable option 0: Disable 1: Enable Bit[0]: Reserved
AC	REGAC	02	RW	De-noise Offset Limit in Auto De-noise Mode
AD	REGAD	25	RW	Register AD Bit[7:5]: Reserved Bit[4:0]: Sharpness value when GAIN < 2x
AE	REGAE	20	RW	Register AE Bit[7:3]: Reserved Bit[2]: Sharpness threshold double Bit[1:0]: Reserved
AF	RSVD	XX	–	Reserved
B0	REGB0	43	RW	Register B0 Bit[7]: Manual de-noise mode enable 0: Auto de-noise mode 1: Manual de-noise Bit[6:0]: Reserved
B1-B6	RSVD	XX	–	Reserved
B7	REGB7	00	RW	Register B7 Bit[7]: Scaling mode vertical output size bit[0] (11 bits total). For others, refer to registers REGB8[7:6] and REGBC Bit[6:4]: Scaling mode horizontal output size bit[2:1] (11 bits total). For others, refer to register REGBB Bit[3:0]: Reserved

Table 5 Device Control Register List (Sheet 13 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
B8	REGB8	00	RW	Register B8 Bit[7:6]: Scaling mode vertical output size bit[2:1] (11 bits total). For others, refer to registers REGB7[7] and REGBC Bit[5:3]: Scaling mode vertical input size bit[2:0] (11 bits total). For others, refer to register REGBA Bit[2:0]: Scaling mode horizontal input size bit[2:0] (11 bits total). For others, refer to register REGB9
B9	REGB9	A0	RW	Scaling Mode Horizontal Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[2:0]
BA	REGBA	80	RW	Scaling Mode Vertical Input Size bit[10:3] (11 bits total). For others, refer to register REGB8[5:3]
BB	REGBB	A0	RW	Scaling Mode Horizontal Output Size[10:3] (11 bits total). For others, refer to registers REGB8[7:6] and REGB7[6:4]
BC	REGBC	80	RW	Scaling Mode Vertical Output Size[10:3] (11 bits total). For others refer to registers REGB7[7] and REGB8[7:6]
BD	CMX1	05	RW	Color Matrix Parameter 1
BE	CMX2	16	RW	Color Matrix Parameter 2
BF	CMX3	05	RW	Color Matrix Parameter 3
C0	CMX4	07	RW	Color Matrix Parameter 4
C1	CMX5	18	RW	Color Matrix Parameter 5
C2	CMX6	1F	RW	Color Matrix Parameter 6
C3	CMX7	2B	RW	Color Matrix Parameter 7
C4	CMX8	2B	RW	Color Matrix Parameter 8
C5	CMX9	00	RW	Color Matrix Parameter 9
C6	CMX10	98	RW	Color Matrix Control 1 Bit[7]: Sign bit of CMX8 Bit[6]: Sign bit of CMX7 Bit[5]: Sign bit of CMX6 Bit[4]: Sign bit of CMX5 Bit[3]: Sign bit of CMX4 Bit[2]: Sign bit of CMX3 Bit[1]: Sign bit of CMX2 Bit[0]: Sign bit of CMX1

Y = (CMX1 × R + CMX2 × G + CMX3 × B) / 32

U = (CMX4 × R + CMX5 × G + CMX6 × B) / 32

V = (CMX7 × R + CMX8 × G + CMX9 × B) / 32

Table 5 Device Control Register List (Sheet 14 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
C7	CMX11	10	RW	Color Matrix Control 2 Bit[7]: Sign bit of CMX9 Bit[6]: Reserved Bit[5]: Auto UV adjustment enable 0: Disable 1: Enable Bit[4]: Special Digital Effects (SDE) enable 0: Disable 1: Enable Bit[3:0]: Reserved
C8	REGC8	02	RW	Register C8 Bit[7]: Fixed Y output value 0: Disable 1: Enable Bit[6]: Negative output 0: Disable 1: Enable Bit[5]: Gray scale output 0: Disable 1: Enable Bit[4]: Fixed V output value 0: Disable 1: Enable Bit[3]: Fixed U output value 0: Disable 1: Enable Bit[2]: Contrast function enable 0: Disable 1: Enable Bit[1]: Color saturation function enable 0: Disable 1: Enable Bit[0]: Hue adjustment enable 0: Disable 1: Enable
C9	REGC9	80	RW	Hue Adjustment Cosine Parameter
CA	REGCA	00	RW	Hue Adjustment Sine Parameter
CB	REGCB	40	RW	Saturation U Gain Value
CC	REGCC	40	RW	Saturation V Gain Value
CD	REGCD	80	RW	Fixed U Output Value
CE	REGCE	80	RW	Fixed V Output Value

Table 5 Device Control Register List (Sheet 15 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
CF	REGCF	00	RW	Y Offset Value Y' = [(Y + Yoffset) × Ygain] + Ybrightness when enabling contrast function
D0	REGD0	20	RW	Y Gain Value
D1	REGD1	00	RW	Y Brightness Value
D2	REGD2	00	RW	Register D2 Bit[7]: Auto UV adjustment enable Bit[6:5]: Reserved Bit[4:0]: UV adjust offset value after gain threshold 2
D3	REGD3	00	RW	FIFO Delay Timing Configuration (works with scaling function)
D4	RSVD	XX	–	Reserved
D5	REGD5	00	RW	IO Pad Direction Control Bit[7]: D7 direction control 0: Input 1: Output Bit[6]: D6 direction control 0: Input 1: Output Bit[5]: D5 direction control 0: Input 1: Output Bit[4]: D4 direction control 0: Input 1: Output Bit[3]: D3 direction control 0: Input 1: Output Bit[2]: D2 direction control 0: Input 1: Output Bit[1]: D1 direction control 0: Input 1: Output Bit[0]: D0 direction control 0: Input 1: Output
D6	REGD6	00	RW	Register D6 Bit[7:2]: Reserved Bit[1]: D9 direction control 0: Input 1: Output Bit[0]: D8 direction control 0: Input 1: Output

Table 5 Device Control Register List (Sheet 16 of 16)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
D7	REGD7	10	RW	Register D7 Bit[7:5]: Reserved Bit[4]: YU swap function 0: U Y V Y 1: Y U Y V Bit[3]: Data pins swap function (changes MSB to D0 and LSB to D9) - works in YUV mode 0: Disable 1: Enable Bit[2]: HREF to HSYNC 0: Output HREF signal 1: Output HSYNC signal Bit[1:0]: Data output format selection 00: YUV output 01: RGB output 10: ISP RAW output 11: RAW output
D8	REGD8	C4	RW	Register D8 Bit[7:6]: Reserved Bit[5]: HREF/HSYNC negative output 0: Positive output 1: Negative output Bit[4]: Reserved Bit[3]: CCIR656 output selection 0: Disable 1: Enable Bit[2]: Reserved Bit[1:0]: RGB data output format selection (effective when register bits REGD7[1:0] = 01) 00: Not used 01: RGB565 10: RGB555 11: RGB444
D9	REGD9	64	RW	Register D9 Bit[7:4]: Sharpness value when 4x < GAIN < 8x Bit[3:0]: Sharpness value when 2x < GAIN < 4x
DA	REGDA	86	RW	Register DA Bit[7:4]: Sharpness value when 16x < GAIN Bit[3:0]: Sharpness value when 8x < GAIN < 16x
DB-DE	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV9665 uses a 26-pin Chip Scale Package 2 (CSP2). Refer to Figure 11 for package information, Table 6 for package dimensions and Figure 12 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 11 OV9665 Package Specifications

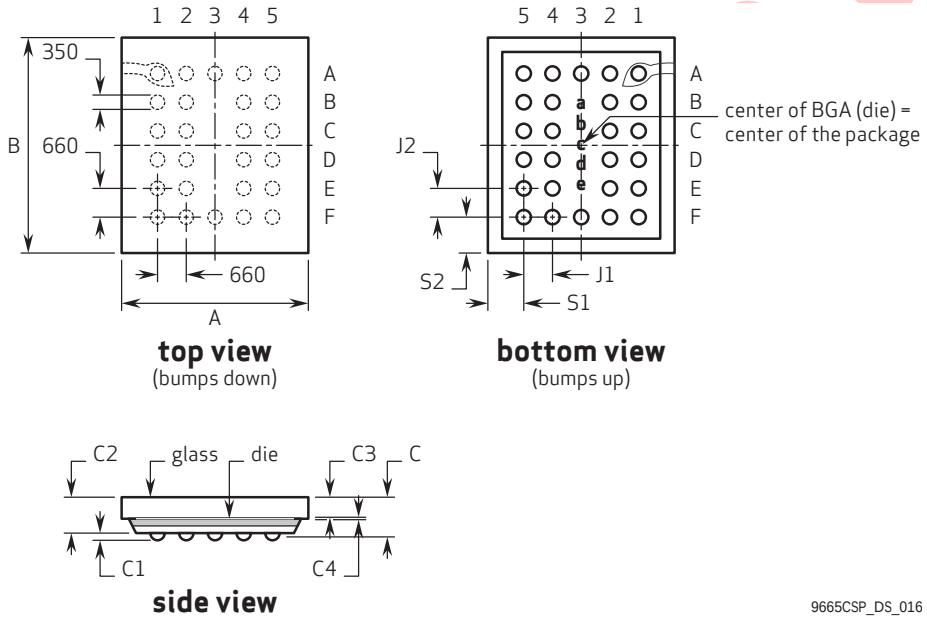
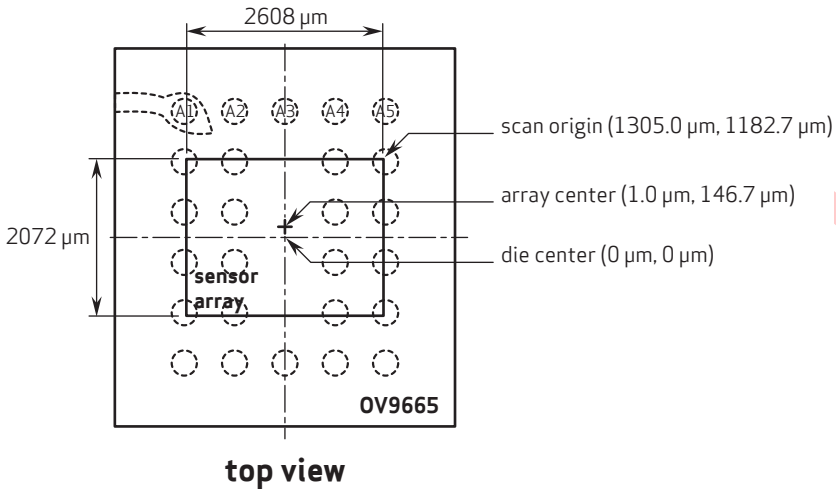


Table 6 CSP Package Dimensions

Parameter	Symbol	Min	Nominal	Max	Unit
Package body dimension X	A	4460	4485	4510	µm
Package body dimension Y	B	4960	4985	5010	µm
Package height	C	845	905	965	µm
Ball height	C1	150	180	210	µm
Package body thickness	C2	680	725	770	µm
Cover glass thickness	C3	375	400	425	µm
Airgap between cover glass and sensor	C4	30	45	60	µm
Ball diameter	D	320	350	380	µm
Total pin count	N		26		
Pin count X-axis	N1		5		
Pin count Y-axis	N2		6		
Pins pitch X-axis	J1		660		µm
Pins pitch Y-axis	J2		660		µm
Edge-to-pin center distance analog X	S1	893	923	953	µm
Edge-to-pin center distance analog Y	S2	813	843	873	µm

Sensor Array Center

Figure 12 OV9665 Sensor Array Center



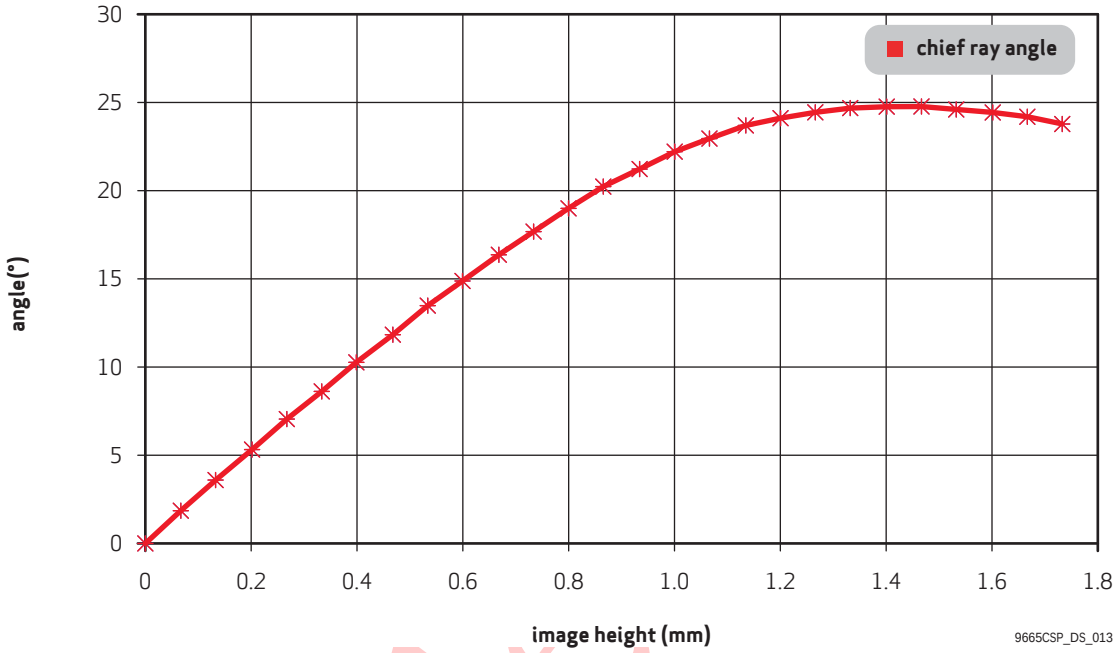
note1 this drawing is not to scale and is for reference only.

note2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

9665CSP_DS_012

Chief Ray Angle

Figure 13 OV9665 Chief Ray Angle



IR Reflow Ramp Rate Requirements

OV9665 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case.

Figure 14 IR Reflow Ramp Rate Requirements

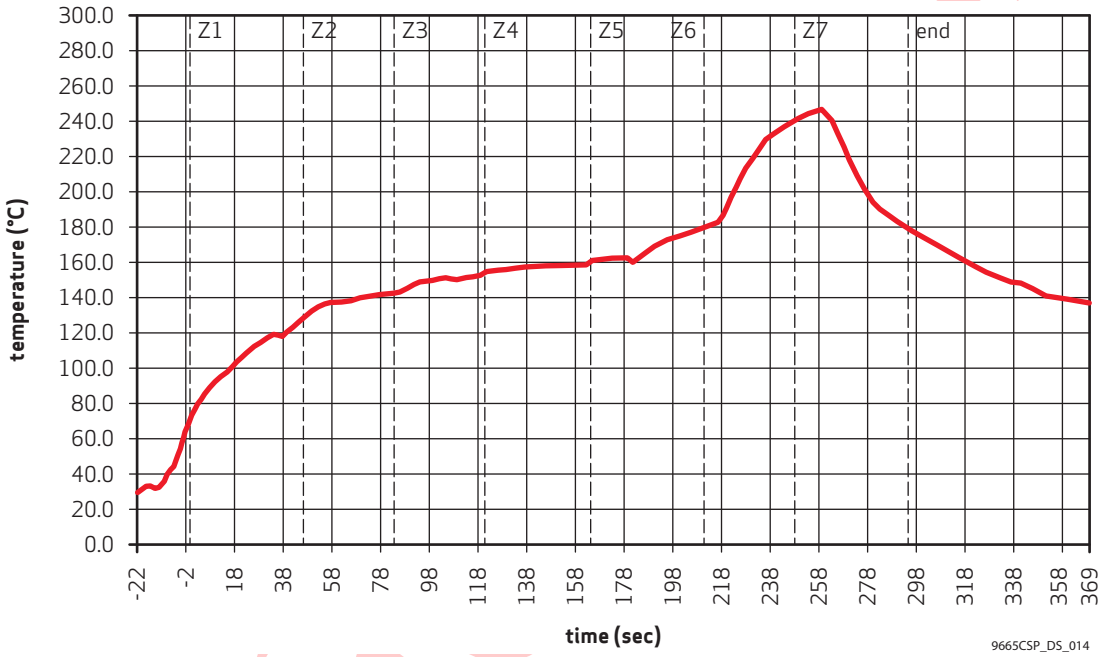


Table 7 Reflow Conditions

Condition	Exposure
Average ramp-up rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak temperature	245°C
Cool-down rate (peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV9665 (CSP2) Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release

REVISION CHANGE LIST

Document Title: OV9665 (CSP2) Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- In Figure 6 on page 7, changed timing between falling edge of HREF and rising edge of VSYNC from 13716 tp to 15223 tp
- In Figure 7 on page 7, changed timing between falling edge of HREF and rising edge of VSYNC from 13679 tp to 13697 tp
- In Table 5 on page 12, changed Register Name, Default value, and R/W type of register 0x0D from “RSVD”, “XX”, and “–” to “REG0D”, “80”, and “RW”, respectively
- In Table 5 on page 12, changed description of register 0x0D from “Reserved” to:

  Register 0D

  Bit[7:5]: Reserved

  Bit[4]: DSP clock selection

  0: For SXGA mode

  1: For VGA 30 mode

  Bit[3:0]: Reserved