

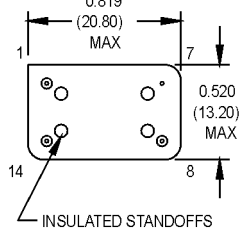
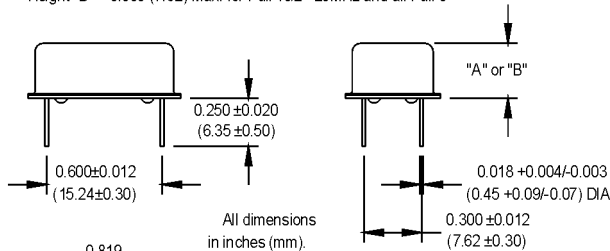
MV Series

14 DIP, 5.0 Volt, HCMOS/TTL, VCXO

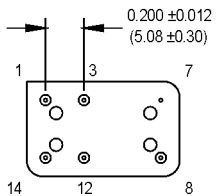


- General purpose VCXO for Phase Lock Loops (PLLs), Clock Recovery, Reference Signal Tracking, and Synthesizers
- Frequencies up to 160 MHz
- Tri-state Option Available

Height "A" = 0.200 (5.08) Max. for Pull 1&2 < 25 MHz
 Height "B" = 0.300 (7.62) Max. for Pull 1&2 > 25MHz and all Pull 3



OPTIONAL 6-PIN PACKAGE WITH TRISTATE



Pin Connections

PIN	FUNCTION
1	Control Voltage
3	Tristate (6-Pin Pkg. Only)
7	Ground
8	Output
12	N/C (6-Pin Pkg. Only)
14	+Vdd

Ordering Information

Product Series	MV	1	3	V	2	C	D	-R	00.0000
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C							
Stability	1: ±1000 ppm	2: ±500 ppm	3: ±100 ppm						
Output Type	V: Voltage Controlled	T: Tristate							
Pull Range (Vc = .5 to 4.5V)	1: ±50 ppm min.	2: ±100 ppm min.							
Symmetry/Logic Compatibility	A: 40/60 CMOS/TTL	C: 45/55 HCMOS							
Package/Lead Configurations	D: DIP; Nickel Header	G: Gull Wing; Nickel Header							
RoHS Compliance	Blank: non-RoHS compliant part	-R: RoHS compliant part							
Frequency (customer specified)									

*Contact factory for availability

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	1.5		160	MHz	See Note 1
Operating Temperature	T _A	(See Ordering Information)				
Storage Temperature	T _S	-55		125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						
1st Year		0.6		0.6	ppm	< 52 MHz / ≥ 52 MHz
Thereafter (per year)		0.5		0.5	ppm	< 52 MHz / ≥ 52 MHz
Pullability/APR		(See Ordering Information)				
Control Voltage	V _c	0.5	2.5	4.5	V	Over control voltage
Linearity				10	%	Positive Monotonic Slope
Modulation Bandwidth	f _m	10			kHz	
Input Impedance	Z _{in}	50k			Ohms	
Input Voltage	V _{dd}	4.75	5	5.25	V	
Input Current	I _{dd}		25	40	mA	1.5 to 24.999 MHz
			35	60	mA	25 to 69.999 MHz
			55	90	mA	70 to 160 MHz
Output Type						HCMOS/TTL
Load						See Note 2
						10 TTL or 50 pF
						5 TTL or 15 pF
Symmetry (Duty Cycle)		(See Ordering Information)				
Logic "1" Level	V _{oh}	90% V _{dd}			V	HCMOS load
		V _{dd} - 0.5			V	TTL load
Logic "0" Level	V _{ol}			10% V _{dd}	V	HCMOS load
				0.5	V	TTL load
Rise/Fall Time	T _r /T _f				ns	See Note 4
1.5 to 54.999 MHz				6 / 10	ns	TTL/HCMOS
55 to 160 MHz				1.5 / 5	ns	TTL/HCMOS
Tri-state Function		Input Logic "1" or floating: output active				
		Input Logic "0": output disables to high-Z				
Start up Time			5		ms	
Phase Jitter	φ _J					
@ 38.88 MHz			0.3	1	ps RMS	Integrated 12 kHz - 20 MHz
@ 155.52 MHz			10	15	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)						Offset from carrier
10 Hz		100 Hz	1 kHz	10 kHz	100 kHz	
@ 38.88 MHz	-71	-104	-134	-151	-153	
@ 155.52 MHz	-62	-93	-113	-115	-114	

1. Frequencies above 90 MHz utilize a PPL design. Fundamental and PLL designs are available for other frequencies. Contact factory.
2. TTL load – see load circuit diagram #1. HCMOS load – see load circuit diagram #2
3. Symmetry is measured at 1.4 V with TTL load, and at 50% with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% V_{dd} and 90% V_{dd} for HCMOS load.

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