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LR490302 Digital Signal Processor for MODEM

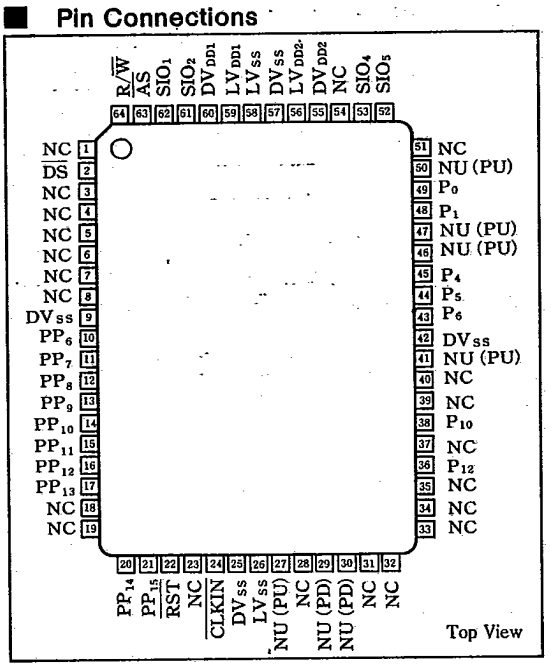
Description

The LR490302 is a digital signal processor IC which provides functions necessary for the MODEM. Used in combination with the analog/digital interface IC (LR4906), it is possible to compose a MODEM sistem for G Ⅱ/G Ⅲ facsimile such as V29, V27ter, V21-2, etc.

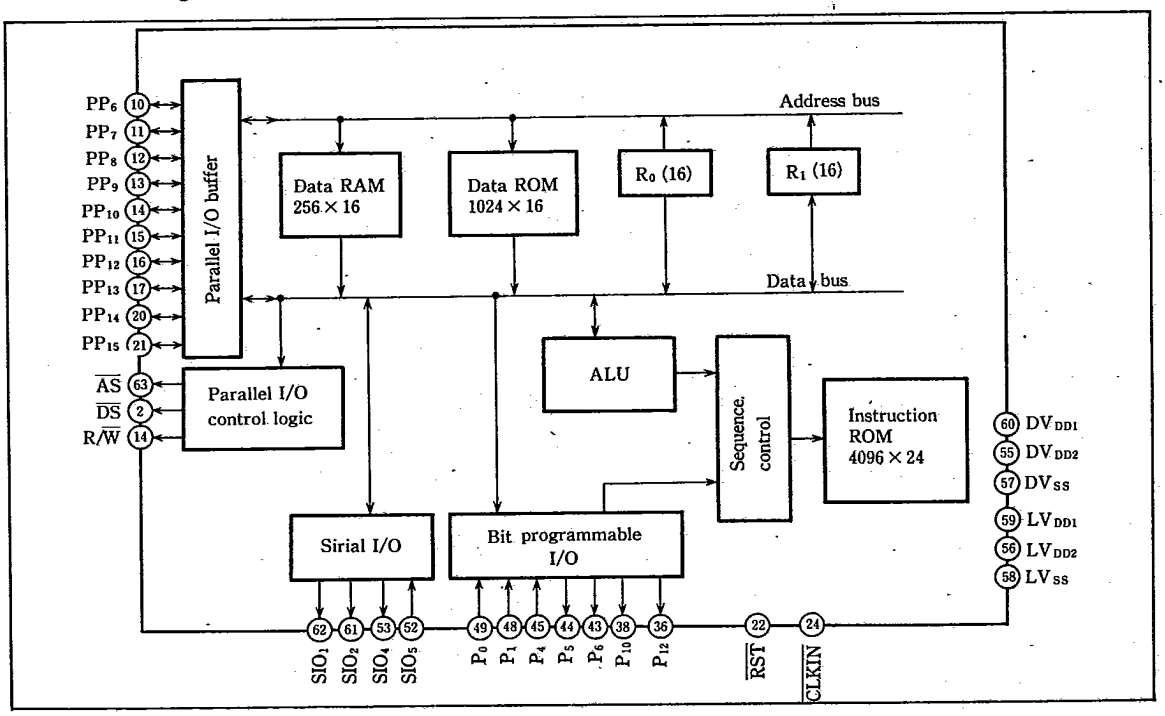
Features

1. Compatible with CCITT G Ⅱ/G Ⅲ facsimile MODEM.
2. In compliance with CCITT V29, V27ter, V21-2, T3, T4 and T30.
3. Half duplex communication
4. Tone output and detection
5. DTMF generator
6. DTMF detect function
7. Adaptive automatic equalization function (G Ⅲ)
8. CMOS low power consumption : 150mW (TYP.)
9. +5V single power supply
10. 64-pin quad flat package

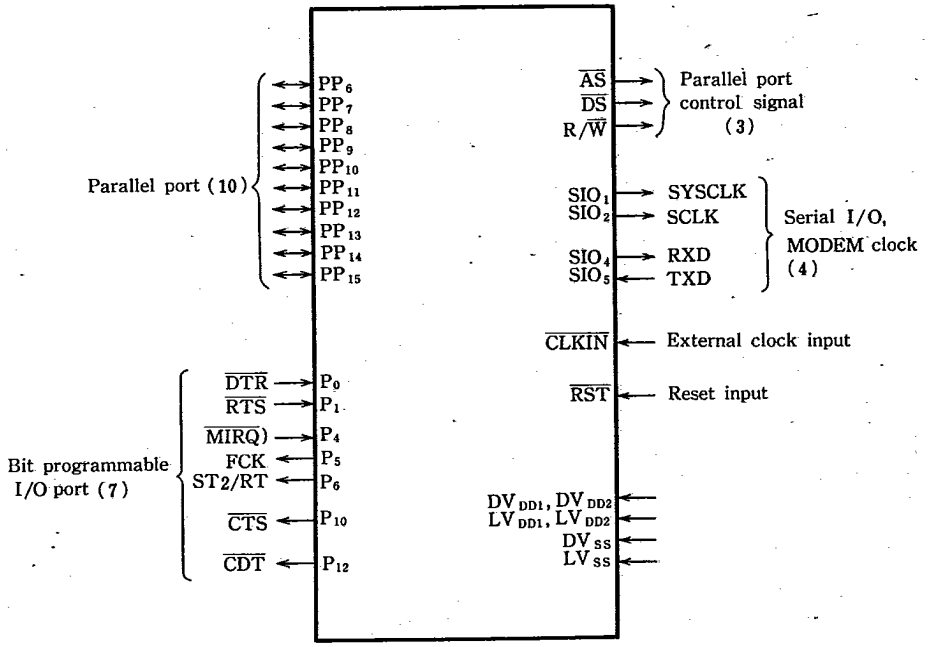
Pin Connections



Block Diagram



Pin Functions



Pin No.	Pin name	I/O	Function	Pin No.	Pin name	I/O	Function
1	NC	—	Non connection	41	NU (PU)	—	Not used. Pulled up when mounted on the circuit board
2	$\overline{DS}$	O	Data strobe pin	42	DV_{SS}	—	I/O driver unit GND
3-8	NC	—	Non connection	43, 44	P_6, P_5	O	Bit programmable output pin
9	DV_{SS}	—	I/O driver unit GND	45	P_4	I	Bit programmable input pin
10-17	PP_6-PP_{13}	I/O	Parallel I/O pin	46, 47	NU (PU)	—	Not used. Pulled up when mounted on the circuit board
18, 19	NC	—	Non connection	48, 49	P_1, P_0	I	Bit programmable input pin
20, 21	PP_{14}, PP_{15}	I/O	Parallel I/O pin	50	NU (PU)	—	Not used. Pulled up when mounted on the circuit board
22	$\overline{RST}$	I	Reset input pin	51	NC	—	Non connection
23	NC	—	Non connection	52	SIO_5	I	Serial input pin
24	$\overline{CLKIN}$	I	External clock input pin	53	SIO_4	O	Serial output pin
25	DV_{SS}	—	I/O driver unit GND	54	NC	—	Non connection
26	LV_{SS}	—	Logic unit GND	55	DV_{DD2}	—	I/O driver unit +5V power supply
27	NU (PU)	—	Not used. Pulled up when mounted on the circuit board	56	LV_{DD2}	—	Logic unit +5V power supply
28	NC	—	Non connection	57	DV_{SS}	—	I/O driver unit GND
29, 30	NU (PD)	—	Not used. Connected to V_{SS} when mounted on the circuit board	58	LV_{SS}	—	Logic unit GND
31-35	NC	—	Non connection	59	LV_{DD1}	—	Logic unit +5V power supply
36	P_{12}	O	Bit programmable output pin	60	DV_{DD1}	—	I/O driver unit +5V power supply
37	NC	—	Non connection	61, 62	SIO_2, SIO_1	O	Serial output pin
38	P_{10}	O	Bit programmable output pin	63	$\overline{AS}$	O	Address strobe pin
39, 40	NC	—	Non connection	64	$R/\overline{W}$	O	Read/write pin

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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3 to+7.0	V
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	0 to+70	℃
Storage temperature	T_{stg}	−55 to+150	℃

■ DC Characteristics

(V_{DD}=5V±5%, Ta=0 to+70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	V_{CL}				0.4	V	1
	V_{IL}				0.8	V	2
Input "High" voltage	V_{CH}		V_{DD}−0.4			V	1
	V_{IH}		2.0			V	2
Output "Low" voltage	V_{OL1}	I_{OL}=7.8mA, C_L=60pF+2TTL			0.4	V	3
	V_{OL2}	I_{OL}=5mA, C_L=40pF+2TTL			0.4	V	4
	V_{OL3}	I_{OL}=4.3mA, C_L=40pF+2TTL			0.4	V	5
Output "High" voltage	V_{OH1}	I_{OH}=14mA, C_L=60pF+2TTL	2.4			V	3
	V_{OH2}	I_{OH}=8mA, C_L=40pF+2TTL	2.4			V	4
	V_{OH3}	I_{OH}=7mA, C_L=40pF+2TTL	2.4			V	5
Input leakage current	I_{LI}	V_{IX}=0 to V_{DD}			10	μA	
Output leakage current	I_{LO}				10	μA	
Current consumption	I_{DD}	f=20MHz, V_{DD}=5.5V		30	100	mA	

Note 1 : Applied to pin $\overline{CLKIN}$
Note 2 : Applied to pins except for $\overline{CLKIN}$
Note 3 : Applied to pins $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, PP_6-PP_{15}
Note 4 : Applied to pins P_0, P_1, P_4, P_5, P_6, P_{10}, P_{12}
Note 5 : Applied to pins SIO_1, SIO_2, SIO_4

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■ AC Characteristics

Parallel I/O bus master timing (f=20.2752MHz)

〈Read cycle〉

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
R/$\overline{W}$ setup time	T_{RAS}	60			ns
Address setup time	T_{AAS}	35			ns
Address hold time	T_{AAH}	25			ns
$\overline{AS}$ pulse width	T_{ASW}	80			ns
$\overline{DS}$-R/$\overline{W}$ recovery time	T_{DRR}	115			ns
$\overline{DS}$-$\overline{AS}$ delay time	T_{DAD}	115			ns
$\overline{AS}$ access time	T_{ASA}			200	ns
$\overline{DS}$ access time	T_{DSA}			95	ns
Data retention time	T_{DSRH}	0			ns
$\overline{DS}$ pulse width	T_{DSRW}	230			ns
Address·$\overline{DS}$ delay time	T_{ADD}	25			ns
$\overline{AD}$·$\overline{DS}$ delay time	T_{ADRD}	75			ns
Low impedance recovery time 1	T_{OLZ1}	265			ns
Low impedance recovery time 2	T_{OLZ2}	115			ns

〈Write cycle〉

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
R/$\overline{W}$ setup time	T_{RAS}	60			ns
Address setup time 1	T_{AAS}	35			ns
Address hold time 1	T_{AAH}	25			ns
Address setup time 2	T_{ADS}	55			ns
Address hold time 2	T_{ADH}	115			ns
Data setup time	T_{DDS}	60			ns
Data hold time	T_{DDH}	170			ns
$\overline{AS}$ pulse width	T_{ASW}	80			ns
$\overline{DS}$ pulse width	T_{DSWW}	130			ns
$\overline{AS}$·$\overline{DS}$ delay time	T_{ADWD}	175			ns
$\overline{DS}$·R/$\overline{W}$ recovery time	T_{DRR}	115			ns
$\overline{DS}$·$\overline{AS}$ delay time	t_{DAD}	115			ns
Low impedance retention time	T_{ADLZ}	110			ns

■ Timing Diagram (Parallel I/O bus master timing)

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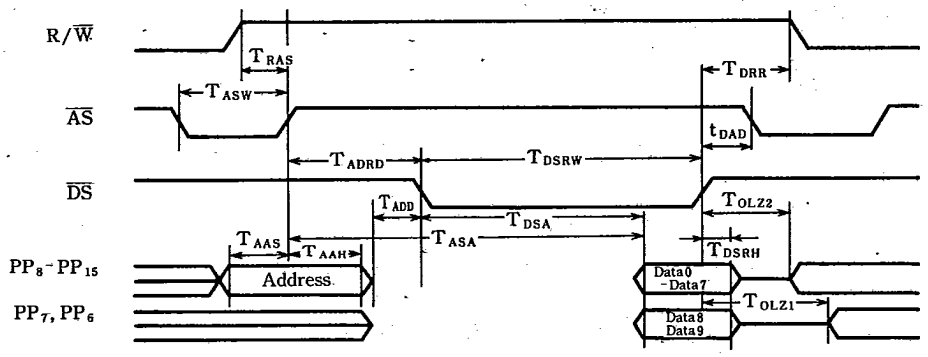
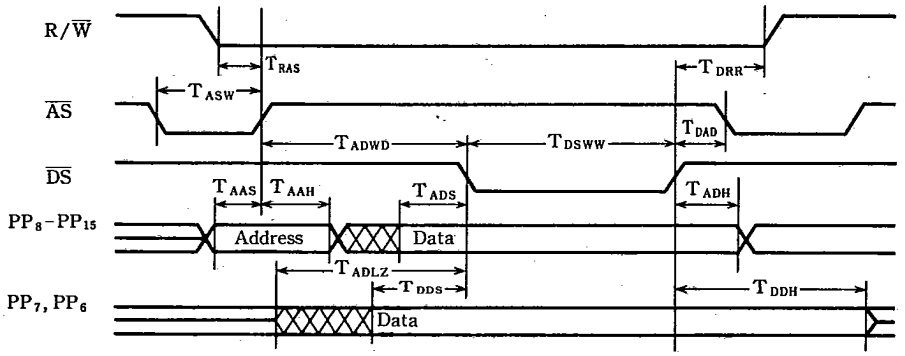
〈Read cycle〉



〈Write cycle〉



■ Pin Descriptions

(1) PP_6-PP_{15} (Pins 10-17, 20 and 21)

The PP_6-PP_{15} are 10-bit bidirectional bus ports used to interface address and data with the LR4906.

(2) $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ (Pins 2, 63 and 64)

$\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ provide signals to control parallel ports. The $\overline{AS}$ and $\overline{DS}$ are strobe pins for address and data, and the R/$\overline{W}$ pins is used to determine the direction of data.

(3) SIO_1, SIO_2, SIO_4 and SIO_5 (Pins 62, 61, 53 and 52)

The SIO_1 provides clocks for the SCF (Swithced Capacitor Filter) to the LR4906.

The SIO_2 provides sampling clocks to the LR4906.

The SIO_4 outputs the receiver serial output data.

The SIO_5 inputs the transmitter serial input data.

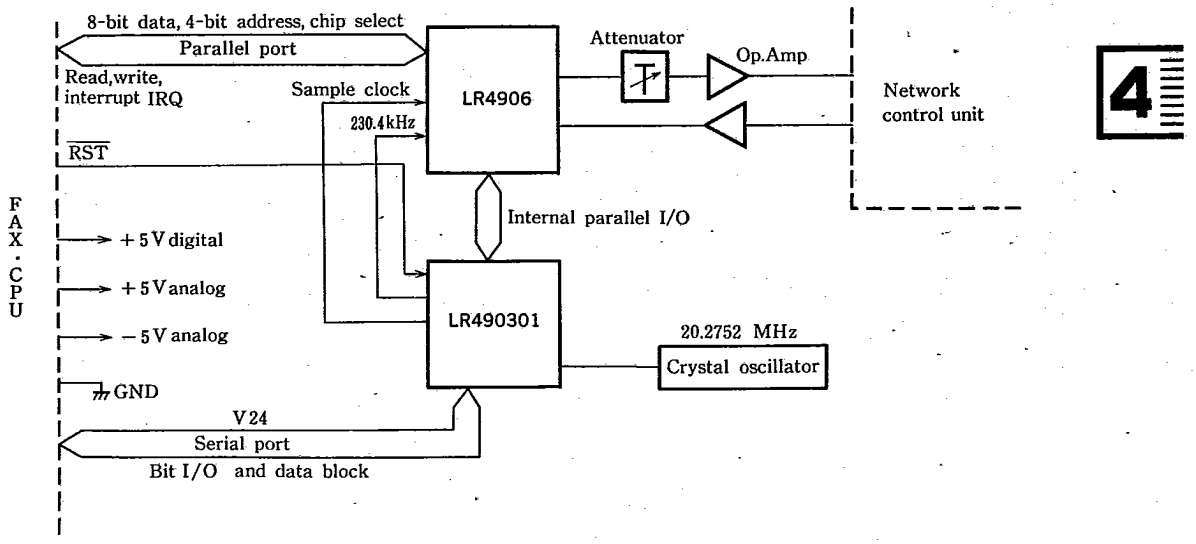
(4) P_0, P_1 P_4-P_6, P_{10} and P_{12} (Pins 49, 48, 45-43, 38 and 36)

The P_0, P_1, P_5, P_6, P_{10} and P_{12} are bit programmable I/O pins for serial I/O interface with a host CPU.

The P_4 inputs an interrupt signal from the LR4906.

■ Two-chip MODEM for G Ⅱ and G Ⅲ Facsimiles

(1) System block



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(2) Specifications and Features

No.	Parameter		Specifications
1	Communication system		Half duplex communication
2	Modulation system	QAM : 9600bps, 7200bps DPSK : 4800bps, 2400bps FSK : 300bps AM-PM-VSB : 10368Hz	In compliance with V29 V27ter, V21-2, T3, T4, and T30 for CCITT G Ⅱ and G Ⅲ facsimiles
3	Tonal signal detection	2100Hz, 1850Hz, 1650Hz, 1500Hz, 1300Hz, 1100Hz Other arbitrary frequencies within telephone band	Simultaneous detection of three kinds of tonal signals in FSK mode
4	High speed/low speed identification function	High speed : Spectrum signal of V29 and V27ter Low speed : Spectrum signal of V21-2 (Signals in 1650-1850Hz band)	High speed/low speed identification as shown left while waiting for speed training
5	Simultaneous receiving	In high speed mode, FSK detection can be done simultaneously, and a flag is displayed.	1. P3DET flag is displayed at high speed signal detection 2. FSKDET flag is displayed at low speed signal detection. HOST shifts it to FSK mode after FSKDET flag is noticed.
6	Training noise	With noises more than the signal level at high speed receiving, training does not start.	Training can be started when signal component more than prescribed S/N is detected in the noise.
7	Tap hold	V29 and V27ter equalized tap	In (V29→FSK→V29), tap value corresponding to network characteristics is stored.
8	Amplitude equalizer	Non-loaded cable/loaded cable Link amplitude equalizer	External fixed equalizer is not required due to a good performance of automatic equalizer for an automatic optimum equalization of network characteristics.
9	Delay equalizer	Link delay equalizer	
10	Signal quality data	Display of SQD (Signal quality)	Yes/No of transmission quality of more than BER 10^{-5} is displayed by flag
11	Tone dialer	DTMF	Simultaneous transmission of two frequencies
12	Receiving input level	G Ⅱ, G Ⅲ	−4 to −43dBm
13	Transmission output level		−4dBm (with 10kΩ load)
14	I/O control	TXD/RXD control	Data serial system
15	G Ⅱ AGC control		AGC control is not required from HOST side. AGC value is stored upon signal reception.
16	Package size	Molded unit size	LR490301 (DSP) 20×16mm LR4906 (ANALOG) 20×16mm
17	Power supply	Average effective current	LR490301 +5V(D) 40mA LR4906 +5V(D) 10mA +5V(D) 30mA −5V(D) 35mA

System Configuration Example

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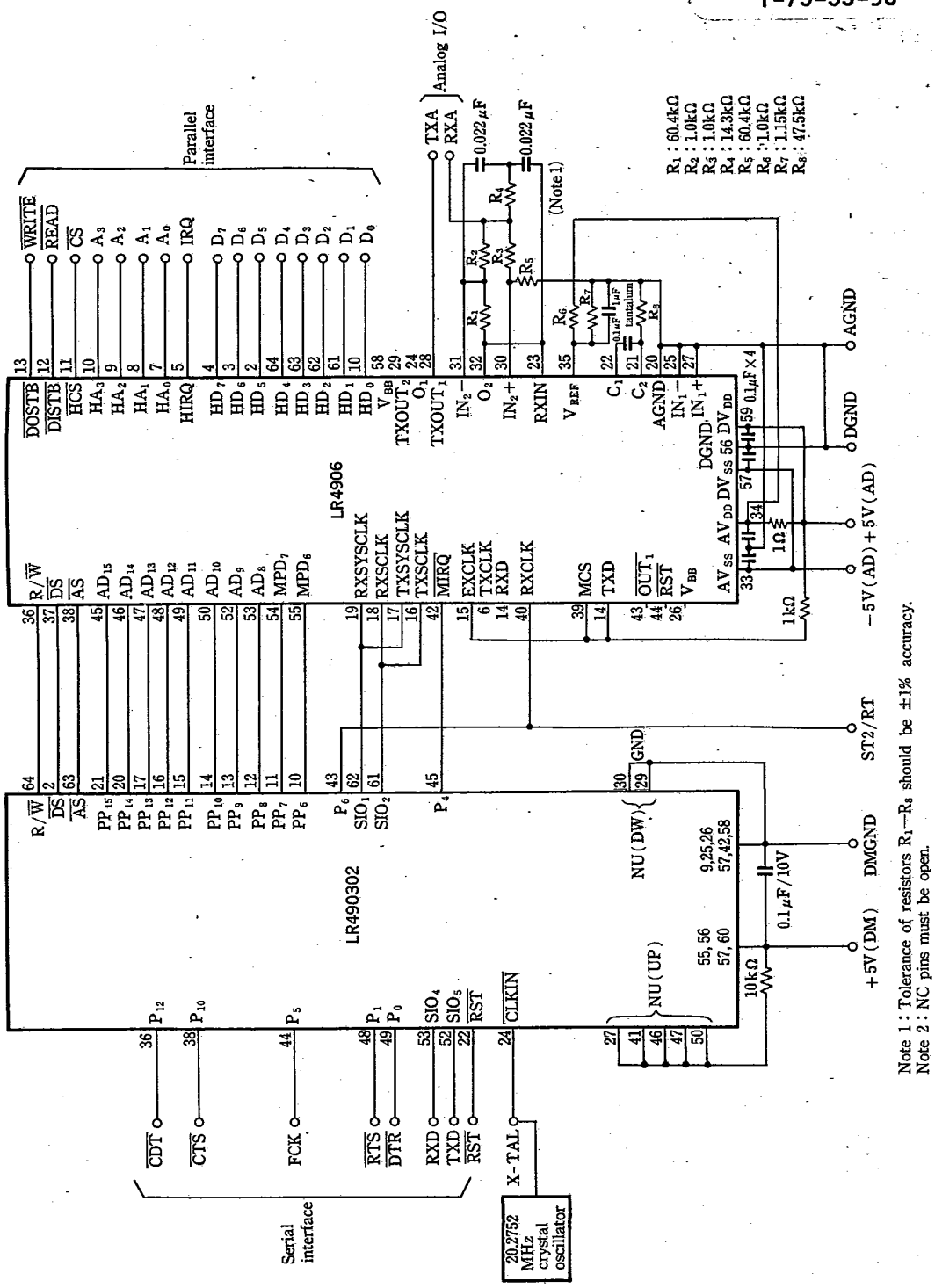

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