LH5023B Dot Matrix LCD Segment Driver LSI

Description

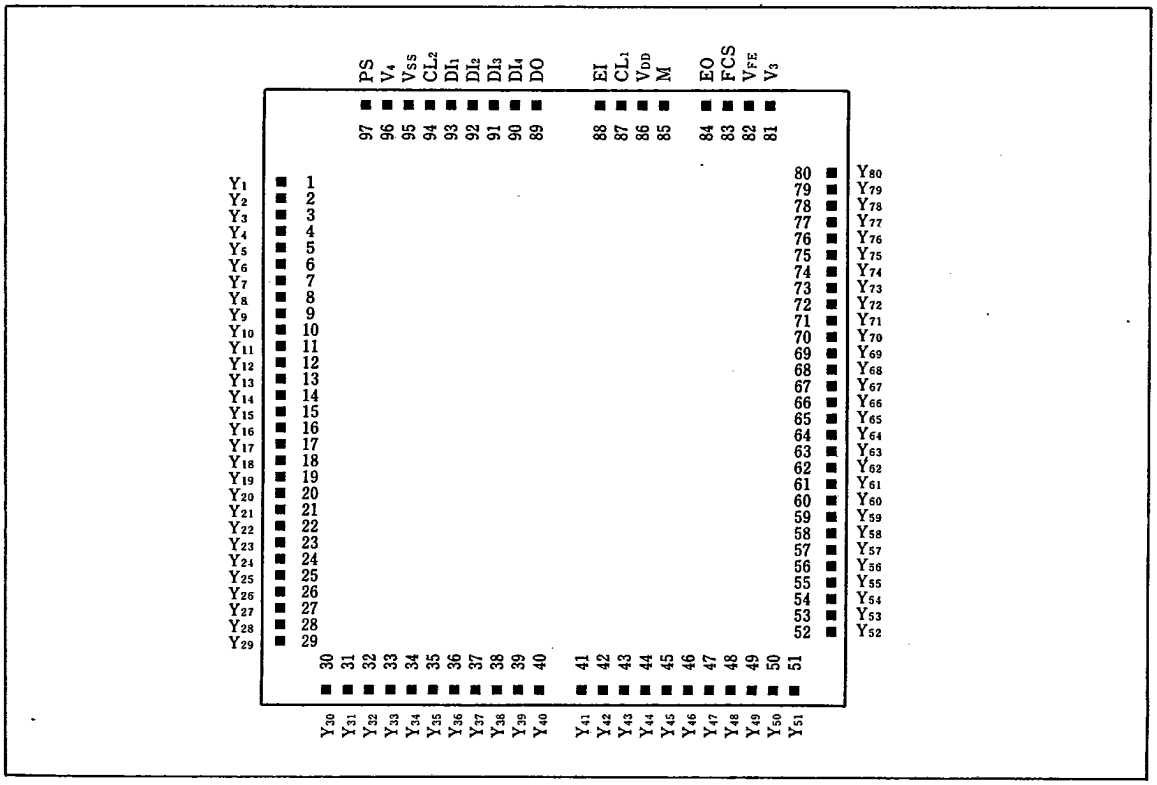
The LH5023B is an 80-output LCD segment driver with right directional shifting system, fabricated using CMOS process. This LSI receives the display pattern input and converts it into 4-bit parallel output data through an 80-stage latch circuit. Then, depending on whether the data is "1" or "0", the waveform of display or non-display is output.

The LH5023B has a chip select function which allows the shift clock CL_2 to be internally inhibited in non-select mode.

Features

1. CMOS process
2. 4-bit parallel input segment driver with a chip select
3. In a chip select mode, internal CL_2 is stopped automatically after 80 bits of data have been input
4. Low power consumption
5. Package: Film (97 pads)

Pad Layout



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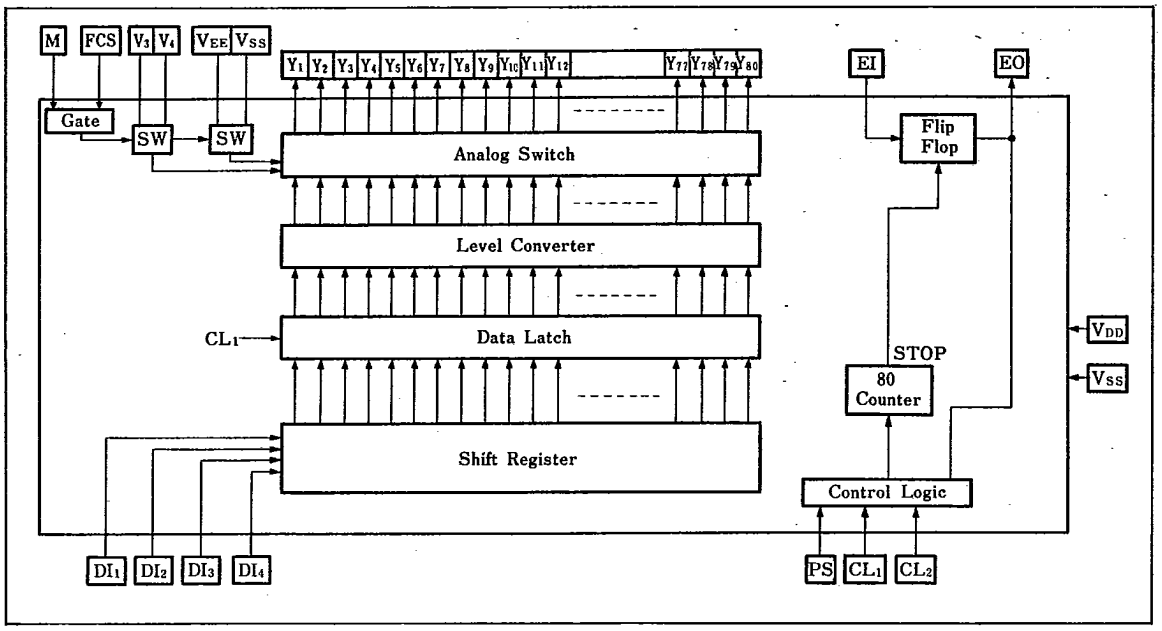
Block Diagram



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■ Pad Function

Pad name	I/O	Function
V_{DD}		Logic power supply. (−5V)
V_{EE}		LCD drive power supply. (−24V)
V_{SS}		GND (0V). (Common to both LCD and logic circuit.)
V_3, V_4		Output voltage supply for the LCD driver circuits. $V_{SS} > V_3 > V_4 > V_{EE}$
Y_1-Y_{80}	O	LCD drive output.
CL_1	I	Data latch clock. (This must be given at twice four of shift clock.)
CL_2	I	Data shift clock.
FCS PS	I I	Mode select pins for 4-bit parallel segment driver. Connect FCS to V_{DD}, and PS to V_{SS}. Then, chip select is to be enabled and DO output to be V_{SS} level. • The relationship between the 4-bit parallel input data and the Y output pins is as follows: DI_1: Y_1, Y_5, Y_9, ····· Y_{73}, Y_{77} DI_2: Y_2, Y_6, Y_{10}, ····· Y_{74}, Y_{78} DI_3: Y_3, Y_7, Y_{11}, ····· Y_{75}, Y_{79} DI_4: Y_4, Y_8, Y_{12}, ····· Y_{76}, Y_{80} • The pins not to be used must be fixed at the same level as V_{SS} pin or V_{DD} pin for reducing current consumption.
M	I	LCD driver waveform alternating signal input pin.
D_{11}-D_{14}	I	Display data input pins
EI EO	I O	This is only used in chip select mode. The basic functions are as follows. (1) EO is low during $CL_1 \times \overline{CL_2}$. (2) After (1) by making EI high, the device goes the select state and the input data is read in on clock $CL_2\downarrow$. Input data is shifted synchronizing with CL_2. (3) After 80 input datas have been read in, EO automatically goes high, and data input is completed. In serial input mode 80 datas are needed. In 4-bit parallel mode 20 datas are needed. (4) When more than two devices are used in chip select mode, EO and EI must be connected. (a) By (1) EO of all the connected devices are reset, and they go non-select state and wait EI. (b) When the first device EI of the connected devices is high, this device operates (2) and (3). (c) After (b) by connecting EO of the first and EI of the next, next device operates (2) and (3), and the following devices operate as same. In non-select mode clock CL_2 is stopped internally, so that power consumption is a little.

Latch data	M	Y_{OUT}
Low No-display	L	V_3
	H	V_4
High display	L	GND
	H	V_{EE}

3

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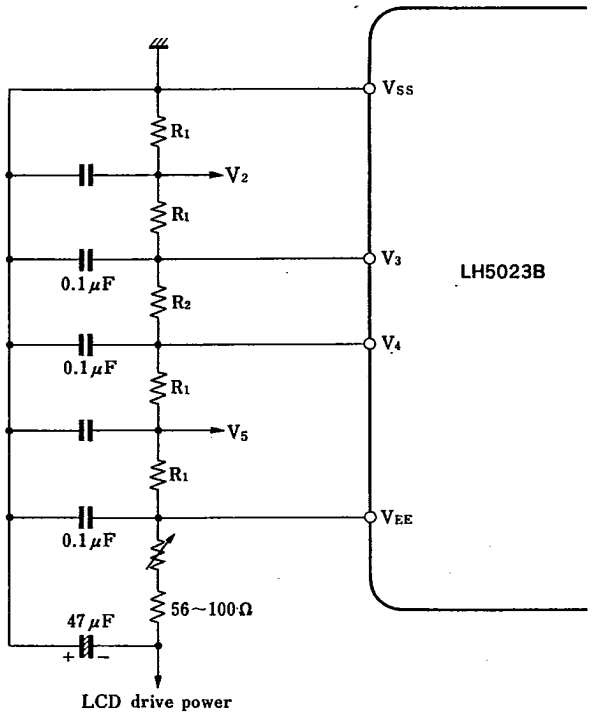
■ Connection-Diagram of LCD Drive Power



Note: Be sure to apply 56Ω to 100Ω of a resistor to the LCD drive power supply.

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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Applied voltage* (logic circuit)	V_{DD}	+0.3 to −7.0	V
Applied voltage* (LCD drive circuit)	V_{EE}	+0.3 to −29.0	V
Input voltage* (logic circuit)	V_I	+0.3 to V_{DD}−0.3	V
Operating temperature	T_{opr}	−20 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

* The maximum applicable voltage on any pin with respect to V_{SS}.

■ DC Characteristics

(V_{SS}=0V, V_{DD}=−5V±0.5V, V_{EE}=−24V±3V, V_3=−2.5V to −5.5V, V_4=−16.5V to −23.5V, Ta=−20℃ to +70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input "Low" voltage	V_{IL}			0.8×V_{DD}	V
Input "High" voltage	V_{IH}		0.2×V_{DD}		V
Output "Low" voltage	V_{OL}	I_{OL}=0.4mA		V_{DD}+0.4	V
Output "High" voltage	V_{OH}	I_{OH}=0.4mA	−0.4		V
Voltage drop between V_i-Y_i	V_{D1}	0.5mA into of the pins Y_1 through Y_{80} V_3=2/12V_{EE}, V_4=10/12V_{EE}		1.0	V
Voltage drop between V_i-Y_i	V_{D2}	0.08mA into each of pins Y_1 through Y_{80} V_3=2/12V_{EE}, V_4=10/12V_{EE}		1.5	V
Input leakage current	$\lvert I_{LI} \rvert$			1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$			10.0	μA
Logic circuit current consumption	I_{LOG}	Frequency 3MHz		10.0	mA

(V_{SS}=0V, V_{DD}=−5V±0.5V, V_{EE}=−15V to −24V, V_3=−1.5V to −5V, V_4=−11.5V to −21V, Ta=−20℃ to +70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input "Low" voltage	V_{IL}			0.8V_{DD}	V
Input "High" voltage	V_{IH}		0.2V_{DD}		V
Output "Low" voltage	V_{OL}	I_{OL}=0.4mA		V_{DD}+0.4	V
Output "High" voltage	V_{OH}	I_{OH}=0.4mA	−0.4		V
Voltage drop between V_i-Y_i	V_{D1}	0.35mA into of the pins Y_1 through Y_{80} V_3=2/12V_{EE}, V_4=10/12V_{EE}		1.0	V
Voltage drop between V_i-Y_i	V_{D2}	0.06mA into each of pins Y_1 through Y_{80} V_3=2/12V_{EE}, V_4=10/12V_{EE}		1.5	V
Input leakage current	$\lvert I_{LI} \rvert$			1.0	μA
Output leakage current	$\lvert I_{LO} \rvert$			10.0	μA
Logic circuit current consumption	I_{LOG}	Frequency 3MHz, 4-bit parallel transfer		10.0	mA

■ Precaution

(1) Care required when power ON and power OFF

Since the LCD drive voltage of this LSI is high, care must be taken not to give a permanent damage to the device due to a large current that flows in it, that may be caused by applying a voltage to the power supply for the LCD drive while the power supply for the logic is in a floating state.

Therefore, in turning the power ON, the power for the LCD drive should be turned ON after, or simultaneously with, the power for the logic ON.

In addition, in turning the power OFF, the power for the logic should be turned OFF after, or simultaneously with, the power for the LCD drive OFF.

(2) Interface with other LSI's

Since the power for the logic of this LSI employs a negative voltage, take care of the polarity of the power supply in interfacing this device with other LSI's.

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■ AC Characteristics

4-bit parallel segment driver (PS="High", FCS="Low")

(V_{SS}=0V, V_{DD}=−5V±0.5V, V_{EE}=−24V±3V, Ta=−20℃ to +70℃)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Applicable pin
Clock cycle	t_C		330		ns	CL_2
Clock "High" width	t_{CWH}		145		ns	CL_2
Clock "Low" width	t_{CWL}		145		ns	CL_1, CL_2
Data setup time	t_{SU}		70		ns	DI_1,DI_2,DI_3,DI_4,EI
Data hold time	t_H		50		ns	DI_1,DI_2,DI_3,DI_4,EI
Output delay time	t_D	C_1=15pF		230	ns	EO
Latch clock "High" width	t_{LWH}		130	*2	ns	CL_1
Clock allowance time (from CL_1↓ to CL_2↑)	t_{C12}		0		ns	CL_1,CL_2
Clock allowance time (from CL_2↓ to CL_1↓)*1	t_{C21}		100		ns	CL_1,CL_2
Clock allowance time (from CL_2↑ to CL_1↑)	t_{P21}		20		ns	CL_1,CL_2
Clock time	t_{CT}			50	ns	CL_1,CL_2
Overlap time of CL_2 "Low" and CL_1 "High"	t_{OV}		80		ns	CL_1,CL_2

[Test condition]

Input amplitude: $0.8V\times V_{DD}$, $0.2V\times V_{DD}$

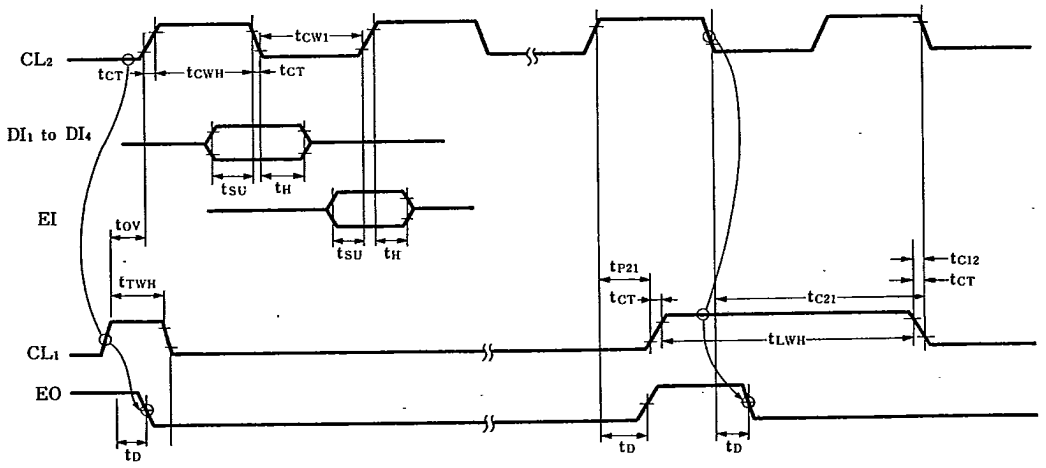
Input decision level: $0.8V\times V_{DD}$, $0.2V\times V_{DD}$

Output decision level: $0.8V\times V_{DD}$, $0.2V\times V_{DD}$

*1: Internal shift register setup time

*2: $1.5t_C-t_C12-t_P21-3t_{CT}$

■ Timing Diagram



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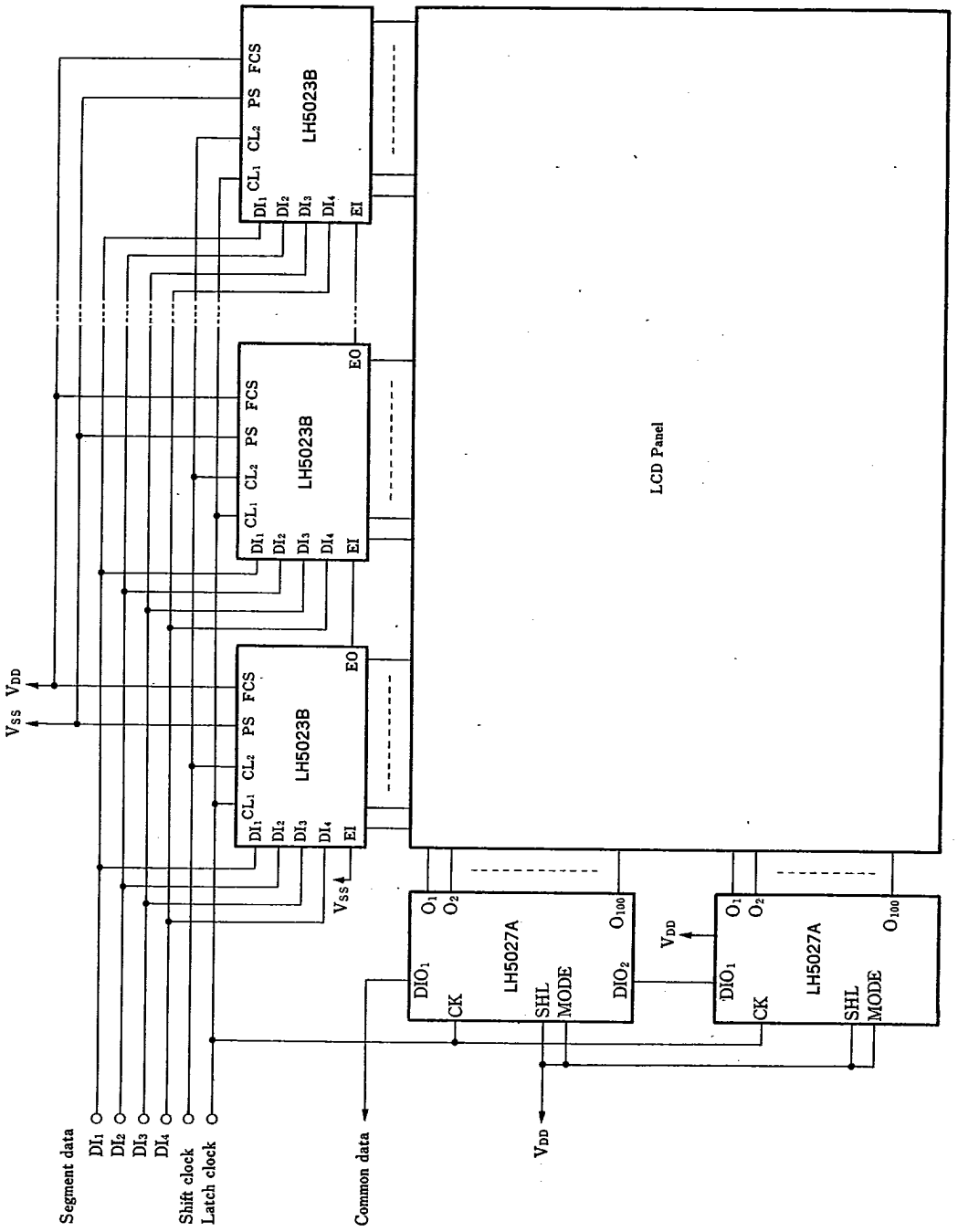
System Configuration Example



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