USB Port Power Supply Controller

ISL6186

The ISL6186 USB power controller family provides overcurrent (OC) fault protection for one or more USB ports.

This product family consists of eight individual functional product variants and three package options and is operation rated for a nominal +2.5V to +5V range and specified over the full commercial and industrial temperature ranges.

Each ISL6186 type incorporates a 45mΩ P-channel MOSFET power switch for power control and features internal current monitoring, accurate current limiting, and current limited delay to turn-off for system supply protection along with control and communication I/O.

The ISL6186 family offers product variants with specified continuous output current levels of 1.5A, 3A or 3.6A, enable active high or low inputs, and latch off or automatic retry after overcurrent turn-off, making these devices well suited for many low-power applications.

This family of ICs is offered in an industry standard SOIC package as well as in the 70% smaller 3x3 DFN package, which provides the same performance and an additional Power-Good output feature in the smallest possible (10 Ld DFN) package.

Features

- 2.5V to 5V Operating Range
- 45mΩ Integrated Power P-channel MOSFET Switches
- Continuous Current Options for 1.5A, 3A and 3.6A
- Thermally Insensitive 12ms of Current Limiting Prior to Turn-Off
- Output Discharges with Reverse Current Blocking When Disabled
- Latch-off or Auto Restart and Enable Polarity Options
- 1µA Off-State Supply Current
- Industry Standard Pin-for-Pin SOIC and Smaller DFN Packages Available

Applications

- USB Port Power Management Including USB 3.0
- Low Power Electronic Circuit Limiting and Breaker

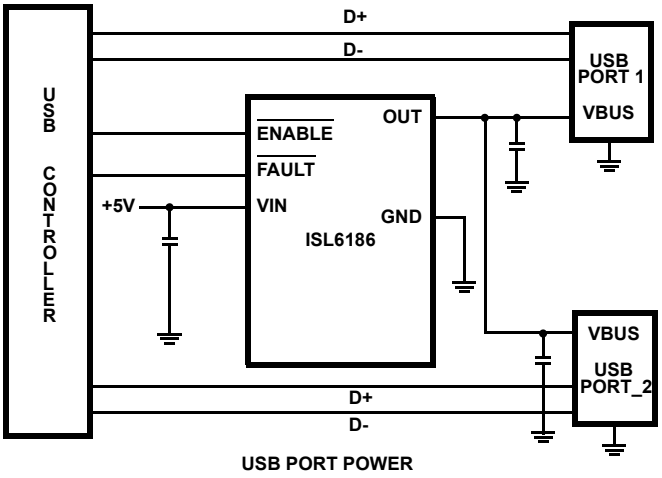


FIGURE 1. TYPICAL APPLICATION

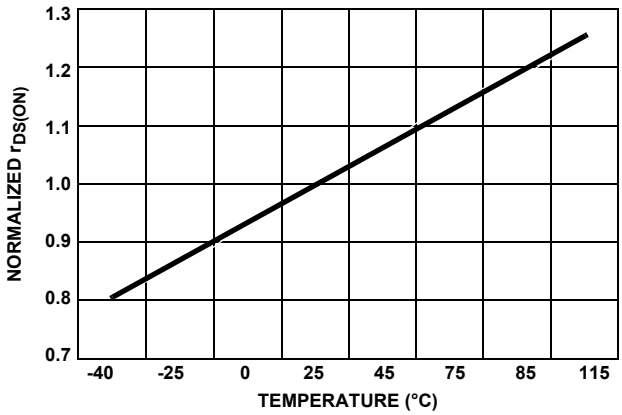
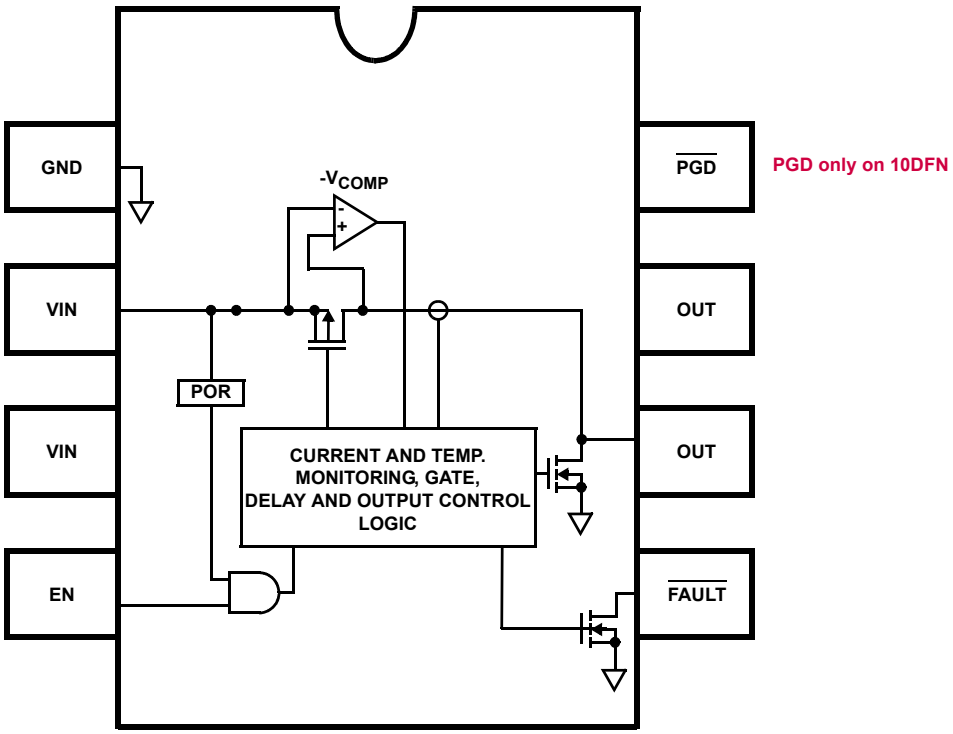


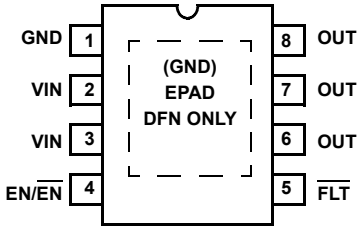
FIGURE 2. NORMALIZED $r_{DS(ON)}$ TEMPERATURE CHARACTERISTIC CURVE

Simplified Block Diagram

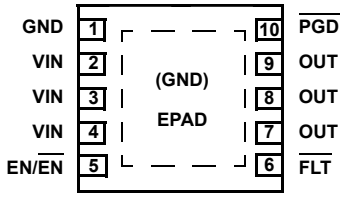


Pin Configurations

ISL6186
(8 LD SOIC/DFN)
TOP VIEW



ISL6186
(10 LD DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER		SYMBOL	DESCRIPTION
8 Ld SOIC/DFN	10 Ld DFN		
1	1	GND	IC ground reference
2, 3	2, 3, 4	VIN	Chip bias, Controlled Voltage Input, Undervoltage Lock Out (UVLO). V_{IN} provides chip bias voltage. At V_{IN} < 1.7V, chip functionality is disabled, $\overline{FLT}$ is active and floating and OUT is held low. Range 0V to 5.5V
4	5	EN/$\overline{EN}$	Enable/Disable inputs, Active high (EN) and active low ($\overline{EN}$) options enable the power switch. These inputs have internal 1MΩ pull-off resistors. Range 0V to V_{IN}

Pin Descriptions (Continued)

PIN NUMBER		SYMBOL	DESCRIPTION
8 Ld SOIC/DFN	10 Ld DFN		
5	6	$\overline{FLT}$	Overcurrent Fault Indicator. Overcurrent fault indicator. $\overline{FLT}$ floats and is disabled until $V_{IN} > V_{UVLO}$. This output is pulled low after the current limit time-out period has expired. Fault is not signaled due to over-temperature shut down. Range 0V to V_{IN}
6, 7, 8	7, 8, 9	OUT	Controlled Supply Output. Upon an OC condition, I_{OUT} is current limited. Current limit response time is within 200µs. This output will remain in current limit for a nominal 12ms before being turned off either for the latch or auto retry versions. Range 0V to V_{IN}
-	10	$\overline{PGD}$	Open drain Power-Good output that pulls low 40ms after V_{OUT} = 90% of V_{IN} and rises after V_{OUT}< 85% of V_{IN}. Range 0V to V_{IN}
PD (DFN only)	PD	EPAD	Thermal Dissipation Exposed PAD Range: Connect to GND.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	EN/$\overline{EN}$ INPUT	V_{IN} = 5V MAXIMUM CONTINUOUS IOUT (A)	LATCH/ AUTO RETRY	POWER-GOOD OUTPUT	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL61861ACBZ	61861A CBZ	EN	1.5	LATCH	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861BCBZ	61861B CBZ	EN	1.5	RETRY	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861CCBZ	61861C CBZ	EN	3	LATCH	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861DCBZ	61861D CBZ	EN	3	RETRY	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861ECBZ	61861E CBZ	$\overline{EN}$	1.5	LATCH	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861FCBZ	61861F CBZ	$\overline{EN}$	1.5	RETRY	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861GCBZ	61861G CBZ	$\overline{EN}$	3	LATCH	NO	0 to +70	8 Ld SOIC	M8.15
ISL61861HCBZ	61861H CBZ	$\overline{EN}$	3	RETRY	NO	0 to +70	8 Ld SOIC	M8.15
ISL61862ACRZ	62AC	EN	1.5	LATCH	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862BCRZ	62BC	EN	1.5	RETRY	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862CCRZ	62CC	EN	3	LATCH	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862DCRZ	62DC	EN	3	RETRY	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862ECRZ	62EC	$\overline{EN}$	1.5	LATCH	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862FCRZ	62FC	$\overline{EN}$	1.5	RETRY	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862GCRZ	62GC	$\overline{EN}$	3	LATCH	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61862HCRZ	62HC	$\overline{EN}$	3	RETRY	NO	0 to +70	8 Ld DFN	L8.3x3J
ISL61863ACRZ	63AC	EN	1.5	LATCH	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863BCRZ	63BC	EN	1.5	RETRY	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863CCRZ	63CC	EN	3	LATCH	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863DCRZ	63DC	EN	3	RETRY	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863ECRZ	63EC	$\overline{EN}$	1.5	LATCH	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863FCRZ	63FC	$\overline{EN}$	1.5	RETRY	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863GCRZ	63GC	$\overline{EN}$	3	LATCH	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863HCRZ	63HC	$\overline{EN}$	3	RETRY	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863ICRZ	63IC	EN	3.6	LATCH	YES	0 to +70	10 Ld DFN	L10.3x3

Ordering Information (Continued)

PART NUMBER (Notes 1, 2, 3)	PART MARKING	EN/$\overline{EN}$ INPUT	V_{IN} = 5V MAXIMUM CONTINUOUS IOUT (A)	LATCH/ AUTO RETRY	POWER-GOOD OUTPUT	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL61863JCRZ	63JC	EN	3.6	RETRY	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863KCRZ	63KC	$\overline{EN}$	3.6	LATCH	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61863LCRZ	63LC	$\overline{EN}$	3.6	RETRY	YES	0 to +70	10 Ld DFN	L10.3x3
ISL61861AIBZ	61861A IBZ	EN	1.5	LATCH	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861BIBZ	61861B IBZ	EN	1.5	RETRY	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861CIBZ	61861C IBZ	EN	3	LATCH	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861DIBZ	61861D IBZ	EN	3	RETRY	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861EIBZ	61861E IBZ	$\overline{EN}$	1.5	LATCH	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861FIBZ	61861F IBZ	$\overline{EN}$	1.5	RETRY	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861GIBZ	61861G IBZ	$\overline{EN}$	3	LATCH	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61861HIBZ	61861H IBZ	$\overline{EN}$	3	RETRY	NO	-40 to +85	8 Ld SOIC	M8.15
ISL61862AIRZ	62AI	EN	1.5	LATCH	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862BIRZ	62BI	EN	1.5	RETRY	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862CIRZ	62CI	EN	3	LATCH	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862DIRZ	62DI	EN	3	RETRY	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862EIRZ	62EI	$\overline{EN}$	1.5	LATCH	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862FIRZ	62FI	$\overline{EN}$	1.5	RETRY	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862GIRZ	62GI	$\overline{EN}$	3	LATCH	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61862HIRZ	62HI	$\overline{EN}$	3	RETRY	NO	-40 to +85	8 Ld DFN	L8.3x3J
ISL61863AIRZ	63AI	EN	1.5	LATCH	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863BIRZ	63BI	EN	1.5	RETRY	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863CIRZ	63CI	EN	3	LATCH	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863DIRZ	63DI	EN	3	RETRY	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863EIRZ	63EI	$\overline{EN}$	1.5	LATCH	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863FIRZ	63FI	$\overline{EN}$	1.5	RETRY	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863GIRZ	63GI	$\overline{EN}$	3	LATCH	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863HIRZ	63HI	$\overline{EN}$	3	RETRY	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863IIRZ	63II	EN	3.6	LATCH	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863JIRZ	63JI	EN	3.6	RETRY	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863KIRZ	63KI	$\overline{EN}$	3.6	LATCH	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61863LIRZ	63LI	$\overline{EN}$	3.6	RETRY	YES	-40 to +85	10 Ld DFN	L10.3x3
ISL61861AEVAL1Z (ISL61861C)		EN	3	LATCH	NO	-	8 Ld SOIC	EVAL BD
ISL61862HEVAL1Z (ISL61862F)		$\overline{EN}$	1.5	RETRY	NO	-	8 Ld DFN	EVAL BD
ISL61863LEVAL1Z (ISL61863L)		$\overline{EN}$	3.6	RETRY	YES	-	10 Ld DFN	EVAL BD

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6186. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

Supply Voltage (VIN to GND, Note 7) 6.5V
EN, FAULT. . . . . VIN
OUT. . . . . GND - 0.3V to VIN 0.3V
Output Current . . . . . Short Circuit Protected; Limited to 5A
ESD Rating
  Human Body Model (Per MIL-STD-883 Method 3015.7). 3kV
  Machine Model (Per MIL-STD-883 Method 3015.7) 300V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead SOIC Package (Note 4)	120	N/A
8 Lead 3x3 DFN Package (Notes 5, 6)	48	6
10 Lead 3x3 DFN Package (Notes 5, 6)	48	6

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Commercial Temperature Range . . . . . 0°C to +70°C
Industrial Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range (Typical). . . . . 2.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{IN} = 5V, T_A = T_J, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER SWITCH						
$r_{DS(ON)\_50}$	ON-Resistance at 5.0V (Pulse Tested)	V_{IN} = 5V, I_{OUT} = 0.5A, T_A = T_J = +25°C	-	45	48	mΩ
		T_A = T_J = +85°C	-	50	**54**	mΩ
$r_{DS(ON)\_33}$	ON-Resistance at 3.3V (Pulse Tested)	V_{IN} = 3.3V, I_{OUT} = 0.5A, T_A = T_J = +25°C	-	54	57	mΩ
		T_A = T_J = +85°C	-	61	**64**	mΩ
$r_{DS(ON)\_25}$	On Resistance at 2.5V (Pulse Tested)	V_{IN} = 2.5V, I_{OUT} = 0.5A, T_A = T_J = +25°C	-	65	69	mΩ
		T_A = T_J = +85°C	-	74	**79**	mΩ
V_{OUT_DIS}	Disabled Output Voltage	V_{IN} = 5V, Switch Disabled, 50µA Load	-	22	**45**	mV
R_{OUT_PD}	Output Pull-Down Resistor	V_{IN} = 5V, Switch Disabled	**3.4**	5	**6**	kΩ
t_R	V_{OUT} Rise Time	R_L = 10Ω, C_L = 10µF, 10% to 90%	-	10	-	µs
t_F	Slow V_{OUT} Turn-off Fall Time	R_L = 10Ω, C_L = 10µF, 90% to 10%	-	200	-	µs
CURRENT CONTROL						
$I_{OUT\_CONT\_5}$	Maximum Continuous Current, V_{IN} = 5V Guaranteed by the Minimum I_{trip} Current Specification	ISL6186xA, B, E, F	-	-	**1.5**	A
$I_{OUT\_CONT\_5}$		ISL6186xC, D, G, H	-	-	**3.0**	A
$I_{OUT\_CONT\_5}$		ISL6186xI, J, K, L (10 Ld DFN)	-	-	**3.6**	A
$I_{OUT\_CONT\_3}$	Maximum Continuous Current, V_{IN} = 3.3V Guaranteed by the Minimum I_{trip} Current Specification	ISL6186xA, B, E, F	-	-	**1.5**	A
$I_{OUT\_CONT\_3}$		ISL6186xC, D, G, H	-	-	**2.5**	A
$I_{OUT\_CONT\_3}$		ISL61861I, J, K, L (10 Ld DFN)	-	-	**2.7**	A
$I_{OUT\_CONT\_2}$	Maximum Continuous Current, V_{IN} = 2.5V	ISL6186xA, B, E, F	-	1.2	-	A
$I_{OUT\_CONT\_2}$		ISL61861C, D, G, H (SOIC)	-	1.8	-	A
$I_{OUT\_CONT\_2}$		ISL61862, ISL61863 C, D, G, H (DFN)	-	2	-	A
$I_{OUT\_CONT\_2}$		ISL61863I, J, K, L (10 Ld DFN)	-	2	-	A

Electrical Specifications V_{IN} = 5V, $T_A = T_J$, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
I_{TRIP_5}	Trip Current, V_{IN} = 5V	ISL6186xA, B, E, F	**1.7**	2.5	**3.3**	A
I_{TRIP_5}		ISL6186xC, D, G, H	**3.0**	3.9	**4.5**	A
I_{TRIP_5}		ISL61863I, J, K, L (10 Ld DFN)	**3.7**	3.9	**5.0**	A
I_{TRIP_3}	Trip Current, V_{IN} = 3.3V	ISL6186xA, B, E, F	**1.7**	2.1	**2.7**	A
I_{TRIP_3}		ISL6186xC, D, G, H	**2.8**	3.5	**4.0**	A
I_{TRIP_3}		ISL61863I, J, K, L (10 Ld DFN)	**3.5**	3.9	**4.3**	A
I_{TRIP_2}	Trip Current, V_{IN} = 2.5V	ISL6186xA, B, E, F	-	1.8	-	A
I_{TRIP_2}		ISL6186xC, D, G, H	-	3.2	-	A
I_{TRIP_2}		ISL61863I, J, K, L (10 Ld DFN)	-	3.4	-	A
I_{LIM_5}	Current Limit, V_{IN} = 5V	ISL6186xA, B, E, F, $V_{IN} - V_{OUT}$ = 1V	**1.37**	1.6	**1.81**	A
I_{LIM_5}		ISL6186xC, D, G, H, $V_{IN} - V_{OUT}$ = 1V	**2.82**	3.1	**3.42**	A
I_{LIM_5}		ISL61863I, J, K, L, (10 Ld DFN) $V_{IN} - V_{OUT}$ = 1V	**3.24**	3.6	**4.00**	A
I_{LIM_3}	Current Limit, V_{IN} = 3.3V	ISL6186xA, B, E, F, $V_{IN} - V_{OUT}$ = 1V	**1.35**	1.5	**1.77**	A
I_{LIM_3}		ISL6186xC, D, G, H, $V_{IN} - V_{OUT}$ = 1V	**2.72**	3.0	**3.35**	A
I_{LIM_3}		ISL61863I, J, K, L (10 Ld DFN), $V_{IN} - V_{OUT}$ = 1V	**3.22**	3.5	**3.95**	A
I_{LIM_2}	Current Limit, V_{IN} = 2.5V	ISL6186xA, B, E, F, $V_{IN} - V_{OUT}$ = 1V	**1.30**	1.5	**1.70**	A
I_{LIM_2}		ISL6186xC, D, G, H, $V_{IN} - V_{OUT}$ = 1V	**2.55**	2.9	**3.14**	A
I_{LIM_2}		ISL61863I, J, K, L (10 Ld DFN), $V_{IN} - V_{OUT}$ = 1V	**3.07**	3.3	**3.75**	A
I_{sc_5}	Short Circuit Current, V_{IN} = 5V	ISL6186xA, B, E, F, V_{OUT} = 0V	**1.45**	2.0	**2.35**	A
I_{sc_5}		ISL6186xC, D, G, H, V_{OUT} = 0V	**2.60**	3.4	**4.50**	A
I_{sc_5}		ISL61863I, J, K, L (10 Ld DFN), V_{OUT} = 0V	**2.48**	3.5	**5.00**	A
I_{sc_3}	Short Circuit Current, V_{IN} = 3.3V	ISL6186XA, B, E, F, V_{OUT} = 0V	**0.95**	1.2	**1.50**	A
I_{sc_3}		ISL6186XC, D, G, H, V_{OUT} = 0V	**1.95**	2.2	**2.70**	A
I_{sc_3}		ISL61863I, J, K, L (10 Ld DFN), V_{OUT} = 0V	**2.00**	2.5	**3.00**	A
I_{sc_2}	Short Circuit Current, V_{IN} = 2.5V	ISL6186xA, B, E, F, V_{OUT} = 0V	-	1.1	-	A
I_{sc_2}		ISL6186xC, D, G, H, V_{OUT} = 0V	-	2.1	-	A
I_{sc_2}		ISL61863I, J, K, L, (10 Ld DFN) V_{OUT} = 0V	-	2.4	-	A
$tsett_{Ilim}$	OC to Limit Settling Time	$V_{IN}/R_L = 2I_{LIM}$, C_L = 10µF to within 10% of I_{LIM}	-	200	-	µs
$tsett_{Ilim\_sev}$	Severe OC to Limit Settling Time	$V_{IN}/R_L = 4I_{LIM}$, C_L = 10µF to within 10% of I_{LIM}	-	30	-	µs
t_{CL}	Current Limit Duration	$I_{OUT} = I_{LIM}$	**9.2**	12	**15**	ms
t_{RTY}	Automatic Retry Period		**0.80**	1	**1.35**	s
I/O PARAMETERS						
Vfault_lo	Fault Output Voltage	Fault I_{OUT} = 10mA	-	-	**0.45**	V
Ifault	Fault Leakage		-	5	-	µA
Venr_5	ENABLE/$\overline{\text{ENABLE}}$ Rising Threshold	V_{IN} = 5V	**1.5**	1.8	**2**	V
Hys_Venr_5	EN/$\overline{\text{EN}}$ Threshold Hysteresis	V_{IN} = 5V	**65**	140	**175**	mV
Venr_3	ENABLE/$\overline{\text{ENABLE}}$ Rising Threshold	V_{IN} = 3.3V	**1.0**	1.3	**1.6**	V
Hys_Venr_3	EN/$\overline{\text{EN}}$ Threshold Hysteresis	V_{IN} = 3.3V	**30**	80	**120**	mV
Venr_2	ENABLE/$\overline{\text{ENABLE}}$ Rising Threshold	V_{IN} = 2.5V	**0.95**	1.1	**1.3**	V
Hys_Venr_2	EN/$\overline{\text{EN}}$ Threshold Hysteresis	V_{IN} = 2.5V	**10**	70	**110**	mV

Electrical Specifications V_{IN} = 5V, T_A = T_J, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Ren_h	ENABLE Pull-Down Resistor	Enable asserted high options	**0.6**	1	**1.55**	MΩ
Ren_l	$\overline{\text{ENABLE}}$ Pull-Up Resistor	Enable asserted low options	**0.6**	1	**1.55**	MΩ
t_{ON}	Enable to Output Turn-on Time	R_L = 10Ω, C_L = 10µF, Enable 50% to Output 90%	-	0.1	-	ms
t_{OFF}	Enable to Output Turn-off Time	R_L = 10Ω, C_L = 10µF, Enable 50% to Output 10%	-	0.25	-	ms
t_{pdPGr}	Enable to Power Good Output Rising Time	Disable to Power-Good De-assert	-	30	-	ns
PG Vth	Power Good Threshold	PGD pulls low when V_{OUT}/V_{IN}	**88**	91	**95**	%
PGN Vth	Power Not Good Threshold	PGD release high when V_{OUT}/V_{IN}	**78**	86	**93**	%
$t_{Vthr2PG}$	PG Vth to $\overline{\text{PG}}$ Falling	$\overline{\text{PG}}$ delay after PG Vth	-	1.5	-	µs
$t_{Vthf2PG}$	PGN Vth to $\overline{\text{PG}}$ Rising	$\overline{\text{PG}}$ delay after PGN Vth	**-**	45	**-**	µs
BIAS PARAMETERS						
I_{VDD}	Enabled V_{IN} Current	Switches Closed, OUTPUT = OPEN	-	57	**75**	µA
I_{VDD}	Disabled V_{IN} Current	Switches Open, OUTPUT = OPEN	-	3.5	**5.5**	µA
V_{UVLO}	Rising POR Threshold	V_{IN} Rising to functional operation	**-**	2.1	**2.3**	V
I_{VR}	Reverse Blocking Leakage Current	V_{IN} = 0V, V_{OUT} = 5V	-	0.3	**2.0**	µA
Temp_dis	Over-Temperature Disable		-	150	-	°C
Temp_hys	Over-Temperature Hysteresis		-	20	-	°C

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Introduction

The ISL6186 is a single channel overcurrent (OC) fault protection IC for the +2.5V to +5V environment. Each ISL6186 has a 45mΩ P-channel MOSFET power switch for power control. An enabling input and fault reporting output compatible with 2.5V to 5V logic allows for external control and reporting. This device features an integrated power switch with current monitoring, accurate current limiting, reverse bias protection, and current limited timed delay to turn-off for system reliability. See Figures 11 through 27 for typical operational waveforms including both undercurrent and overcurrent situations.

The ISL6186 offers current sense and limiting with V_{IN} = 5V to guarantee continuous current levels of 1.5A, 3A and 3.6A, making these devices well suited for a myriad of USB and other low-power (18W max) port power management applications and configurations.

The ISL6186 also provides thermally insensitive timed OC turn-off and fault notification, isolating and protecting the voltage bus in the event of a peripheral OC or short circuit independent of the ambient thermal condition.

The ISL6186 undervoltage lockout feature prevents turn-on of the output unless the correct ENABLE state and V_{IN} > V_{UVLO} are present. During initial turn-on, the ISL6186 prevents false fault reporting by blanking the fault signal.

During operation, once an OC condition is detected, the output is current limited for t_{CL} to allow transient OC conditions to pass. If still in current limit after the current limit period has elapsed, the output is then turned off and the fault is reported by pulling the $\overline{\text{FAULT}}$ output low. On the latch-off options, after turn-off, both the output and the $\overline{\text{FAULT}}$ signal are latched low until reset by the enable signal being de-asserted or a POR occurring. At this time, the $\overline{\text{FAULT}}$ signal will clear and the switch is ready to be turned back on. On the auto restart options, the ISL6186 will attempt to periodically turn on the output as long as the enable is asserted.

When disabled, the ISL6186 has a low quiescent supply current and output to input reverse current flow blocking capability.

The ISL6186 family is provided with enable polarity options and an industry standard 8 Ld SOIC pinout along with two versions in the 70% smaller 3x3 DFN. The 8 Ld DFN package offers the same performance as the 8 Ld SOIC whereas the 10 Ld DFN offers higher current capability in the smallest possible package due to its lower package electrical and thermal resistance. Additionally, the 10 Ld DFN has a Power-Good output $\overline{\text{PGD}}$ that pulls low 40ms after V_{OUT}>90% of V_{IN} and rises after V_{OUT}< 85% of V_{IN}.

Functional Description

Power On Reset (POR)

The ISL6186 POR feature inhibits device functionality when V_{IN} <V_{UVLO}.

Reverse Polarity Protection

In any event in which the power switch is disabled or powered down, and $V_{OUT} > V_{IN}$, there will be no output to input current flow, nor will the output voltage appear on the input.

Soft-Start

Upon enable, the voltage on the VOUT pin will ramp up according to the equation: I_{LIM}/C_{OUT} (V/s). Resistive or active load will slow the V_{OUT} ramp-up toward the top of its curve.

Fault Blanking On Start-Up

During initial turn-on, the ISL6186 prevents nuisance faults being reported to the system controller by blanking the fault signal until the internal FET is fully enhanced.

Current Trip and Limiting Levels

The ISL6186 provides integrated current sensing in the MOSFET, which allows for rapid control of OC events. Once an OC condition is detected, the ISL6186 goes into its current limiting (CL) control mode. The ISL6186 is variant specified to allow a continuous current (I_{CONT}) operation of 1.5A, 3A or 3.6A. As the current increases past its continuous current rating, it will reach a level that causes the device to enter its current limit mode; that is, the current trip level. The current trip level is in all cases adequately above the I_{CONT} rating so as not to cause unintended false faults. The current limit is specified at $V_{OUT} = V_{IN}$ - 1V to test a known representative condition and is featured at a nominal value slightly higher than the continuous current rating. The speed of this current limiting control is inversely related to the magnitude of the OC fault. Thus, a hard overcurrent is more quickly pulled to its limiting value than a marginal OC condition.

Over-Temperature Shutdown

Although the ISL6186 has an over-temperature shutdown and lockout feature because of the 12ms timed shutdown, the thermal shutdown is likely only to be invoked in extremely high ambient temperatures. $\overline{FAULT}$ does not respond to OT events.

The over- temperature protection invokes and disables the switch turn-on operation. Once the die temperature is ~+140°C, it will turn off an already on switch at ~+150°C and releases the part to operation once the die temperature falls to ~+120°C.

Turn-off Time Delay

During operation, once an OC condition is detected, the output is current limited for ~12ms to allow transient OC conditions to pass. If still in current limit and after the current limit period has elapsed, the output is then turned off, and the fault is reported by pulling the $\overline{FAULT}$ output low. The internal 12ms timer starts upon current limiting and is independent of ambient or IC thermal conditions, thus providing more consistent operation over the entire temperature range.

Latch-off Restart/Auto-Restart Start

After turn-off, with the latch-off options, both the output and the $\overline{FAULT}$ signal are latched low until reset by the enable signal being de-asserted, at which time the $\overline{FAULT}$ signal will clear and the IC is ready for enable to assert. On the auto-restart options, the ISL6186 will attempt to periodically turn on the output at approximately 1s intervals as long as the enable is asserted. If the OC condition remains indefinitely, so will the fault indication and the restart attempts, until such time as the thermal protection feature is invoked, thus increasing the restart period.

Power-Good Output

This feature is an active low, open-drain, power-good indicator that asserts after V_{OUT}/V_{IN}>90% and de-asserts when V_{OUT}/V_{IN} < 85%. It immediately de-asserts upon the IC being disabled.

Active Output Pull-down

Another ISL6186 feature is the 10kΩ active pull-down on the outputs to <60mV above GND when the device is disabled, thus ensuring discharge of the load.

Typical Performance Curves

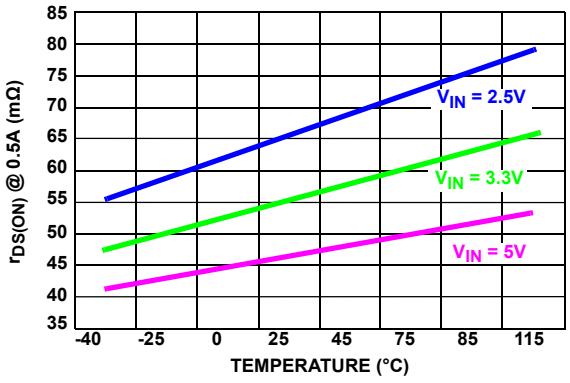


FIGURE 3. SWITCH ON-RESISTANCE AT 0.5A

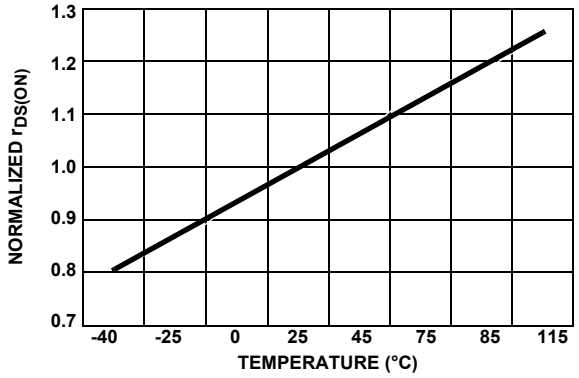


FIGURE 4. NORMALIZED SWITCH RESISTANCE

Typical Performance Curves (Continued)

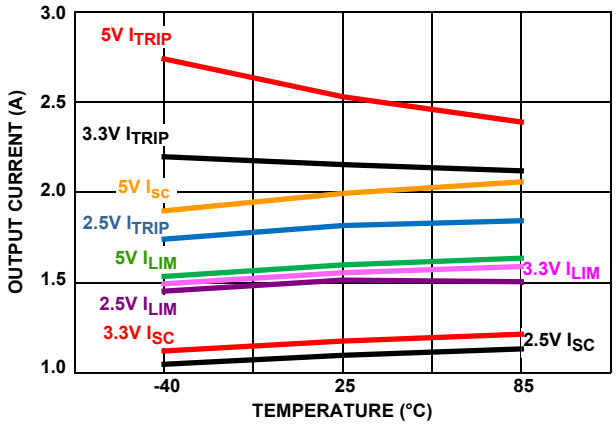


FIGURE 5. 1.5A CONTINUOUS CURRENT CHARACTERISTICS

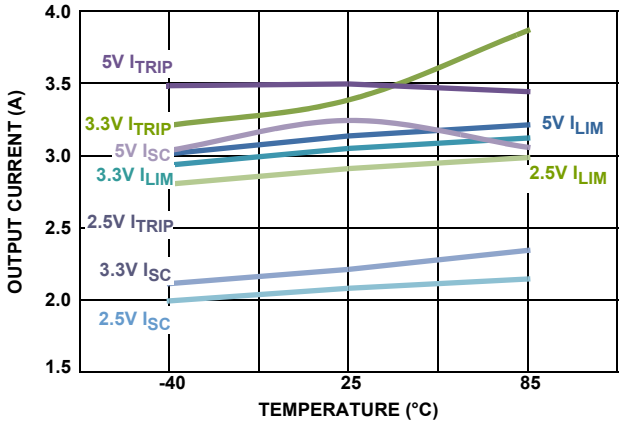


FIGURE 6. 3A CONTINUOUS CURRENT CHARACTERISTICS

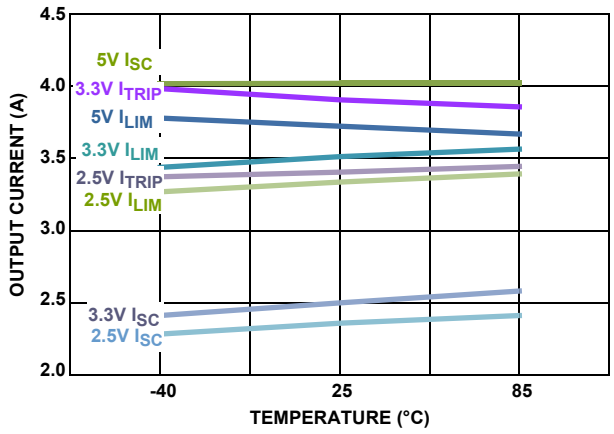


FIGURE 7. 3.6A CONTINUOUS CURRENT CHARACTERISTICS

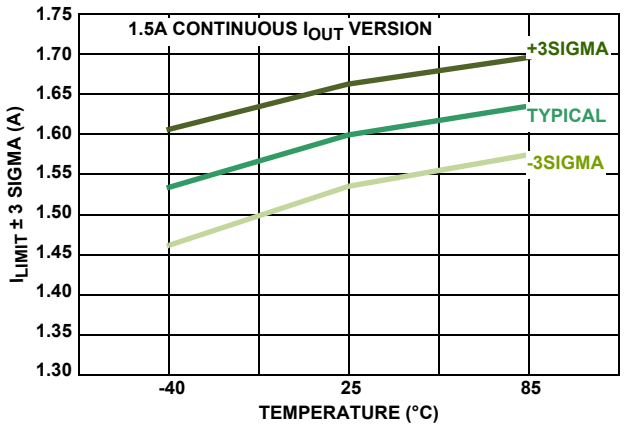


FIGURE 8. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V.

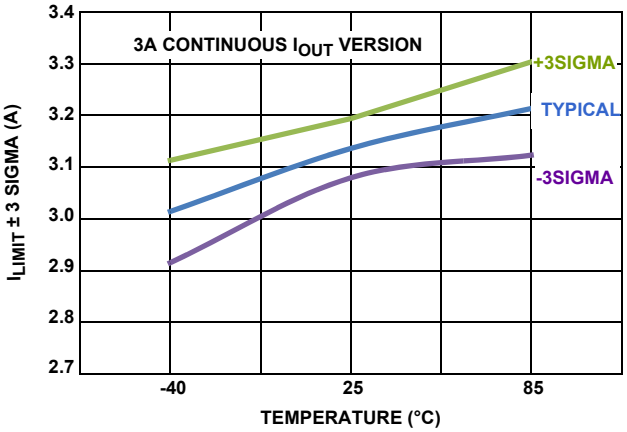


FIGURE 9. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V

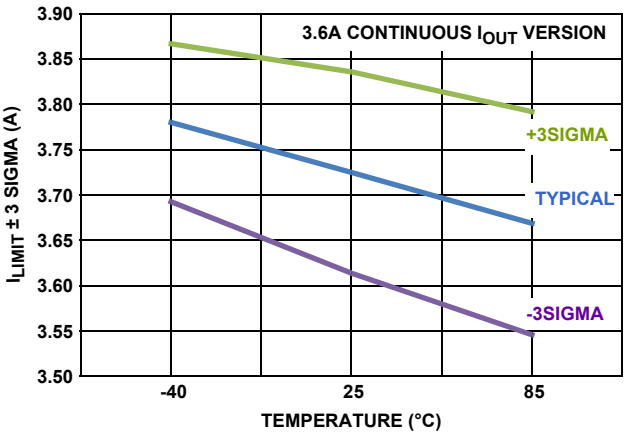


FIGURE 10. LIMITING CURRENT ±3 SIGMA, V_{IN} = 5V

Typical Performance Curves (Continued)

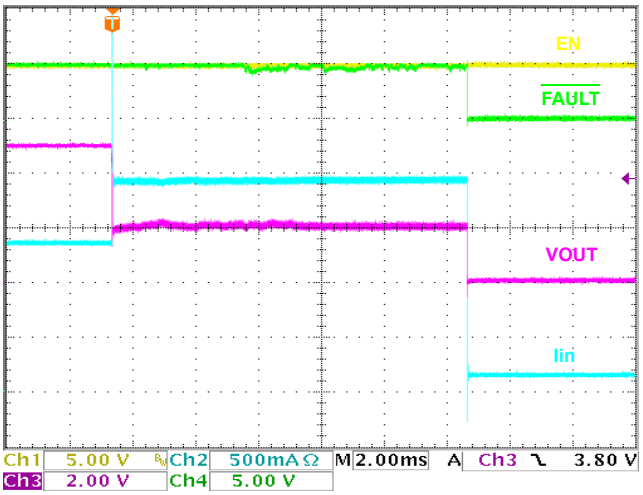


FIGURE 11. 1.5A VARIANT I_{LIM} WAVEFORM

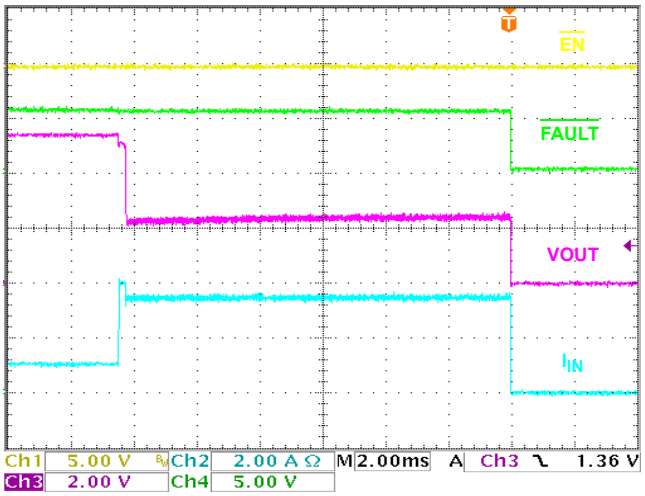


FIGURE 12. 3A VARIANT I_{LIM} WAVEFORM

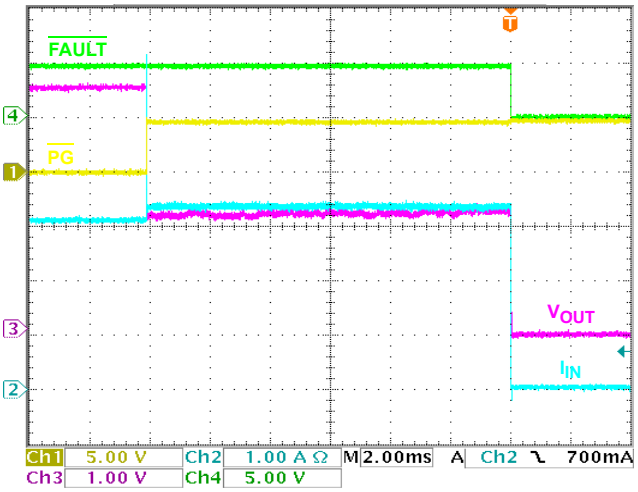


FIGURE 13. 3.6A VARIANT I_{LIM} WAVEFORM w PG

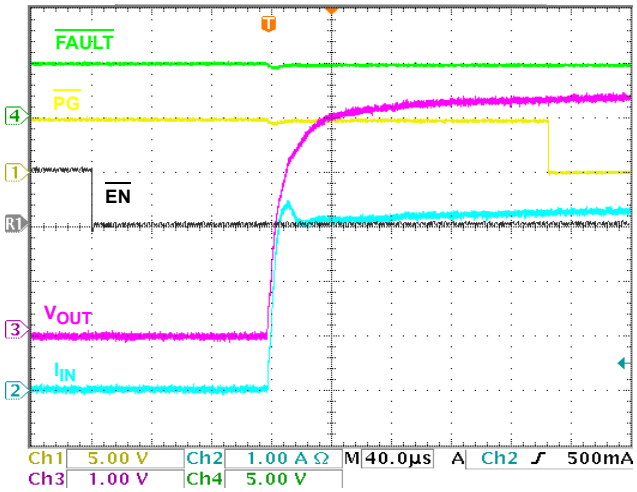


FIGURE 14. LISL6186 TURN-ON w PG

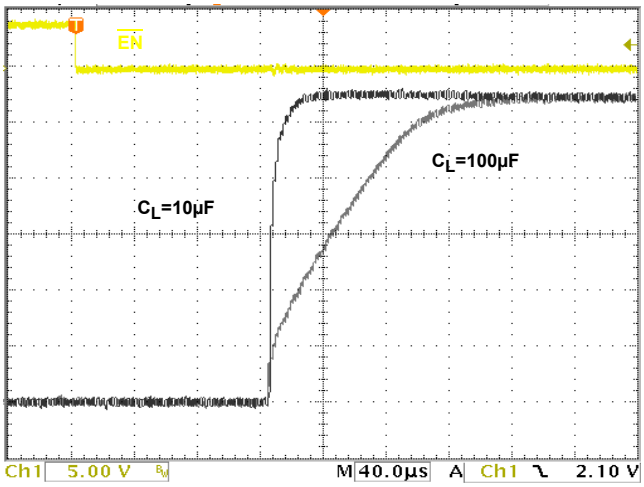


FIGURE 15. V_{OUT} TURN-ON/RISE TIME vs C_{LOAD}. V_{IN} = 5.5V, R_L = 10Ω

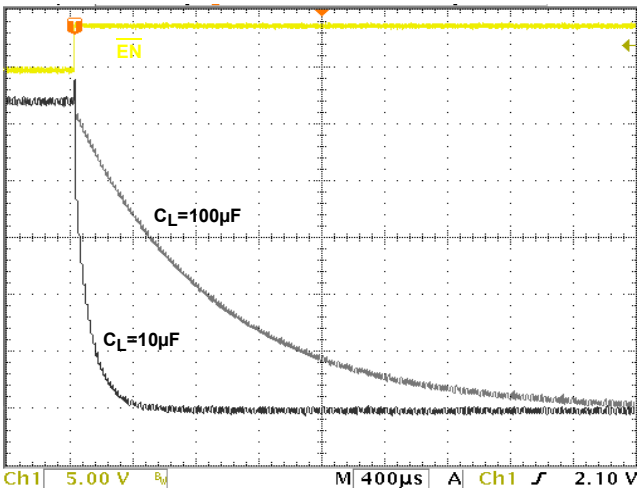


FIGURE 16. V_{OUT} TURN-OFF/FALL TIME vs C_{LOAD}. V_{IN} = 5.5V, R_L = 10Ω

Typical Performance Curves (Continued)

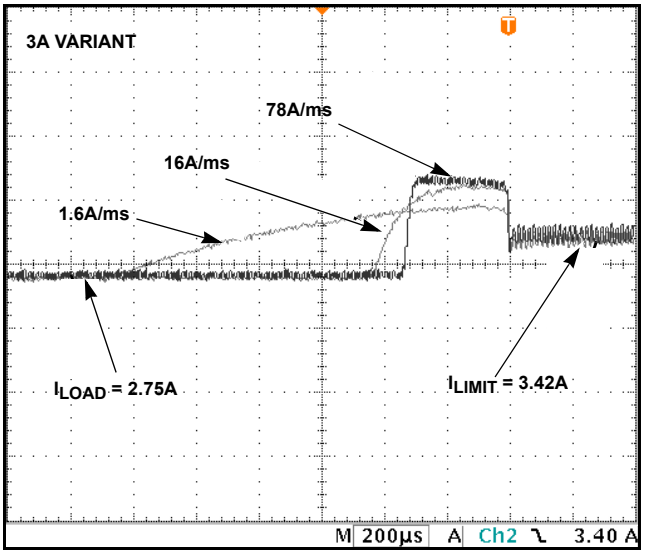


FIGURE 17. OC RAMP RATE I_{LIM} WAVEFORMS

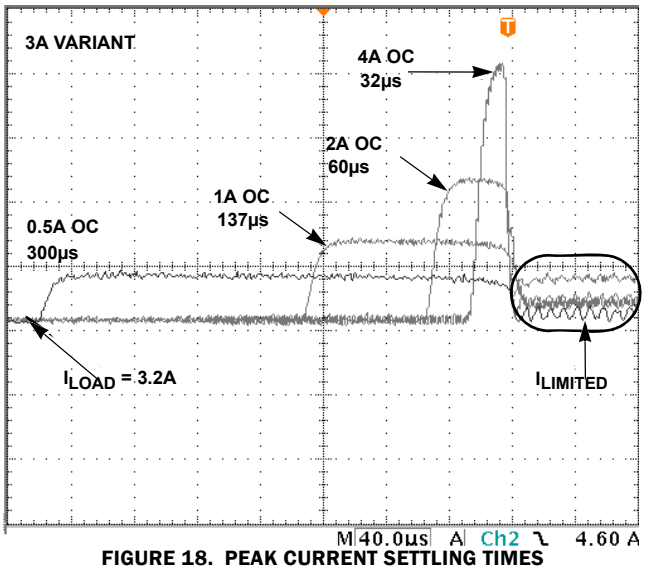


FIGURE 18. PEAK CURRENT SETTLING TIMES

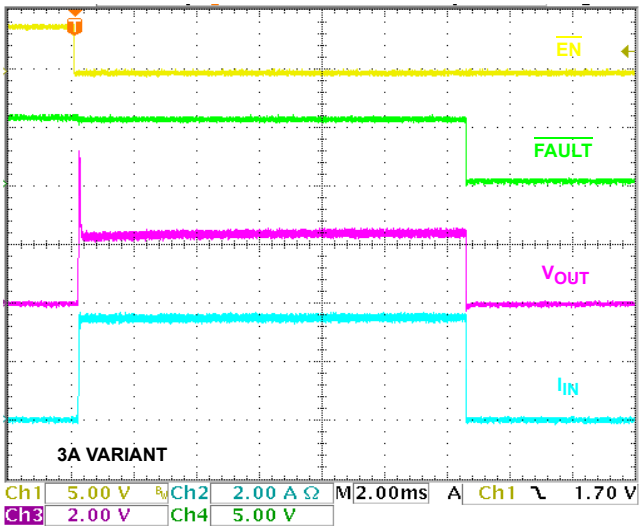


FIGURE 19. TURN-ON INTO AN OVERCURRENT

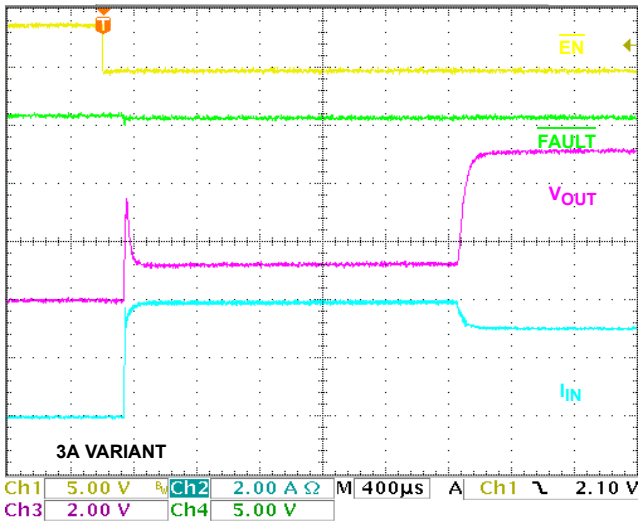


FIGURE 20. TURN-ON INTO MOMENTARY OC

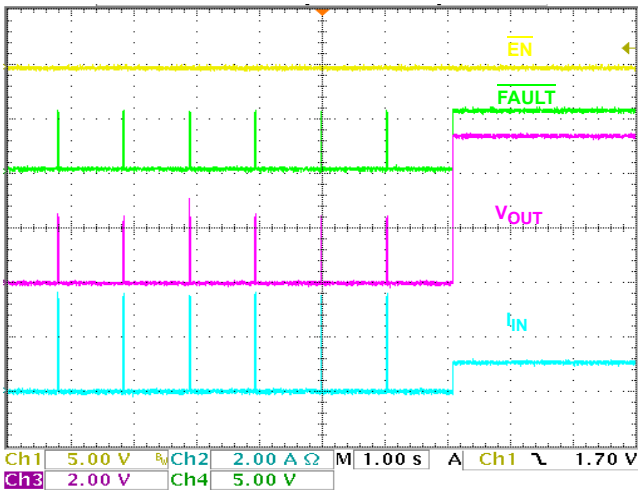


FIGURE 21. OVERCURRENT RETRY FUNCTION

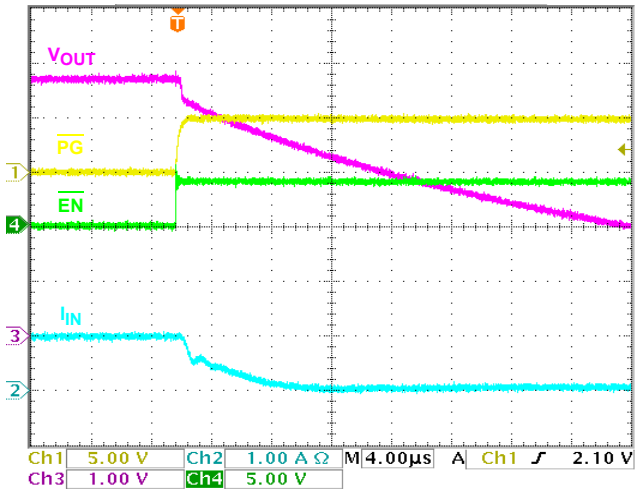


FIGURE 22. TURN-OFF w $\overline{PG}$

Typical Performance Curves (Continued)

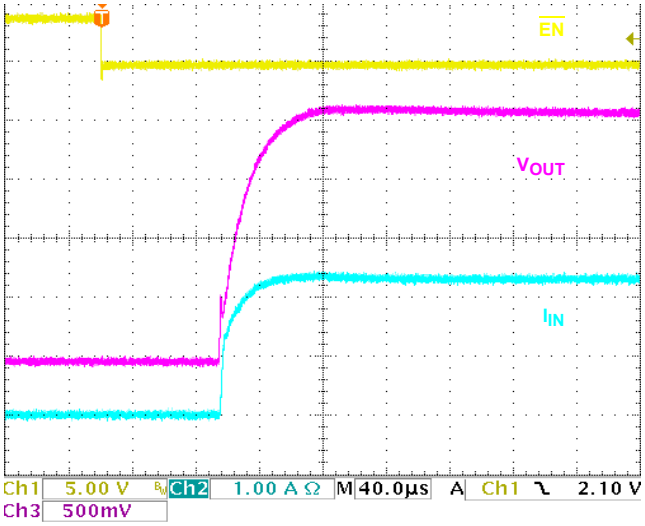


FIGURE 23. V_{IN} = 2.4V TURN-ON INTO 0.88Ω

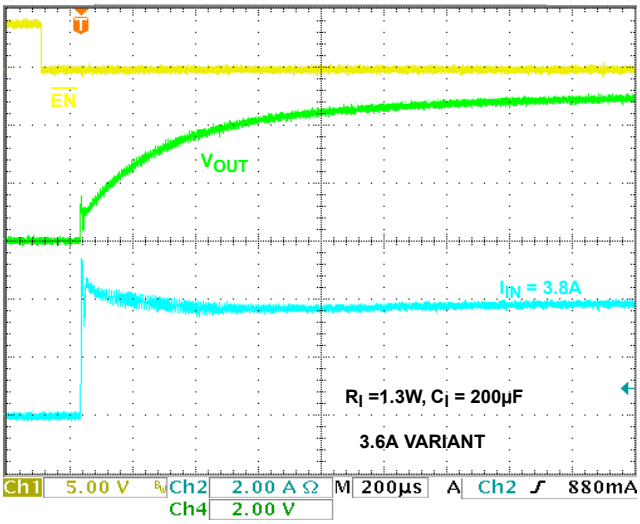
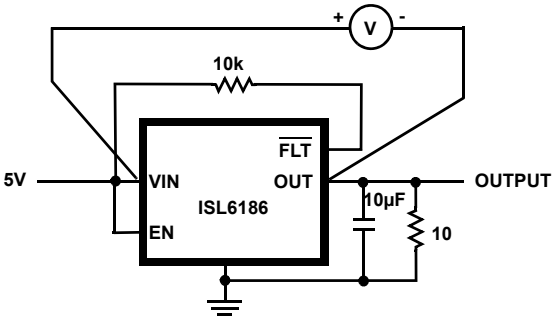


FIGURE 24. TURN-ON INTO TO 18WLOAD

Test Circuits



$r_{DS(ON)} = V/(V_{OUT}/10\Omega)$

FIGURE 25A. $r_{DS(ON)}$

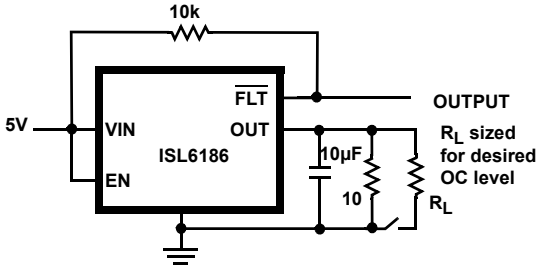


FIGURE 25B. CURRENT LIMITING

FIGURE 25. DC TEST CIRCUIT

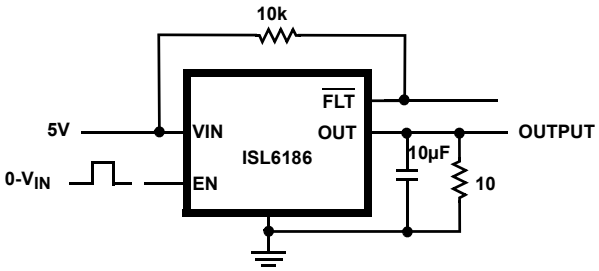


FIGURE 26A. TRANSIENT TEST CIRCUIT

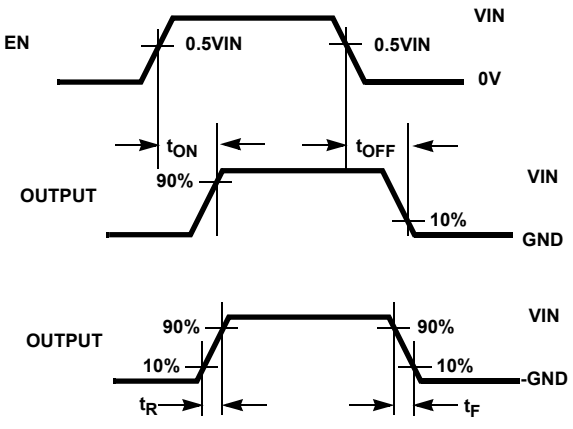
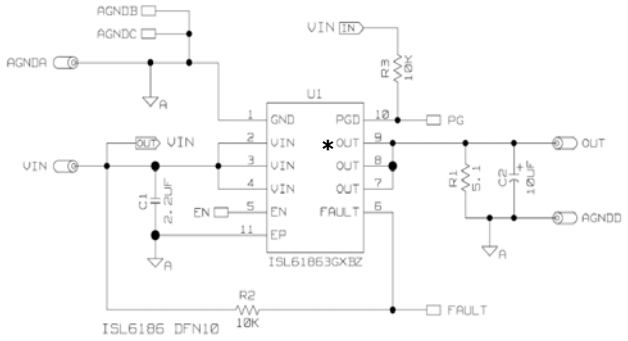


FIGURE 27. TRANSIENT WAVEFORM MEASUREMENT POINTS

ISL61863EVAL1Z Schematic and Photo



NOTE: *PGD Output only available on ISL61863 types

FIGURE 28A. ISL61863EVAL1Z SCHEMATIC

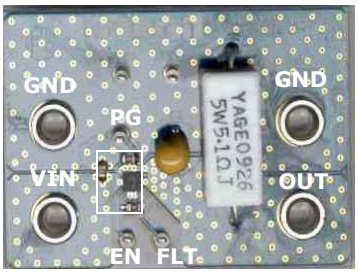


FIGURE 28B. ISL61863EVAL1Z BOARD PHOTO

FIGURE 28. ISL61863EVAL1Z SCHEMATIC and ISL61863EVAL1Z PHOTOGRAPH

Application Information

Using the ISL6186EVAL1Z Platform General and Biasing Information

There are three evaluation platforms for the ISL6186 family. There is one for each package style, each with a different continuous output current level and representing a mix of enable polarity and output retry or latch options. The standard available evaluation board options are listed at the end of the Ordering Information table, which starts on page 3. Figure 28A illustrates the schematic for the 10 Ld DFN ISL61863EVAL1Z. Other than the unique PGOOD output on the ISL61863 types, all the schematics and functions are the same across all three package types. Consult the individual package pinouts on page 2 for those differences.

The evaluation platform is biased and monitored through a few labeled test points. See Table 1 for test point assignments and descriptions.

TABLE 1. ISL61863EVAL1Z TEST POINT ASSIGNMENTS

TP NAME	DESCRIPTION
GND	Eval Board and IC Gnd
VIN	Eval Board, IC Bias and Power Input
EN	Enable Switch
OUT	Switch Power Output
PG	Power-Good Output
FLT	Fault Output

Upon proper bias of the evaluation platform and correct enabling of the IC, the ISL6186 will have a nominal $V_{IN}/5.1\Omega$ load current that is below the continuous current rating passing through each enabled switch. See Figures 14 to 16 for typical ISL6186 turn-on and turn-off waveforms.

External current loading in excess of the trip current level for the particular part being evaluated will result in the ISL6186 entering current limiting mode. Figure 11 illustrates current limiting mode for the ISL6186 product variants with 1.5A of continuous load current rating. The scope shot shows current limiting for ~12ms before it is turned off and the fault signal is asserted.

Application Considerations

See Table 2 for a listing of ISL6186XEVAL1Z board components.

Decoupling V_{IN}

Application considerations for the ISL6186 family are widely accepted best industry practices. Good decoupling practices on the V_{IN} pin must be followed by placement close to the IC, with at least 2.2µF being recommended. For the 3.0 and 3.6A versions, at least 33µF is recommended to prevent spiking and glitching on V_{IN} during an OC event. Use good PCB layout practices to reduce input and output inductance to the ISL6186.

Loading V_{OUT}

When designing with the 3A and 3.6A versions in an implementation in which the output may be unloaded (open) while the ISL6186 is turned on, a minimum of 4.7µF of capacitive loading is recommended to prevent high dv/dt from unnecessarily activating the surge/ESD circuitry.

Continuous Current Ratings

The ISL6186 provides several continuous current rated devices specified at V_{IN} = 5V: these are the 1.5A, 3A and 3.6A options, which are capable over the entire temperature extreme. At V_{IN} = 3.3V, current capability is degraded, and the ISL6186 is specified at 1.5A and 3A. At V_{IN} = 2.5V, there are no specifications, but a typical value is provided in the specification table as guidance for +25°C operation. This degraded capability is due to the higher $r_{DS(ON)}$ of the FET switch at the lower bias voltage.

Enhanced thermal characteristics and an increased number of bond wires allows the 10 Ld DFN to have a higher current capability than either the 8 Ld SOIC or 8 Ld DFN.

TABLE 2. ISL6186XEVAL1Z BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6186	Intersil, ISL6186
R1	Output Load Resistor	5.1Ω, 5%, 3W
R2	FLT Output Pull-up Resistor	10kΩ, 0805
R3 * only on ISL61863EVAL1Z	PGD Output Pull-up Resistor	10kΩ, 0805
C1	Decoupling Capacitor	2.2µF on ISL61862EVAL1Z 33µF on ISL61861EVAL1Z and ISL61863EVAL1Z
C2	Load Capacitor	10µF 16V Electrolytic, Radial Lead

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
9/1/11	FN7698.1	Initial release to web.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL6186

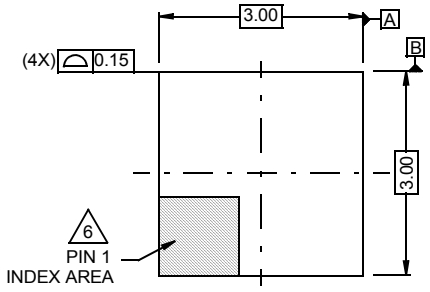
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

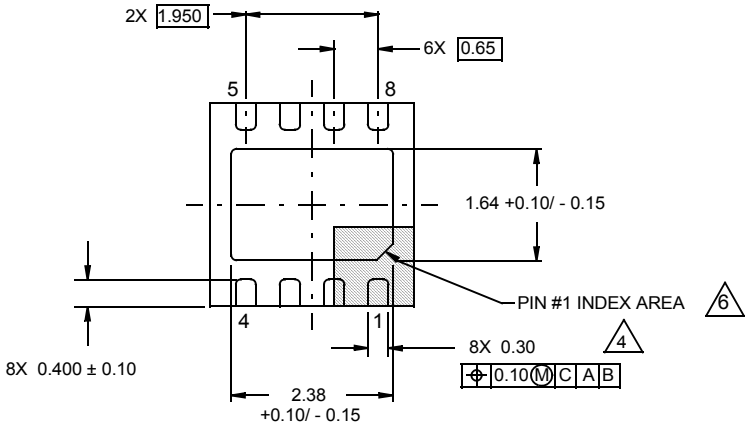
Package Outline Drawing
L8.3x3J

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

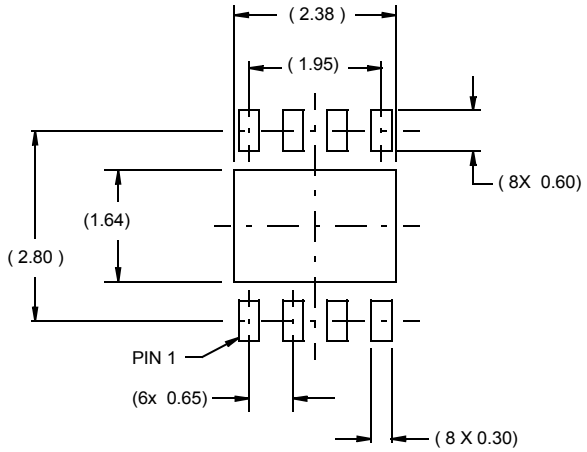
Rev 0 9/09



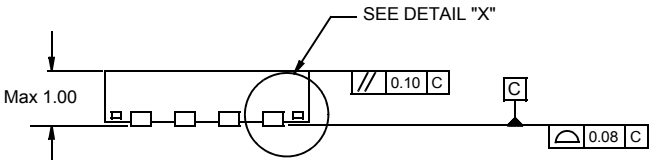
TOP VIEW



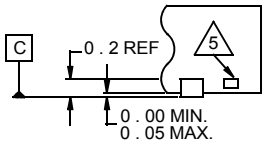
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

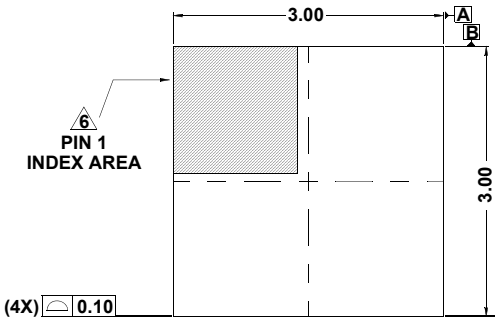
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

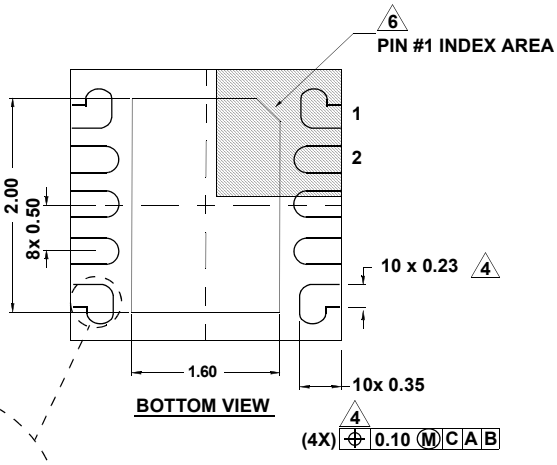
L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

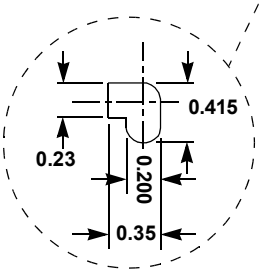
Rev 6, 09/09

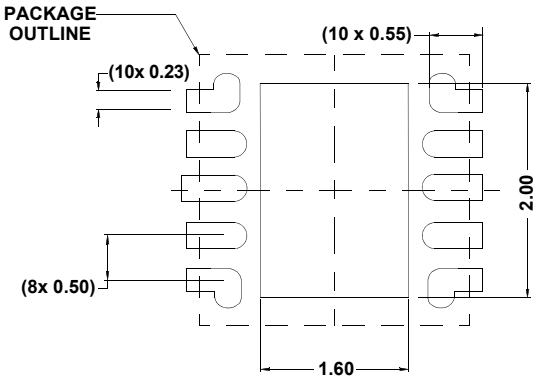


TOP VIEW

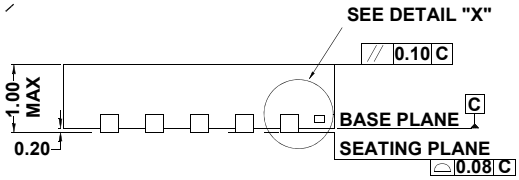


BOTTOM VIEW

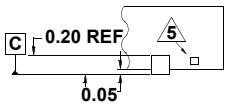




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

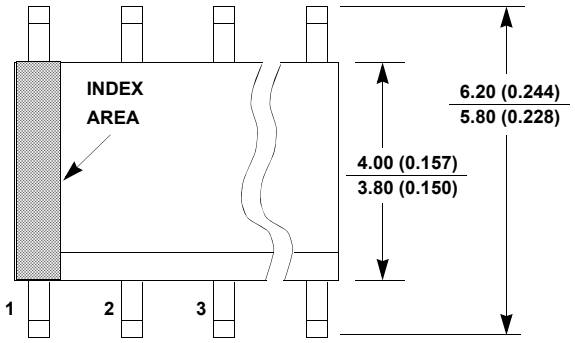
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Package Outline Drawing

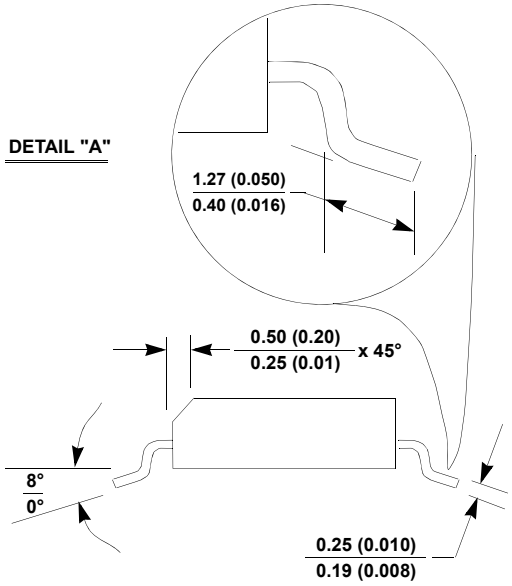
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

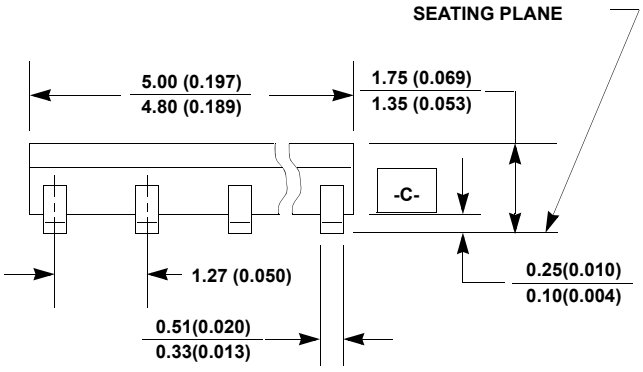
Rev 3, 3/11



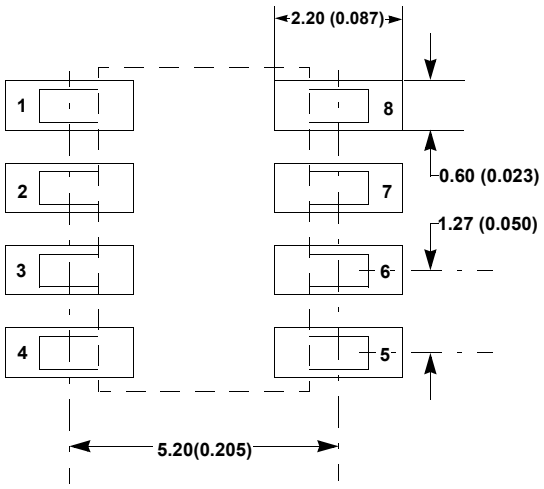
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.