T-51-10-12

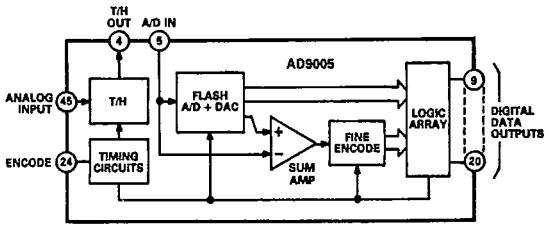
12-Bit, 10MSPS A/D Converter

AD9005

FEATURES
- Complete 12-Bit A/D Converter
- Includes Track and Hold, Reference and Timing
- Bipolar Analog Input (±1.024V)
- Up to 10MSPS Sampling Rate
- Low Power Dissipation: 3.1W
- Low Harmonic Distortion

APPLICATIONS
- Radar
- Digital Oscilloscopes
- Electro-Optics
- Medical Scanners
- Communication/Signal Intelligence

AD9005 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD9005 is a complete 12-bit A/D converter featuring on-board track-and-hold amplifier, voltage reference and timing circuitry. Featuring sampling rates from dc to 10MSPS, the AD9005 uses a subranging converter architecture to achieve high speed and high resolution. Dynamic performance includes a SNR of 64dB and harmonic distortion of −72dBc with a 4.3MHz analog input.

Critical to this performance is the use of advanced bipolar integrated circuits, custom designed for the AD9005 and manufactured by Analog Devices. The AD9005 is TTL compatible with offset binary outputs. It is available in a 46-pin hermetic metal DIP in two temperature ranges: 0 to +70°C commercial range and −55°C to +125°C military range (case temperature).

ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9005KM	0 to +70°C	46-Pin DIP	M-46
AD9005TM	−55°C to +125°C	46-Pin DIP	M-46

*See Section 14 for package outline information.

SPECIFICATIONS

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ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_{CC}$) . . . . . +18V
Negative Supply Voltage ($-V_{EE}$) . . . . . −18V
Positive Supply Voltage ($+V_S$) . . . . . +6V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Analog Input Voltage (Pin 45) . . . . . ±3.0V dc
Digital Input Voltage . . . . . −0.5V to $+V_S$
Digital Output Current 4mA

Operating Temperature Range (Case)
AD9005KM . . . . . 0 to +70°C
AD9005TM . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +165°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($+V_{CC}$ = +15V, $-V_{EE}$ = −15V, $+V_S$ = +5V, $-V_S$ = −5.2V, unless otherwise stated)

Parameter	Temp	Test Level	AD9005KM Min	AD9005KM Typ	AD9005KM Max	AD9005TM Min	AD9005TM Typ	AD9005TM Max	Units
RESOLUTION	Full	I	12			12			Bits
LSB Weight	Full	V		0.5			0.5		mV
STATIC ACCURACY									
Differential Nonlinearity	+25°C	I	−0.75	±0.5	+0.75	−0.75	±0.5	+0.75	LSB
	Full	VI	−1.0		+1.0	−1.0		+1.25	LSB
Integral Nonlinearity	+25°C	I		±1.0	±2.25		±1.0	±2.25	LSB
	Full	VI			±2.5			±2.75	LSB
No Missing Codes	Full	VI		GUARANTEED			GUARANTEED		
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.0			±2.0	% FS
Offset Error	+25°C	I		±4	±15		±4	±15	mV
	Full	VI			±30			±40	mV
ANALOG INPUT									
Input Voltage Range	Full	V		±1.024			±1.024		V p-p
Input Resistance	Full	VI	950	1000	1050	950	1000	1050	Ω
Input Capacitance	+25°C	V		5			5		pF
Large Signal Input Bandwidth[3]	Full	V		38			38		MHz
DYNAMIC CHARACTERISTICS[5]									
Maximum Conversion Rate	Full	I	10			10			MSPS
Output Data Delay[6,9] (t_{PD})	+25°C	V		90			90		ns
Aperture Delay	+25°C	V		5			5		ns
Aperture Uncertainty	+25°C	IV		10	20		10	20	ps rms
Transient Response (to ±1LSB)[7]	+25°C	IV			120			120	ns
Overvoltage Recovery Time[8] (to ±1LSB)	+25°C	IV			250			250	ns
In-Band Harmonics[10,4]									
F_{IN} = 540kHz	+25°C	IV	−70	−75		−69	−75		dBc
F_{IN} = 2.3MHz	+25°C	I	−68	−72		−67	−72		dBc
	Full	VI	−67			−66			dBc
F_{IN} = 4.3MHz	+25°C	I	−66	−72		−66	−72		dBc
	Full	VI	−65			−63			dBc
Signal to Noise Ratio[11,4]									
F_{IN} = 540kHz	+25°C	IV	65	67		64	67		dB
F_{IN} = 2.3MHz	+25°C	I	63	65		63	65		dB
	Full	VI	63			60			dB
F_{IN} = 4.3MHz	+25°C	I	62	64		62	64		dB
	Full	VI	61			60			
Two-Tone Intermodulation Distortion[12]									
F_{IN} = 2.2MHz+2.3MHz	+25°C	V		−74			−74		dBc

Parameter	Temp	Test Level	AD9005KM Min	AD9005KM Typ	AD9005KM Max	AD9005TM Min	AD9005TM Typ	AD9005TM Max	Units
ENCODE INPUT[14]									
Logic "1" Voltage	Full	IV	2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8	V
Logic "1" Current	Full	IV			150			150	μA
Logic "0" Current	Full	IV			150			150	μA
Input Capacitance	+25°C	V		5			5		pF
Encode Pulse Width (High)	+25°C	IV	25			25			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (2mA Source)	Full	IV	2.4			2.4			V
Logic "0" Voltage (4mA Sink)	Full	IV			0.4			0.4	V
Logic Coding	Full	IV		Offset Binary			Offset Binary		
POWER SUPPLY									
Supply Voltage $+V_{CC}$	Full	VI	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	V
Supply Current $+V_{CC}$	Full	VI		33	40		23	25	mA
Supply Voltage $-V_{EE}$	Full	VI	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	V
Supply Current $-V_{EE}$	Full	VI		55	70		45	55	mA
Supply Voltage $+V_S$	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply Current Analog $+V_S$	Full	VI		124	140		124	140	mA
Supply Current Digital $+V_S$	Full	VI		55	110		55	110	mA
Supply Voltage $-V_S$	Full	VI	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
Supply Current Analog $-V_S$	Full	VI		160	185		160	185	mA
Supply Current Digital $-V_S$	Full	VI		73	115		73	115	mA
Nominal Power Dissipation	Full	VI		3.1	4.1		3.1	4.1	W
PSRR[13, 15]	+25°C	I		0.01	0.02		0.01	0.02	%/%

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NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute rating conditions for extended periods of time may affect device reliability.

[2]Maximum junction temperature should not be allowed to exceed 165°C. Hybrid thermal model:

$t_{JUNCTION} = t_{AMBIENT} + P_{DISSIPATION} \times (\theta_{CA} + \theta_{JC})$
$= t_{CASE} + P_{DISSIPATION} \times (\theta_{JC})$

46 Pin metal DIP: θ_{CA} = 14°C/W in still air;
θ_{CA} = 6°C/W with 500LFPM air flow
θ_{JC} = 6°C/W

[3]Determined by 3dB reduction in reconstructed output.

[4]Input at 1dB below full scale.

[5]Measured at 10MHz encode rate.

[6]Measured from ENCODE in to data out for LSB only.

[7]For full-scale step input; 12-bit accuracy is attained in the specified time.

[8]Recovers to 12-bit accuracy in specified time following 200% full-scale input voltage.

[9]Excludes pipeline delay of two clock cycles (see timing diagram).

[10]Worst case spurious in-band signal relative to input level.

[11]RMS signal to RMS noise, including harmonics.

[12]Worst case spurious in-band signal relative to level of input tones, which are both −7dB below full scale.

[13]Sensitivity of full scale gain error with respect to power supply variation within supply Min/Max limits.

[14]ENCODE signal rise and fall times should be less than 5ns for normal operation. Transition from "0" to "1" initiates conversion.

[15]PSRR is tested over given voltage range.

EXPLANATION OF TEST LEVELS

Test Level I	–	100% production tested.
Test Level II	–	100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III	–	Sample tested only.
Test Level IV	–	Parameter is guaranteed by design and characterization testing.
Test Level V	–	Parameter is a typical value only.
Test Level VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices. Guaranteed, not tested, for commercial temperature range.

RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage Min	Input Voltage Nominal	Input Voltage Max
$-V_S$	−5.45	−5.2	−4.95
$+V_S$	+5.25	+5.0	+4.75
$-V_{EE}$	−15.75	−15.0	−14.25
$+V_{CC}$	+14.25	+15.0	+15.75
Analog Input	−1.024		+1.024

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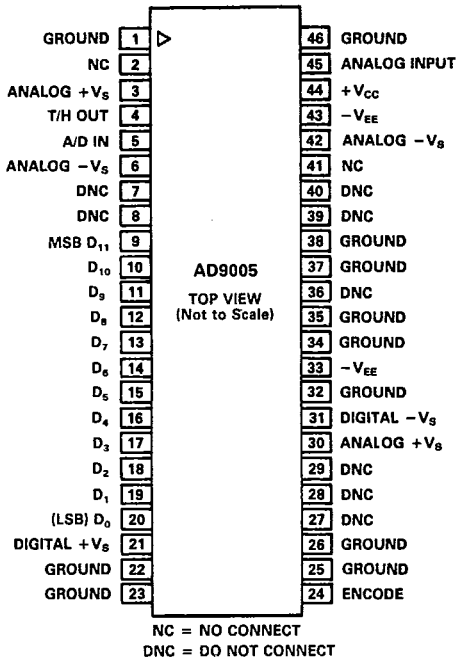
AD9005 PIN DESIGNATIONS



NC = NO CONNECT
DNC = DO NOT CONNECT

PIN DESCRIPTIONS

Pin	Name	Description
1	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
2	NC	Not internally connected.
3	ANALOG $+V_S$	Positive analog supply pin. Nominally +5V dc.
4	T/H OUT	Output of internal track-and-hold amplifier. Connect to Pin 5 for normal operation.
5	A/D IN	Input to internal A/D encoder. Connect to Pin 4 for normal operation.
6	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2V dc.
7, 8	DNC	Do not connect. Internal test point.
9	D_{11} (MSB)	Most significant bit of digital output data.
10-19	D_1-D_{10}	Digital data outputs.
20	D_0 (LSB)	Least significant bit of digital output data.

OUTPUT CODING

ANALOG INPUT	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
≥+1.024V	1	1	1	1	1	1	1	1	1	1	1	1
≤−1.024V	0	0	0	0	0	0	0	0	0	0	0	0

21	DIGITAL $+V_S$	Positive digital supply pin. Nominally +5V dc.
22, 23	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
24	ENCODE	Convert command. TTL compatible, rising edge triggered.
25, 26	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
27-29	DNC	Do not connect. Internal test point.
30	ANALOG $+V_S$	Positive analog supply pin. Nominally +5V dc.
31	DIGITAL $-V_S$	Negative digital supply pin. Nominally −5.2V dc.
32	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
33	$-V_{EE}$	Negative analog supply pin. Nominally −15V dc.
34, 35	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
36	DNC	Do not connect. Internal test point.
37, 38	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
39, 40	DNC	Do not connect. Internal test point.
41	NC	Not internally connected.
42	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2V dc.
43	$-V_{EE}$	Negative analog supply pin. Nominally −15V dc.
44	$+V_{CC}$	Positive analog supply pin. Nominally +15V dc.
45	ANALOG INPUT	Analog input. Full scale of ±1.024V.
46	GROUND	Circuit ground. All grounds should be connected together near the AD9005.

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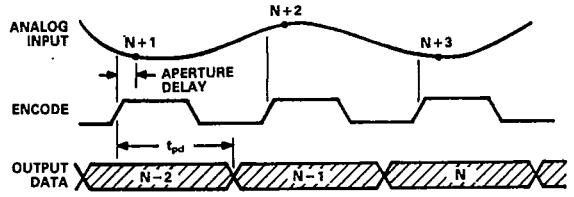
TIMING DIAGRAM



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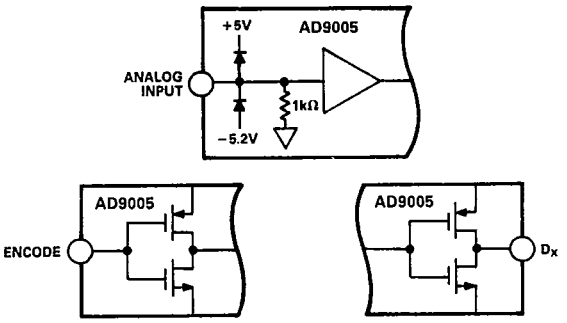
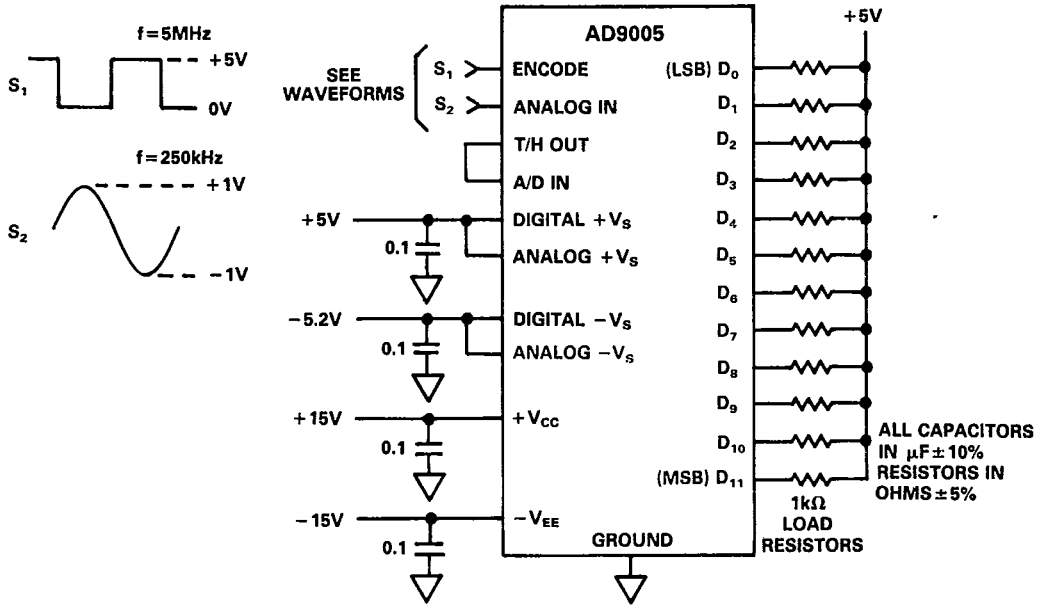
EQUIVALENT INPUT/OUTPUT CIRCUITS



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The AD9005 is a complete analog-to-digital converter. The AD9005 uses a subranging A/D architecture enhanced by hybrid technology. This includes an on-board track-and-hold amplifier, on-board references, timing circuitry and output latches.

The analog input of the AD9005 is fed directly into the internal track-and-hold amplifier, thus eliminating the need for external signal conditioning in many applications. This amplifier provides low input capacitance, and a bipolar (±1.024V) input range. Normally reverse-biased Schottky diodes on the input provide overrange protection. If the amplitude, bandwidth or dc voltage level of the analog input signal calls for external signal conditioning, it is advisable to use an amplifier with low harmonic distortion and low noise characteristics. Selection of such an amplifier is difficult because the performance of the AD9005 will likely exceed that of most commercially available amplifiers. A good choice would be the AD9610, a wideband, low noise, current feedback operational amplifier. It is important to remember that band limiting the analog input signal can avoid aliasing during the A/D conversion process.

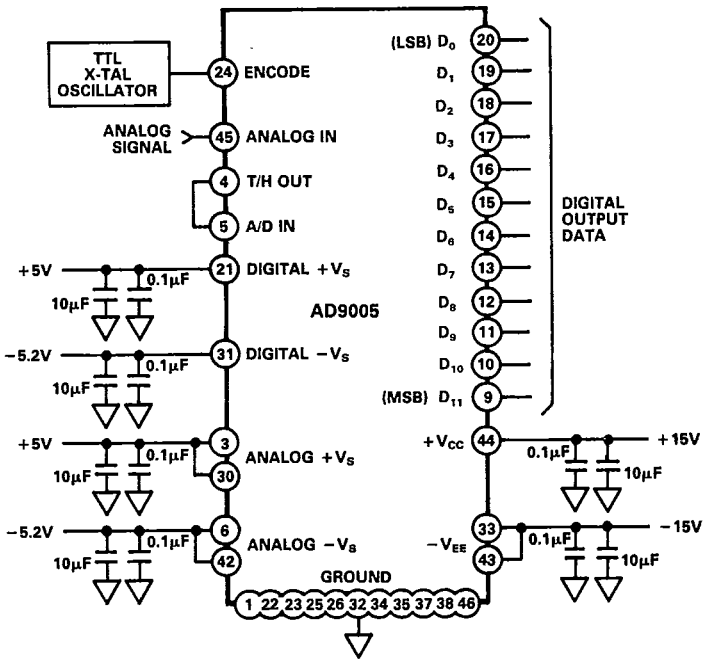
Timing in the AD9005 is critical, and careful measures must be taken to support 12-bit accuracy. One simple way to enhance the performance of the AD9005 is to synchronize the system clock to a crystal oscillator. This will minimize any clock jitter, a must for maintaining the spectral purity of analog signals near Nyquist limits. Because the conversion cycle begins with the rising edge of the encode signal, a fast, clean rising edge will also help to reduce any clock jitter. T-51-10-12

When the ENCODE signal of the AD9005 goes HIGH, the internal track-and-hold enters the hold state; after 65ns, it returns to track mode. In applications in which the AD9005 is clocked slowly or intermittently (i.e., in burst mode), the encode signal should be returned to a logic LOW state during the idle periods.

The ENCODE signal pulse width should also be adjusted so that it is in the HIGH (hold) state for a minimum of 25ns. This ensures that the T/H enters the hold mode before the A/D conversion takes place.

The AD9005 has many appealing characteristics for 12-bit A/D converter applications. Its dynamic performance is state-of-the-art in hybrid technology. Typical applications include radar, missile guidance, digital oscilloscopes, waveform analyzers, medical instrumentation, electro-optics, communications and ESM.

TYPICAL AD9005 APPLICATION



Layout Information

The accuracy of a 12-bit converter, especially one with the dynamic performance level of the AD9005, requires that designers pay careful attention to printed circuit board layouts. Analog signal paths should be impedance matched, with termination/load resistors at or near package connections. Analog signal paths should also be isolated from digital signal paths. Otherwise digital signals can be capacitively coupled into the analog section of the circuit, degrading the overall performance of the A/D converter.

Digital switching noise on power supplies can also degrade converter performance. Because of this noise (inherent with TTL logic), the digital power supplies of the AD9005 should be separated from the analog power supplies. In addition, each power supply should be capacitively decoupled to ground. To accomplish this, a single large value capacitor with a high resonant frequency (a 10μF tantalum capacitor for example) should be used on each of the AD9005's power supplies, at or near the package. In addition, a lower value capacitor with good high frequency characteristics (a 0.1μF ceramic chip capacitor is recommended) should be connected to each power supply pin connection.

For applications in which only single +5V and/or −5.2V supplies are available, a ferrite bead, placed in series between the analog and digital power pins, can be used to isolate the digital noise from the analog circuits.

Noise on the circuit ground is often the limiting factor in A/D converter performance. Perhaps the most critical concerns of circuit layout are the ground connections. To reduce ground noise, a two-sided printed circuit board is recommended, the component side being reserved (as much as possible) for a single, low impedance ground plane. The other side should be used for all (possible) power and signal connections. Each of the ground connections of the AD9005 should be connected to the ground plane, and most of the area under the AD9005 should be part of this ground plane. The metal case of the AD9005 is connected to ground.

Operation of the AD9005 requires that Pin 4, the output of the internal track-and-hold, be connected to Pin 5, the input to the AD9005's A/D converter circuitry. A suggested layout, showing this connection, is shown below.

A final suggestion regarding circuit layout concerns the use of sockets. Ideally, parts should be soldered into boards in final designs. If sockets must be used, individual pin sockets are recommended to avoid lead inductance and capacitive coupling between adjacent pins. Pin sockets are available from Amp, part #6−330808−0.

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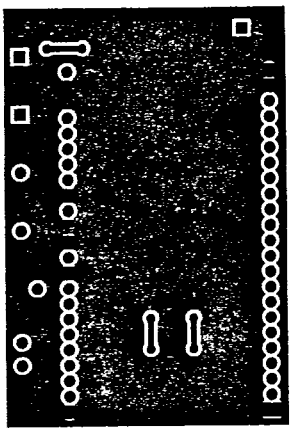
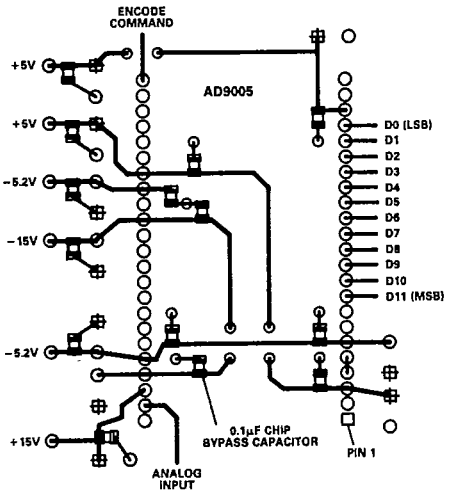
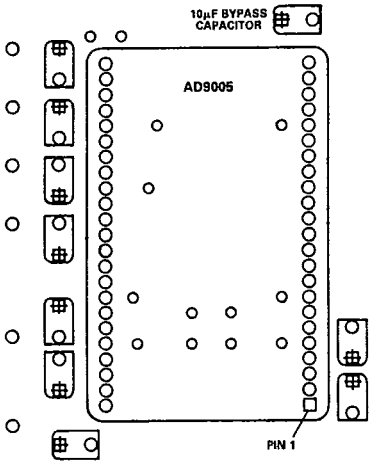
SUGGESTED LAYOUT



GND PLANE SIDE
(As Viewed from Top)



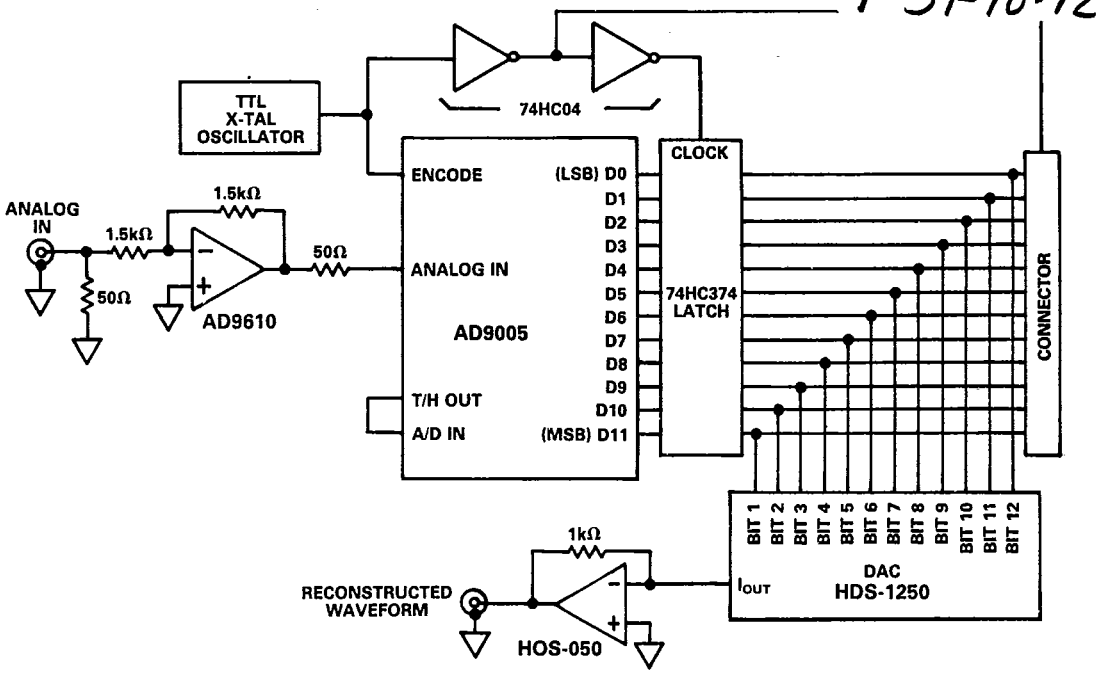
SOLDER SIDE
(As Viewed from Top)



COMPONENT MOUNTING
(As Viewed from Top)

EVALUATION CIRCUIT

T-51-10-12



Contact factory about evaluation board availability.

AD9005 DYNAMIC PERFORMANCE (@ +25°C)