3.4.3 IDLE 2 Mode

Figure 3.4 (2) shows the timing of HALT release caused by interrupts in the RUN/IDLE 2 mode.

In the IDLE 2 mode, the HALT state is released by an interrupt with the same timing as in the RUN mode, except the internal operation of the MCU. In the RUN mode, only the CPU stops executing the current instruction, and the system clock is supplied to all internal devices. In the IDLE 2 mode, however, the system clock is supplied to only specific internal I/O devices. As a result, the HALT state in the IDLE 2 mode requires only a 1/3 of the power consumed in the RUN mode. In the IDLE 2 mode, the system clock is supplied to the following I/O devices:

- 8-bit timer
- 16-bit timer
- Serial interface
- Watchdog timer

3.4.4 STOP Mode

Figure 3.4 (4) is a timing chart for releasing the HALT state by interrupts in the STOP mode.

The STOP mode is selected to stop all internal circuits including the internal oscillator. In this mode, all pins except special ones are put in the high-impedance state, independent of the internal operation of the MCU. Table 3.4 (1) summarizes the state of these pins in the STOP mode. Note, however, that the pre-halt state (The status prior to execution of HALT instruction) of all output pins can be retained by setting the internal I/O register WDMOD<DRVE> (Drive enable: Bit 0 of memory address FFD2H) to "1". The content of this register is initialized to "0" by resetting.

When the CPU accepts an interrupt request, the internal oscillator is restarted immediately. However, to get the stabilized oscillation, the system clock starts its output after the time set by the warming up counter WDMOD<WARM> (Warming up: Bit 4 of memory address FFD2H). A warming-up time of either the clock oscillation time $\times 2^{14}$ or $\times 2^{16}$ can be set by setting this bit to either "0' or "1". This bit is initialized to "0" by resetting.

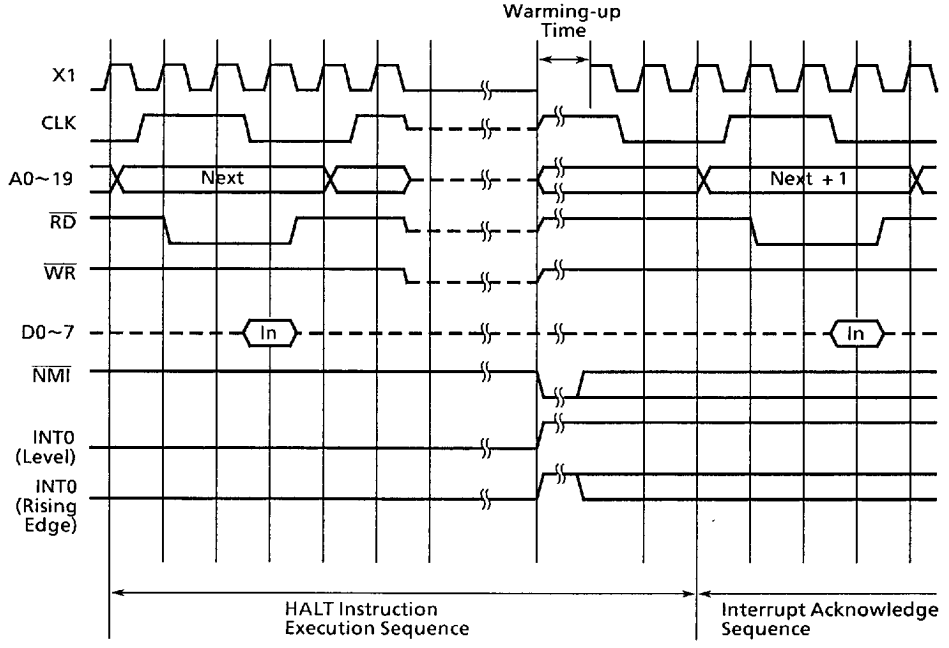

Figure 3.4 (4) Timing Chart of HALT Released by Interrupt in STOP Mode

The internal oscillator can be also restarted by the input of the $\overline{\text{RESET}}$ signal at "0" to the CPU. In the Reset restart mode, however, the warming-up counter remains inactive in order to get the quick response of MCU when the power is turned on (Power on Reset). As a result, the normal operation may not be performed due to the unstable clock supplied immediately after restarting the internal oscillator. To avoid this, it is necessary to keep the $\overline{\text{RESET}}$ signal at "0" long enough to release the HALT state in the STOP mode.

Table 3.4 (1) State of Pins in STOP Mode

	IN/OUT	90C840A		90C841A	
		DRVE = 0	DRVE = 1	DRVE = 0	DRVE = 1
P0	Input mode Output mode	—— OUT	—— OUT	—— ——	—— ——
P1	Input mode Output mode	—— ——	IN OUT	——	OUT
P2	Input mode Output mode	—— ——	IN OUT	——	OUT
P3	Input pin Output pin	—— ——	IN OUT	←	
P4	Output pin	——	OUT		
P5	Input pin	——	——		
P6	Input mode Output mode	—— OUT	IN OUT		
P7	Input mode Output mode	—— OUT	IN OUT		
P80 (INT0) P81 (INT1) P82 (INT2) P83 (TO3/TO4)	Input pin Input pin Input pin Output pin	IN —— —— ——	IN IN * IN * OUT		
$\overline{\text{NMI}}$ CLK $\overline{\text{RESET}}$ X1 X2	Input pin Output pin Input pin Input pin Output pin	IN —— IN —— " 1 "	IN " 1 " IN —— " 1 "		

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* : Intermediate bias is still applied to this pin in the zero cross detect mode.

—— : Indicates that input mode/input pin cannot be used for input and that the output mode/output pin have been set to high impedance.

IN : The input enable status.

IN : The input gate is operating. Fix the input voltage at either "0" or "1" to prevent the pin floating.

OUT : The output status.

It is necessary to leave INT0 at "1" until the second bus cycle of the interrupt response sequence is completed, when the STOP mode is released by the level mode of INT0.

Table 3.4 (2) I/O Operation During Halt and How to Release the Halt Command

Halt mode			RUN	IDLE2	IDLE1	STOP
WDMOD <HALTM1,0>			00	11	10	01
Operating block	CPU		Halt			
	I/O port		Keeps the state when the halt command was executed.			See Table 3.4 (1)
	8 bit timer		Operation		Halt	
	16 bit timer					
	Stepping motor controller					
	Serial interface					
	A/D converter					
	Watchdog timer					
	Interrupt controller					
Halt releasing source	Interrupt	NMI	○	○	○	○
		INTWD	○	○	—	—
		INT0	○	○	○	○
		INTT0	○	○	—	—
		INTT1	○	○	—	—
		INTT2	○	○	—	—
		INTAD	○	—	—	—
		INTT3	○	○	—	—
		INTT4	○	○	—	—
		INT1	○	○	—	—
		INTT5	○	○	—	—
		INT2	○	○	—	—
		INTRX	○	○	—	—
		INTTX	○	○	—	—
	Reset		○	○	○	○

○ : Can be used to release the halt commnad.
— : Cannot be used to release the halt command.

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3.5 Function of Ports

The TMP90C840A contains total 54 pins (TMP90C841A: 28 pins) input/output ports. These ports function not only for the general-purpose I/O but also for the input/output of the internal CPU and I/O. Table 3.5 describes the functions of these ports.

Table 3.5 Functions of Ports

Port name	Pin name	No. of pins	Direction	Direction set unit	Resetting value	Pin name for internal function
Port 0	P00~P07	8	I/O	Byte	Input	D0~D7
Port 1	P10~P17	8	I/O	Byte	Input	A0~A7
Port 2	P20~P27	8	I/O	Bit	Input	A8~A15
Port 3	P30	1	Input	—	Input	RxD
	P31	1	Input	—	Input	RxD
	P32	1	Output	—	Output	TxD/$\overline{\text{RTS}}$/SCLK
	P33	1	Output	—	Output	TxD
	P34	1	Input	—	Input	$\overline{\text{CTS}}$
	P35	1	Output	—	Output	$\overline{\text{RD}}$
	P36	1	Output	—	Output	$\overline{\text{WR}}$
	P37	1	Input	—	Input	$\overline{\text{WAIT}}$
Port 4	P40~P43	4	Output	—	Output	A16~A19
Port 5	P50~P55	6	Input	—	Input	AN0~AN5
Port 6	P60~P63	4	I/O	Bit	Input	M00~M03/TO1
Port 7	P70~P73	4	I/O	Bit	Input	M10~M13/TO3
Port 8	P80	1	Input	—	Input	INT0
	P81	1	Input	—	Input	INT1/TI4
	P82	1	Input	—	Input	INT2/TI5
	P83	1	Output	—	Output	TO3/TO4

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These port pins function as the general-purpose input/output ports by resetting. The port pins, for which input or output is programmably selectable, function as input ports by resetting. A separate program is required to use them for an internal function.
The TMP90C841A functions in the same way as the TMP90C840A except:

- Port 0 always functions as a data bus (D0 to D7).
- Port 1 always functions as Address bus (A0 to A7).
- Port 2 always functions as Address bus (A8 to A15).
- P35 and P36 of Port 3 always function as $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins, respectively.

3.5.1 Port 0 (P00~P07)

Port 0 is an 8-bit general-purpose I/O port PO whose I/O function is specified by the control register P01CR<P0C> in byte. By resetting all bits of the control register are initialized to "0", whereby Port 0 turns to the input mode, and the contents of the output latch register are undefined.

In addition to the general-purpose I/O port function, it functions as a data bus (D0~D7). Access of an external memory makes it automatically function as a data bus and <P0C> are cleared to "0".

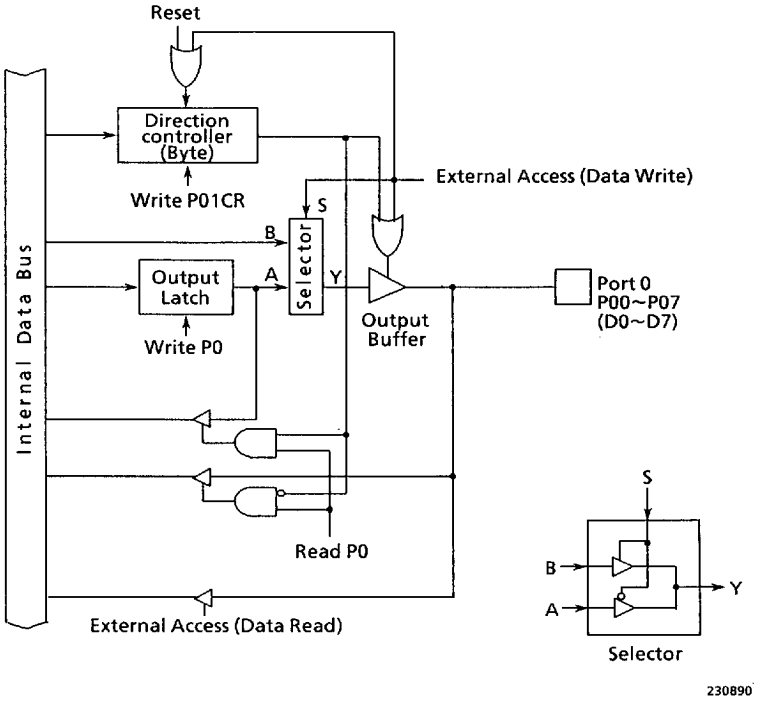

Figure 3.5 (1) Port 0

3.5.2 Port 1 (P10~P17)

Port 1 is an 8-bit general-purpose I/O port P1 whose I/O function is specified by the control register P01CR<P1C> in byte. All bits of the output latch and the control register are initialized to "0" by resetting, whereby Port 1 is put in the input mode.

In addition to the general-purpose I/O port function, it functions as an address bus (A0~A7). The address bus function can be selected by setting only the external extension control register P01CR<EXT> to "1" regardless of the status of the above control register <P1C>. The register <EXT> is reset to "0" whereby Port 1 and Port 2 turn to the general-purpose I/O mode.

The register <EXT> of the TMP90C841A is always set to "1" so that Port 1 functions as an address bus (A0~A7).

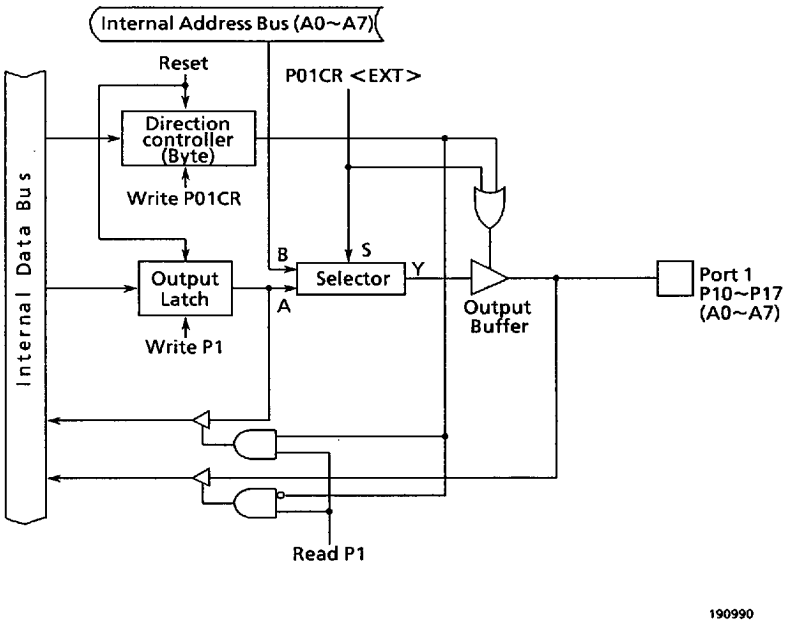

Figure 3.5 (2) Port 1

Port 0 Register

		7	6	5	4	3	2	1	0
P0 (FFC0H)	bit Symbol	P07	P06	P05	P04	P03	P02	P01	P00
	Read/Write	R/W							
	Resetting Value	Input Mode							

Port 1 Register

		7	6	5	4	3	2	1	0
P1 (FFC1H)	bit Symbol	P17	P16	P15	P14	P13	P12	P11	P10
	Read/Write	R/W							
	Resetting Value	Input Mode							

Port 0,1 Control Register

		7	6	5	4	3	2	1	0
P01CR (FFC2H)	bit Symbol		IRF0	IRFT0	IRFT1		EXT	P1C	P0C
	Read/Write		R				W	W	W
	Resetting Value		0	0	0		0	0	0
	Function		Interrupt Request Flag 1: Interrupt is requested				P1, P2 Control 0: I/O port 1: Address bus	P1 Control 0: In 1: Out	P0 Control 0: In 1: Out

Prohibit Read Modify Write.

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See "3.3.3 Interrupt controller"

Set I/O of Port 0

0	Input
1	Output

Set I/O of Port 1

0	Input
1	Output

Set general-purpose port/address bus of Ports 1 and 2

0	General-purpose port
1	Address bus

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Figure 3.5 (3) Registers for Port 0 and 1

3.5.3 Port 2 (P20~P27)

Port 2 is an 8-bit general-purpose I/O port P2 whose I/O functions are specified by the control register P2CR for each bit. All bits of the output latch and the control register are initialized to "0" by resetting, where by Port 2 turns to the input mode.

In addition to the general-purpose I/O port function, it functions as an address bus (A8~A15). The address bus function can be selected by setting the register P01CR <EXT> (shared with port 1) to "1" and setting the Port 2 control register P2CR to the output mode. When the Port 2 control register P2CR is set to "0", Port 2 functions as an input port, regardless of the status of the EXT register.

For the TM90C841A, all bits of the register <EXT> and the control register are always set to "1", and Port 2 functions as an address bus (A8 to A15).

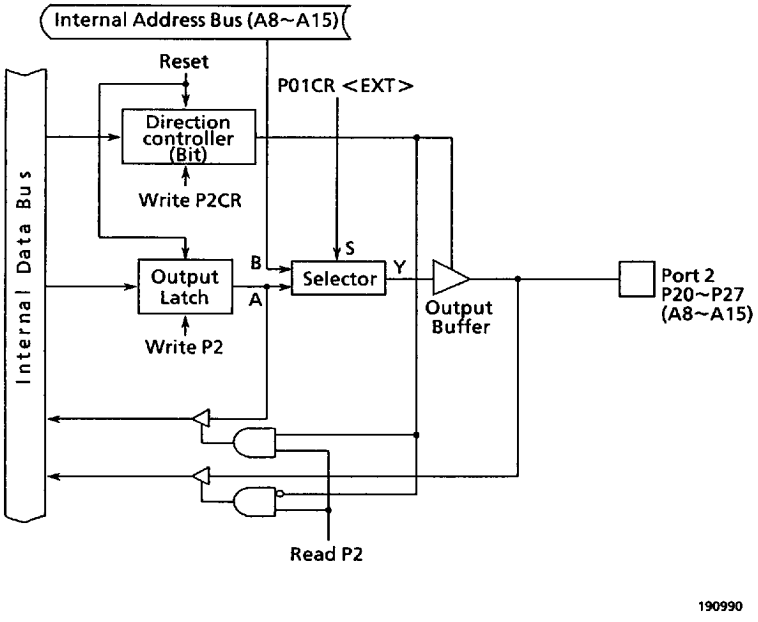

Figure 3.5 (4) Port 2

Port 2 Register

		7	6	5	4	3	2	1	0
P2 (FFC4H)	bit Symbol	P27	P26	P25	P24	P23	P22	P21	P20
	Read/Write	R / W							
	Resetting Value	Input Mode							

Port 2 Control Register

		7	6	5	4	3	2	1	0
P2CR (FFC5H)	bit Symbol	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
	Read/Write	W							
	Resetting Value	0	0	0	0	0	0	0	0
	Function	0 : In 1 : Out (I/O selected bit by bit)							

Prohibit Read Modify Write

→ Set I/O of Port 2 and Address Bus

P2CR <P2XC> \ P01CR <EXT>	0	1
0	Input Port	Input Port
1	Output Port	Address Bus

Note : Settings can be in units of bits. Here, P2CR<P2XC> is the Xth bit of P2CR.

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Figure 3.5 (5) Registers for Port 2

3.5.4 Port 3 (P30~P37)

Port 3 is an 8-bit general-purpose I/O port P3 with fixed I/O function. All bits of the output latch are initialized to "1" by resetting, and "High level" is generated to the output port.

In addition to the I/O port function, P30~P34 have the I/O function for the internal serial interface, while P35~P37 have the external memory control function. The additional functions can be selected by the control register P3CR. All bits of the control register are initialized to "0" by resetting, and the port turns to the general-purpose I/O Ports mode.

However, access of an external memory makes P35~P36 automatically function as the memory control pins ($\overline{RD}$ and $\overline{WR}$), and access of an internal memory makes them function as general-purpose I/O ports.

When an external memory is accessed, therefore, the output latch registers P35 ($\overline{RD}$) and P36 ($\overline{WR}$) should be kept at "1" which is the initial value after the reset.

The P3CR <RDE> of the control register is intended for a pseudostatic RAM. When set to "1", it always functions as an $\overline{RD}$ pin. Therefore the $\overline{RD}$ pin outputs "0" (Enable) when it is an internal memory read and internal I/O read cycle.

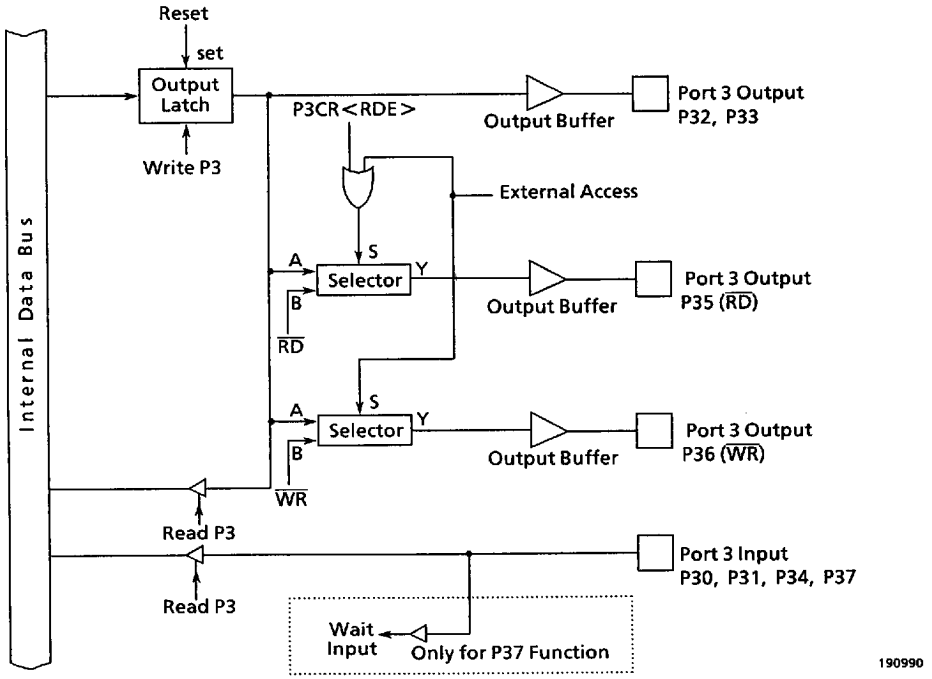

Figure 3.5 (6) Port 3