NB100LVEP224

Product Preview

2.5V/3.3V 1:24 Differential ECL/PECL Clock Driver with Clock Select and Output Enable

The NB100LVEP224 is a low skew 1–to–24 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are differential ECL/PECL and they are selected by the CLK_SEL pin. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable ($\overline{OE}$) is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (See Figure 4).

The NB100LVEP224 guarantees low output–to–output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot.

The NB100LVEP224, as with most other ECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP224 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single–ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in LVPECL mode, or $V_{EE} \leq -3.0$ V in NECL mode. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on PECL terminations, designers should refer to Application Note AND8020/D.

- 15 ps Typical Output–to–Output Skew
- 85 ps Typical Device–to–Device Skew
- Maximum Frequency > 1 GHz
- 575 ps Typical Propagation Delay
- LVPECL Mode Operating Range:
  V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = –2.375 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default Low with Inputs Open or at V_{EE}
- Thermally Enhanced 64–Lead LQFP

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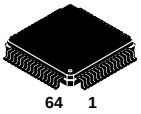
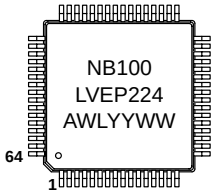
MARKING DIAGRAM*





64–LEAD LQFP
CASE 848G
THERMALLY ENHANCED
FA SUFFIX

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NB100LVEP224FA	LQFP–64	160 Units/Tray
NB100LVEP224FAR2	LQFP–64	1500/Tape & Reel

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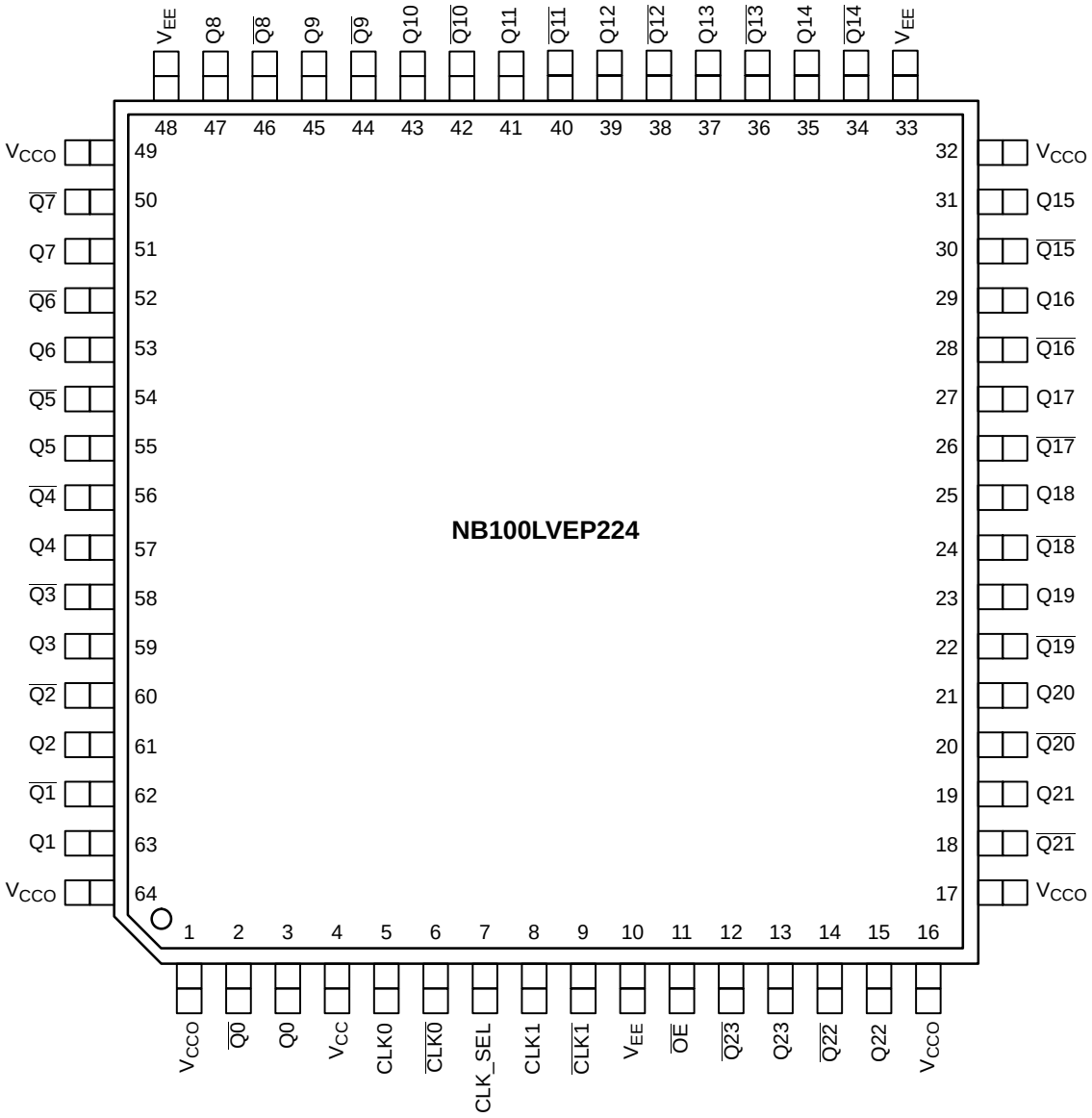


All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to appropriate Power Supply to guarantee proper operation. The thermally conductive exposed pad on package bottom (see package case drawing) must be attached to a heat–sinking conduit, capable of transferring 1.2 Watts. This exposed pad is electrically connected to V_{EE} internally.

Figure 1. 64–Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLK0*, $\overline{\text{CLK0}}$**	ECL Differential Input Clock
CLK1*, $\overline{\text{CLK1}}$**	ECL Differential Input Clock
CLK_SEL*	ECL Input CLK Select
$\overline{\text{OE}}$*	ECL Output Enable
Q0–Q23, $\overline{\text{Q0}}$–$\overline{\text{Q23}}$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}***	Negative Supply

* Pins will default LOW when left open.

** Pins will default HIGH when left open.

***The thermally conductive exposed pad on the bottom of the package is electrically connected to V_{EE} internally.

FUNCTION TABLE

$\overline{\text{OE}}$ (1)	CLK_SEL	Q0–Q23	$\overline{\text{Q0–Q23}}$
L	L	CLK0	$\overline{\text{CLK0}}$
L	H	CLK1	$\overline{\text{CLK1}}$
H	L	L	H
H	H	L	H

1. The $\overline{\text{OE}}$ (Output Enable) signal is synchronized with the falling edge of the LVPECL_CLK signal.

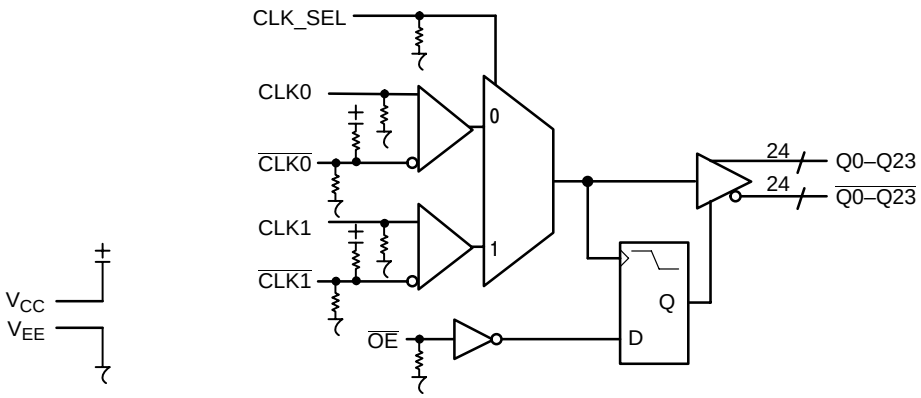


Figure 2. Logic Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 1)		Level 3
Flammability Rating Oxygen Index		UL 94 V–0 @ 0.125 in 28 to 34
Transistor Count		654 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 to 0 –6 to 0	V
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (See Application Information)	0 LFPM 500 LFPM	64 LQFP 64 LQFP	35.6 30	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case) (See Application Information)	0 LFPM 500 LFPM	64 LQFP 64 LQFP	3.2 6.4	°C/W °C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0 V (Note 3)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		170			170			170		mA
V_{OH}	Output HIGH Voltage (Note 4)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 4)	1355	1480	1695	1355	1480	1695	1355	1480	1695	mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Note 5)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Note 5)	1490		1675	1490		1675	1490		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6) (Figure 5)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.5 V.
4. All outputs loaded with 50 Ω to V_{CC} – 2.0 V.
5. Single ended input operation is limited $V_{CC} \geq 3.0$ V in LVPECL mode.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NECL DC CHARACTERISTICS V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V (Note 7)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		170			170			170		mA
V_{OH}	Output HIGH Voltage (Note 8)	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV
V_{OL}	Output LOW Voltage (Note 8)	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Note 9)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Note 9)	–1810		–1625	–1810		–1625	–1810		–1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10) (Figure 5)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC}.
8. All outputs loaded with 50 Ω to V_{CC} – 2.0 V.
9. Single ended input operation is limited $V_{EE} \leq$ –3.0 V in NECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V (Note 11)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{Opp}	Differential Output Voltage (Figure 3) f_{out} < 50 MHz	500	600		600	700		600	700		mV
	f_{out} < 0.8 GHz	450	600		550	700		550	700		mV
	f_{out} < 1.0 GHz	400	550		450	650		450	650		mV
t_{PLH} t_{PHL}	Propagation Delay (Differential) CLKx–Qx		575			575			575		ps
	CLK_SELx–Qx		675			675			675		ps
t_{skew}	Within–Device Skew (Note 12)		15			15			15		ps
	Device–to–Device Skew (Note 13)		85			85			85		ps
t_{JITTER}	Random Clock Jitter (Figure 3) (RMS)					< 1					ps
V_{PP}	Input Swing (Differential) (Note 15) (Figure 5)	150	800	1200	150	800	1200	150	800	1200	mV
t_S	$\overline{OE}$ Set Up Time (Note 14)	200			200			200			ps
t_H	$\overline{OE}$ Hold Time	200			200			200			ps
t_r/t_f	Output Rise/Fall Time (20%–80%)		160			160			160		ps

11. Measured with PECL 750 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to V_{CC} – 2 V.
12. Skew is measured between outputs under identical transitions and conditions on any one device.
13. Device–to–Device skew for identical transitions at identical V_{CC} levels.
14. $\overline{OE}$ Set Up Time is defined with respect to the falling edge of the clock. $\overline{OE}$ High–to–Low transition ensures outputs remain disabled during the next clock cycle. OE Low–to–High transition enables normal operation of the next input clock.
15. V_{PP} is the differential input voltage swing required to maintain AC characteristics including t_{PD} and device–to–device skew.

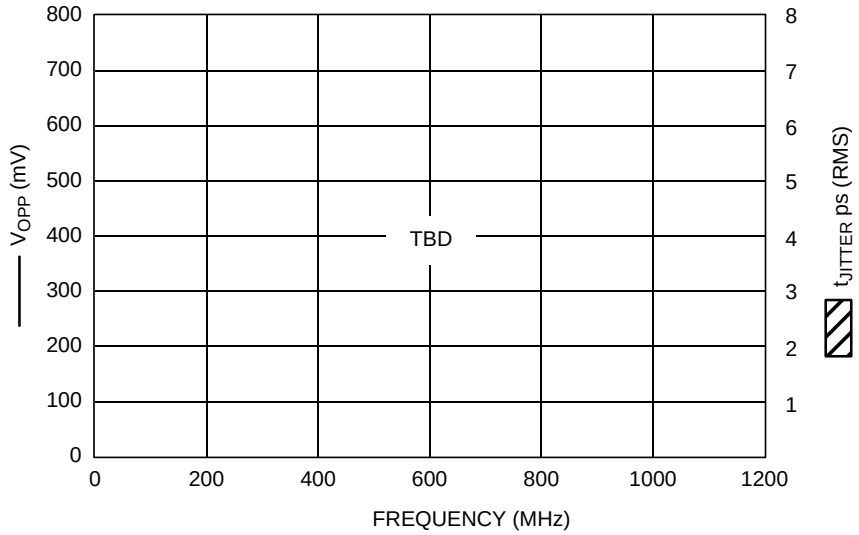


Figure 3. Output Frequency (F_{OUT}) versus Output Amplitude (V_{OPP}) and Random Clock Jitter (t_{JITTER})

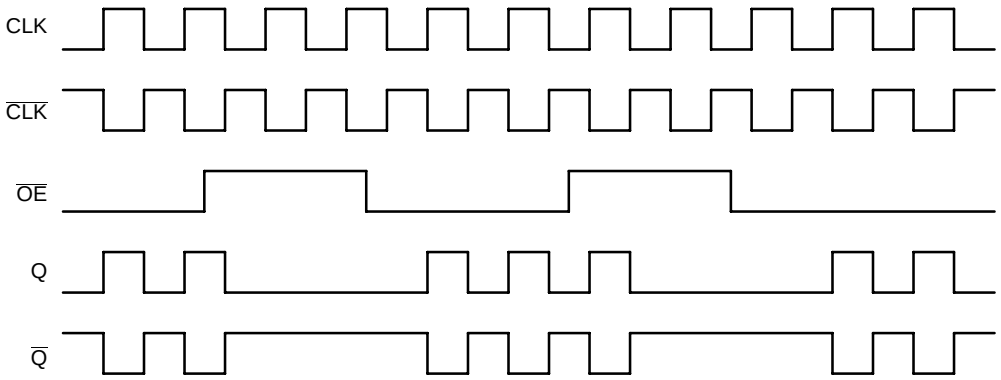


Figure 4. Output Enable (OE) Timing Diagram

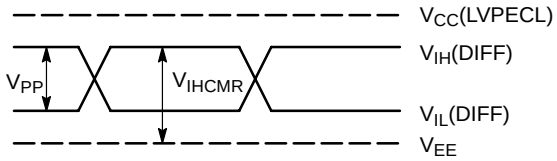


Figure 5. LVPECL Differential Input Levels

Resource Reference of Application Notes

AN1405 – ECL Clock Distribution Techniques

AND8002 – Marking and Date Codes

AND8009 – ECLinPS Plus Spice I/O Model Kit

AND8020 – Termination of ECL Logic Devices

16. For an updated list of Application Notes, please see our website at http://onsemi.com.

APPLICATIONS INFORMATION

Using the thermally enhanced package of the NB100LVEP224

The NB100LVEP224 uses a thermally enhanced 64–lead LQFP package. The package is molded so that a portion of the leadframe is exposed at the surface of the package bottom side. This exposed metal pad will provide the low thermal impedance that supports the power consumption of the NB100LVEP224 high–speed bipolar integrated circuit and will ease the power management task for the system design. In multilayer board designs, a thermal land pattern on the printed circuit board and thermal vias are recommended to maximize both the removal of heat from the package and electrical performance of the NB100LVEP224. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area should be at least the same size and shape as the exposed pad on the package. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal conduit. The thermal vias will connect the exposed pad of the package to internal copper planes of the board. The number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern.

The recommended thermal land design for NB100LVEP224 applications on multi–layer boards comprises a 4 X 4 thermal via array using a 1.2 mm pitch as shown in Figure 6 providing an efficient heat removal path.

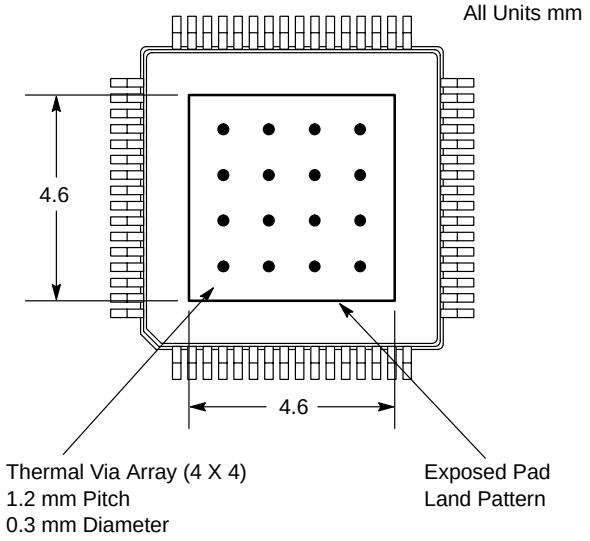


Figure 6. Recommended Thermal Land Pattern

The via diameter should be approximately 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via may result in voiding during the solder process and must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for the exposed pad package is equivalent to standard surface mount packages. Figure 7, “Recommended solder mask openings”, shows a recommended solder mask opening with respect to a 4 X 4 thermal via array. Because a large solder mask opening may result in a poor rework release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff of 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

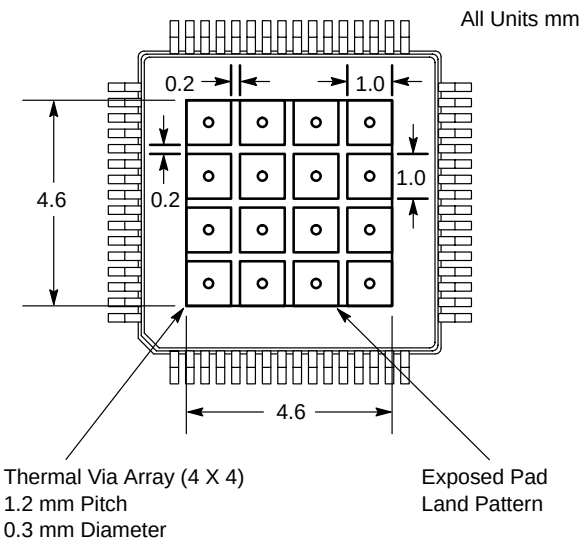


Figure 7. Recommended Solder Mask Openings

Proper thermal management is critical for reliable system operation. This is especially true for high–fanout and high output drive capability products.

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 1. Thermal Resistance *

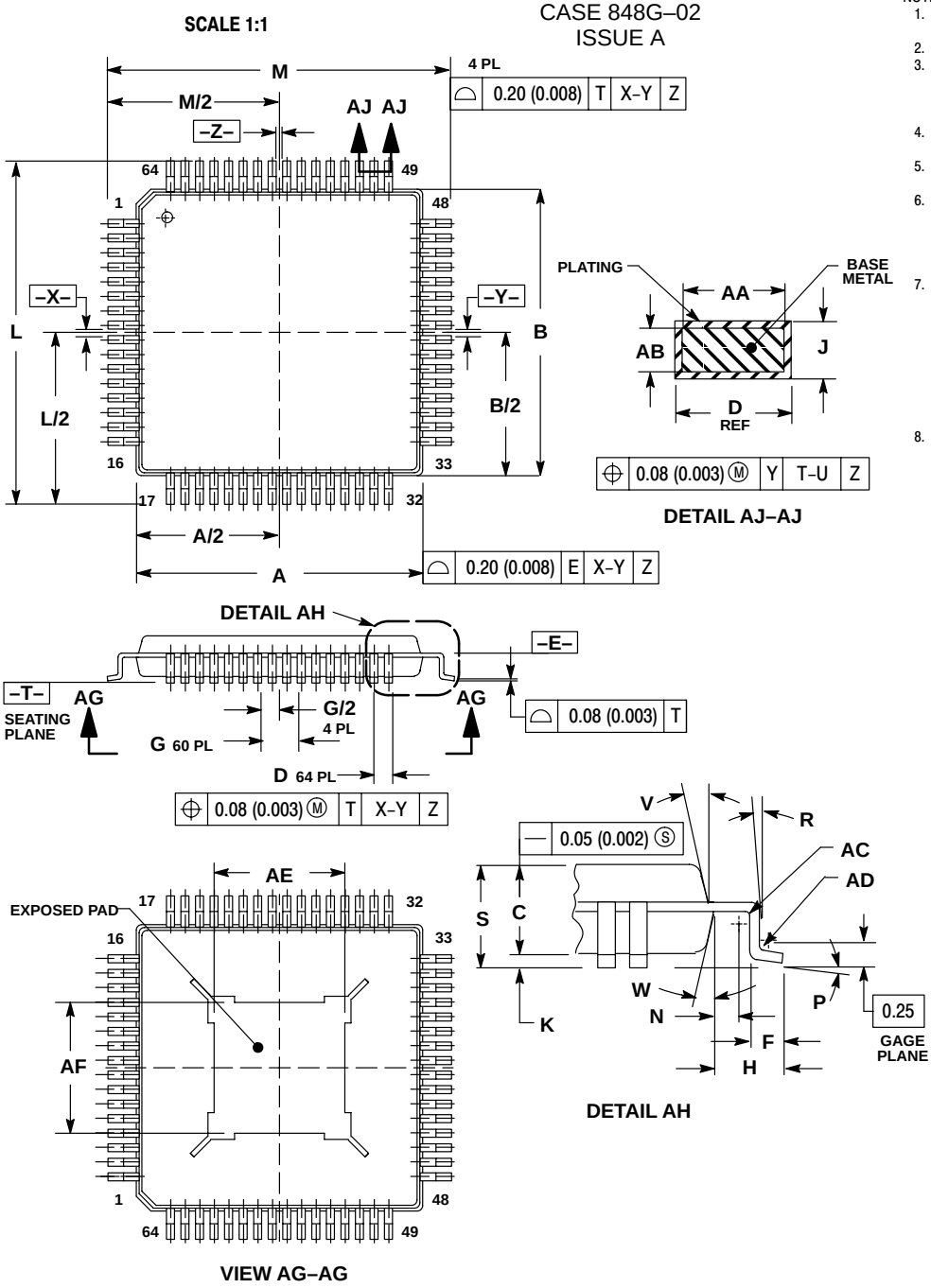
LFPM	θJA °C/W	θJC °C/W
0	35.6	3.2
100	32.8	4.9
500	30.0	6.4

* Junction to ambient and Junction to board, four–conductor layer test board (2S2P) per JESD 51–8

These recommendations are to be used as a guideline, only. It is therefore recommended that users employ sufficient thermal modeling analysis to assist in applying the general recommendations to their particular application to assure adequate thermal performance. The exposed pad of the NB100LVEP224 package is electrically shorted to the substrate of the integrated circuit and V_{EE}. The thermal land should be electrically connected to V_{EE}.

PACKAGE DIMENSIONS

LQFP
FA SUFFIX
64–LEAD PACKAGE
CASE 848G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM PLANE "E" IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
4. DATUM "X", "Y" AND "Z" TO BE DETERMINED AT DATUM PLANE DATUM "E".
5. DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM "T".
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLAND "E".
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
B	10.00 BSC		0.394 BSC	
C	1.35	1.45	0.053	0.057
D	0.17	0.27	0.007	0.011
F	0.45	0.75	0.018	0.030
G	0.50 BSC		0.020 BSC	
H	1.00 REF		0.039 BSC	
J	0.09	0.20	0.004	0.008
K	0.05	0.15	0.002	0.006
L	12.00 BSC		0.472 BSC	
M	12.00 BSC		0.472 BSC	
N	0.20	---	0.008	---
P	0 °	7 °	0 °	7 °
R	0 °	---	0 °	---
S	---	1.60	---	0.063
V	11 °	13 °	11 °	13 °
W	11 °	13 °	11 °	13 °
AA	0.17	0.23	0.007	0.009
AB	0.09	0.16	0.004	0.006
AC	0.08	---	0.003	---
AD	0.08	---	0.003	---
AE	4.50	4.78	0.180	0.188
AF	4.50	4.78	0.180	0.188

Notes

Notes

Notes

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