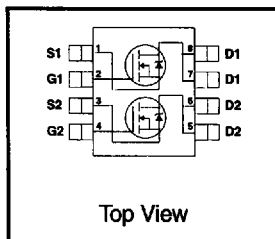


HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching



$$V_{DS} = 50V$$

$$R_{DS(on)} = 0.30\Omega$$

$$I_D = 2.0A$$

Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.80W is possible in a typical PCB mount application.



SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	1.3	
I_{DM}	Pulsed Drain Current ①	8.0	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.0	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	1.4	
	Linear Derating Factor	0.016	W/°C
	Linear Derating Factor (PCB Mount)**	0.011	
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-PCB	—	—	62	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	90	

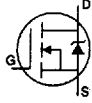
** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	50	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.053	—	V/°C	Reference to 25°C , $I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	$V_{GS}=10V$, $I_D=1.5A$ ④
		—	—	0.50		$V_{GS}=5.0V$, $I_D=0.60A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.5	—	3.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	Forward Transconductance	1.0	—	—	S	$V_{DS}=25V$, $I_D=1.5A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	2.0	μA	$V_{DS}=50V$, $V_{GS}=0V$
		—	—	250		$V_{DS}=40V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
Q_g	Total Gate Charge	—	—	6.6	nC	$I_D=1.3A$
Q_{gs}	Gate-to-Source Charge	—	—	1.3		$V_{DS}=40V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	2.0		$V_{GS}=10V$ See Fig. 6 and 12 ④
$t_{d(on)}$	Turn-On Delay Time	—	5.4	—	ns	$V_{DD}=30V$
t_r	Rise Time	—	5.6	—		$I_D=0.60A$
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		$R_G=25\Omega$
t_f	Fall Time	—	19	—		$R_D=50\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	120	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	63	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	12	—		$f=1.0MHz$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	8.0		
V_{SD}	Diode Forward Voltage	—	—	1.4	V	$T_J=25^\circ\text{C}$, $I_S=1.8A$, $V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	38	57	ns	$T_J=25^\circ\text{C}$, $I_F=1.8A$
Q_{rr}	Reverse Recovery Charge	—	50	80	nC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

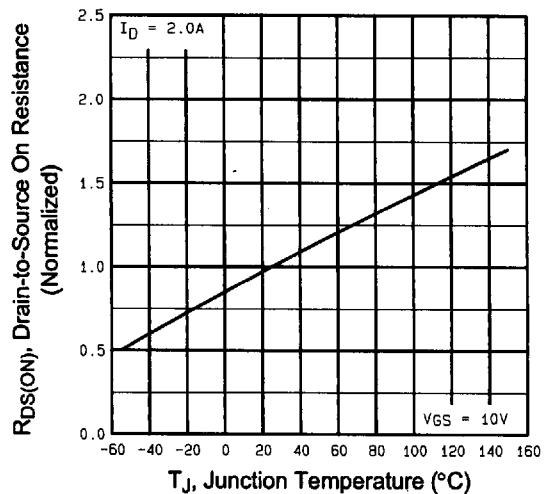
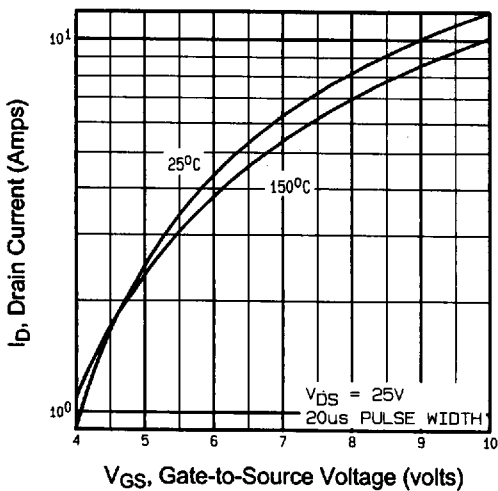
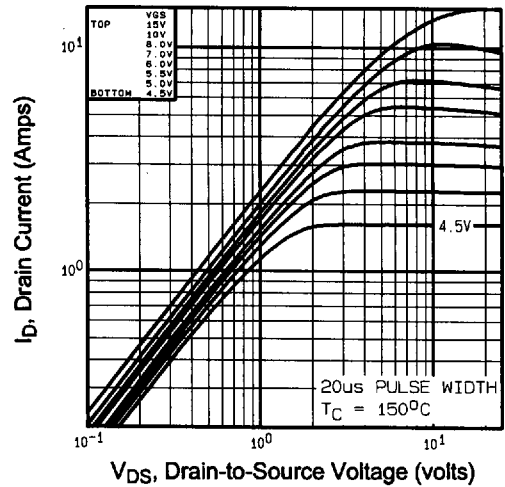
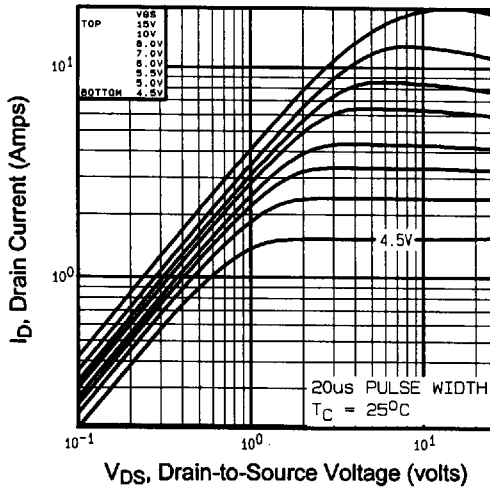
Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ $I_{SD} \leq 2.0A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

② Not Applicable

④ Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.



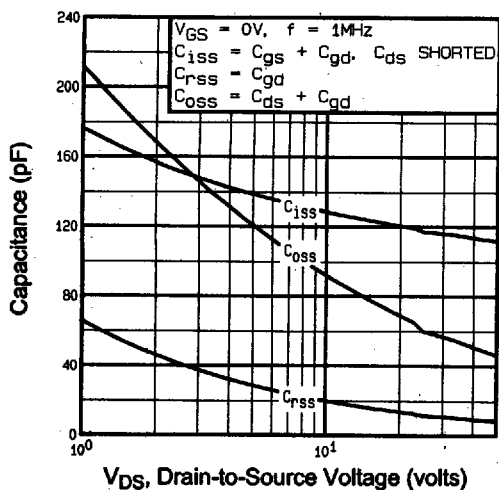


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

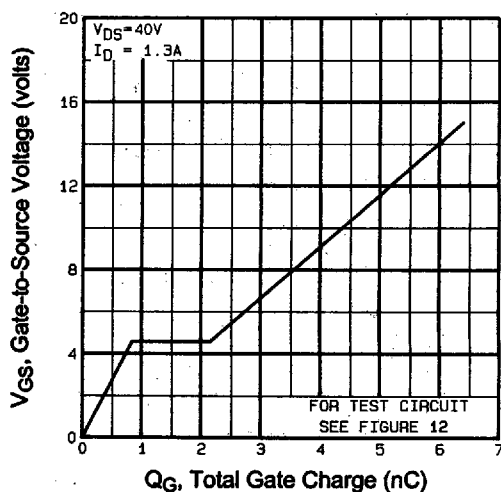


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

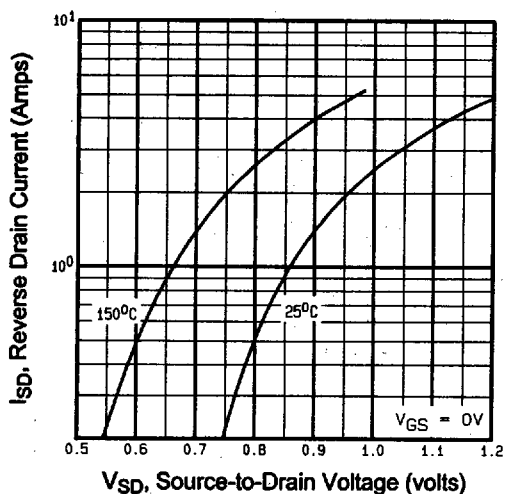


Fig 7. Typical Source-Drain Diode Forward Voltage

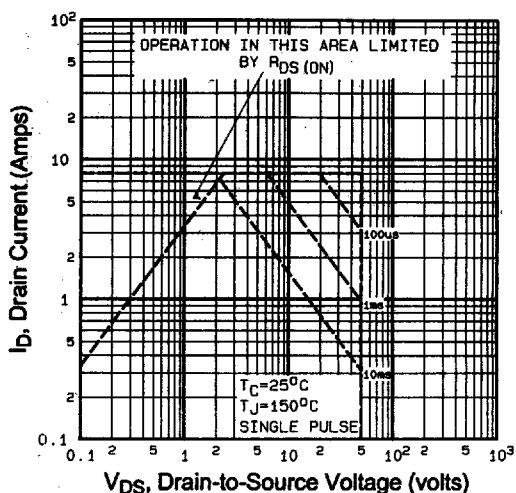


Fig 8. Maximum Safe Operating Area

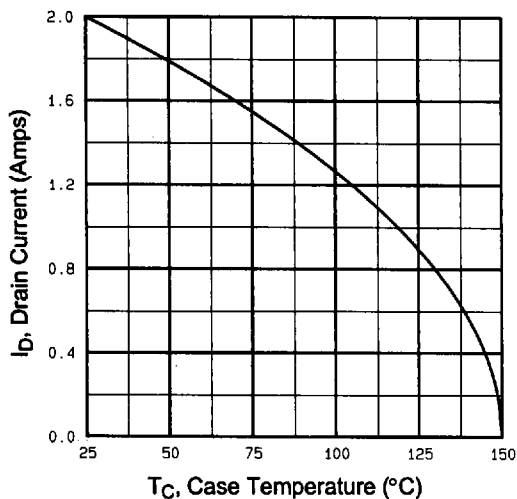


Fig 9. Maximum Drain Current Vs. Case Temperature

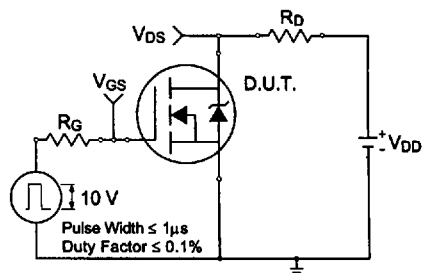


Fig 10a. Switching Time Test Circuit

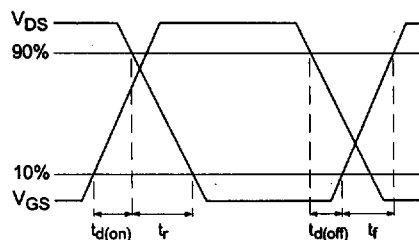


Fig 10b. Switching Time Waveforms

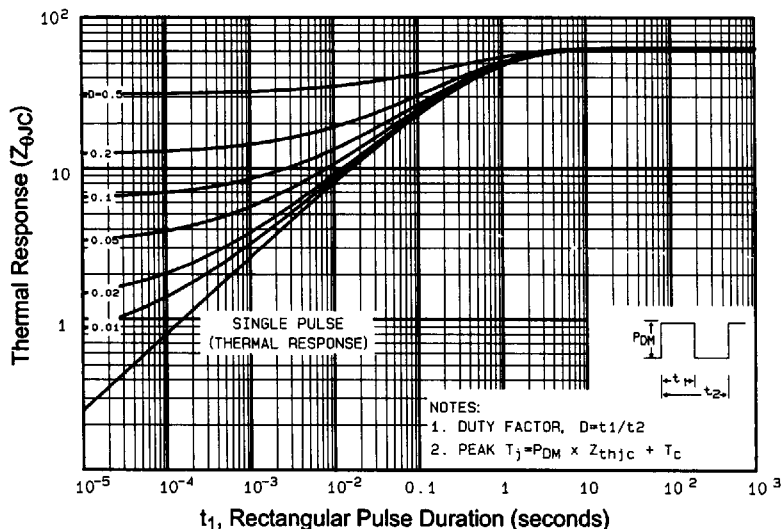


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

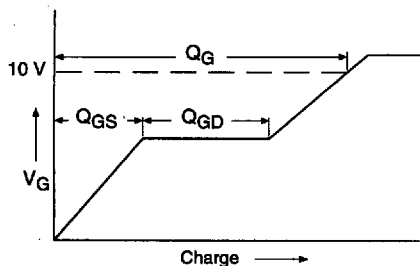


Fig 12a. Basic Gate Charge Waveform

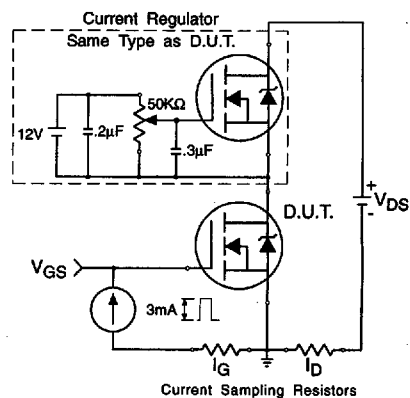


Fig 12b. Gate Charge Test Circuit

Refer to the Appendix Section for the following:

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 327

Appendix B: Package Outline Mechanical Drawing – See page 332

Appendix C: Part Marking Information – See page 332

Appendix D: Tape & Reel Information – See page 336

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