Integrated Device Technology, Inc.

CMOS SINGLE 8-BIT PaletteDAC™ FOR TRUE COLOR APPLICATIONS

PRELIMINARY
IDT75C457

FEATURES

- 165/135/125/110/80 MHz operating speeds
- Pin- and function-compatible with Brooktree Bt 457
- Fixed pipeline delay: No external circuitry required
- 50ns read access time
- Integral and differential linearity < 1/2 LSB
- Single 8-bit DAC
- 256 x 8 Dual-Ported Color Palette RAM
- 4 x 8 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible output
- Single 5 volt power supply
- 84-pin PGA and PLCC packages
- Typical power dissipation: 1000mW
- CEMOS™ Monolithic construction
- Military product is compliant with MIL-STD-883, Class B

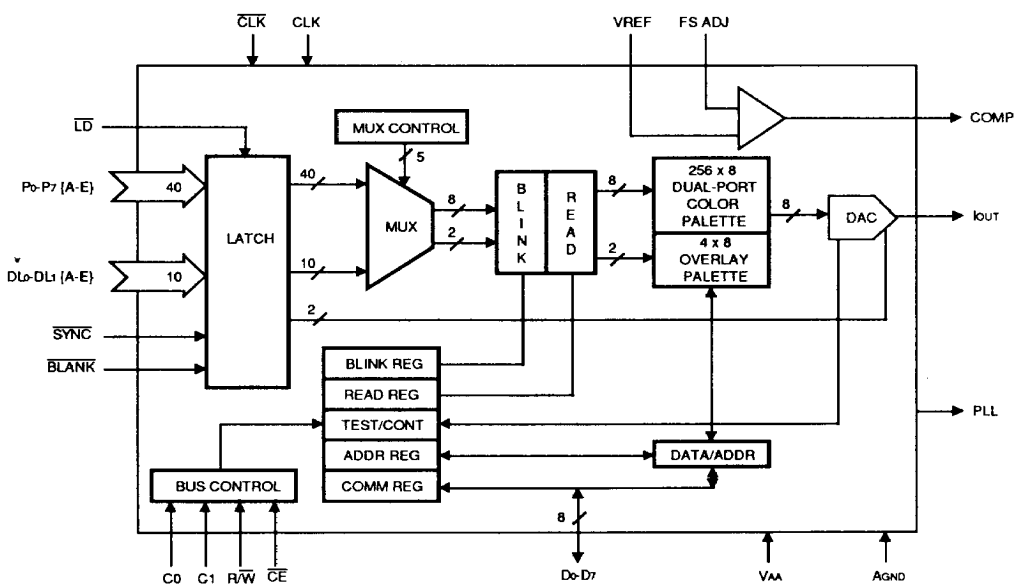
DESCRIPTION

The IDT75C457 is a single channel 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of true-color, high resolution graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

Features included on-chip are programmable blink rates, bit plane masking and blinking, as well as color overlay capability. The IDT75C457 generates an RS-343A compatible video output that is capable of driving a doubly terminated 75 ohm coaxial cable directly. A PLL current output enables synchronization of three IDT75C457s, thus allowing display of true-color images.

The IDT75C457 military PaletteDACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest levels of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2523 drw 01

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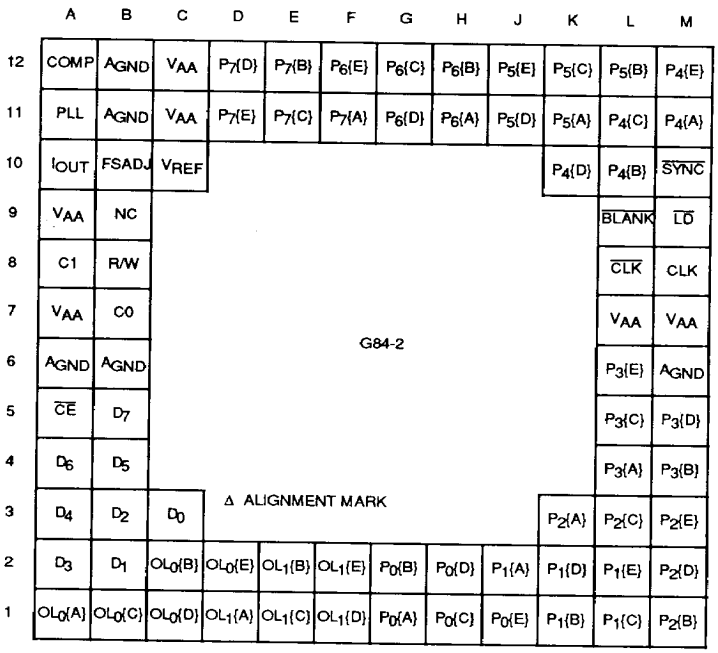
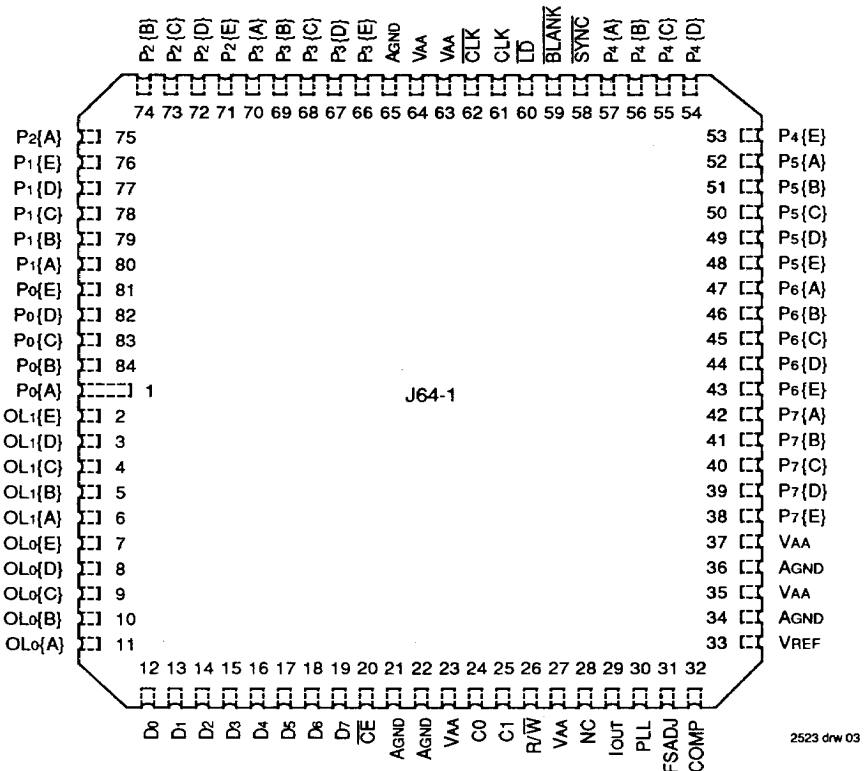
PIN CONFIGURATIONS



PGA
TOP VIEW

2523 drw 02



NC - No Connect

PLCC
TOP VIEW

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GENERAL INFORMATION

The IDT75C457 triple 8-bit PaletteDAC is a highly integrated building block which interfaces a relatively low bandwidth frame buffer memory to analog RS-343A high bandwidth output.

The IDT75C457 includes a look-up table for updating color information and other graphics applications. The basic functional blocks are the microprocessor bus interface, the frame buffer memory interface and multiplexer, a dual-port RAM with one R/$\overline{W}$ port, one high-speed R/O port and one 8-bit video speed DAC.

MICROPROCESSOR BUS INTERFACE

The IDT75C457 supports a standard microprocessor bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay registers allow color updating without contention with the display refresh process.

The bus interface consists of eight bidirectional data pins, D_0-D_7, with two control inputs, C0 and C1, a read/write direction input, R/$\overline{W}$, and a clock input, $\overline{CE}$. All data and control information are latched on the falling edge of $\overline{CE}$, as shown in Figure 3. All accesses to the chip are controlled by the data in the address register combined with the control inputs C0, C1 and R/$\overline{W}$, depicted in the Truth Table (Table 1).

An access to a control register requires writing a 4 through 7 into the address register (C0 = C1 = 0) and then writing or reading data to the selected register (C0 = 0, C1 = 1). When accessing the control registers, the address register is not changed, facilitating read-modify-write operations. If an invalid address is loaded into the address register, data written is ignored or invalid data is read out.

It is also possible to access the color palette information. The palette is organized as 256 address with 8 bits of red, blue or green information. Additionally, there are two extra addresses assigned to overlay information, yielding a total memory size of 260 x 8.

There are two modes of accessing palette entries on the IDT75C457, "Normal", and "RGB".

In Normal mode, writing color data entails the MPU loading the address register with the address of the color palette location or the overlay palette location to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette or the overlay palette. The address register then increments to the next address location which the MPU may modify simply by writing another color. Reading color data is similar to writing, except the MPU executes read cycles.

Normal mode is useful if a 24-bit data bus is available, as 24 bits of color information (eight bits each of red, green, and blue) may be read or written to three IDT75C457s in a single MPU cycle. In this application the $\overline{CE}$ inputs of all three IDT75C457s are connected together. If only an eight-bit data bus is available, the $\overline{CE}$ inputs must be individually selected during the appropriate color read or write cycle (red $\overline{CE}$ during red write cycle, blue during blue write cycle, etc.). When accessing the color palette the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay palette, the address register increments to $04 following a read or write cycle to overlay color three.

In RGB mode, writing color data entails the MPU loading the address register with the address of the color palette location or overlay palette location to be modified. The MPU performs three successive write cycles (eight bits each of red, green or blue), using C0 or C1 to select either the color palette or the overlay palette. After the blue write cycle, the address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green or blue data. Reading color data is similar to writing except the MPU executes the read cycles.

RGB mode is useful if only an eight-bit data bus is available. Each IDT75C457 is programmed to be red, green or blue PaletteDAC, and will respond only to the assigned read or write cycle. In this application, the IDT75C457s share a common eight-bit data bus. The $\overline{CE}$ inputs of all three IDT75C457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

Address Register Data	C1	C0	Access
X	0	0	Address Register
$00-$FF	0	1	Color Palette
$00	1	1	Overlay Color 0
$01	1	1	Overlay Color 1
$02	1	1	Overlay Color 2
$03	1	1	Overlay Color 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Test Register

2523 tbl 01

Table 1. Truth Table for MPU Operations

When accessing the color palette, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay palette, the address register increments to location $04 following a blue read or write cycle to overlay color three. To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count module three. They are reset to 0 when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR 0-7) are accessible to the MPU.

FRAME BUFFER INTERFACE

The frame buffer interface consists of five 8-bit input ports which correspond to five consecutive pixels. In addition, there are two extra bits per port which may be used for overlay information. To reduce the bandwidth requirements for the pixel data, the IDT75C457 latches 4 or 5 pixels (the multiplex factor is programmable to 4 or 5 by bit 7 of the command register) on each rising edge of $\overline{LD}$. The color and overlay information is internally multiplexed at the pixel clock frequency,

CLK, and sequentially output. This arrangement allows pixel data to be transferred at a rate 4 or 5 times slower than the pixel clock. Typically, $\overline{LD}$ is the pixel clock divided by 4 or 5 and is used to clock data out of the frame buffer memory.

As shown in Figure 2, sync, blank, color and overlay information are latched on the rising edge of $\overline{LD}$. Up to 40 bits of color information are input through P_0-P_7{A-E} and up to 10 bits of overlay information are input through OL_0-OL_1{A-E}. Both sync and blank have separate inputs, $\overline{SYNC}$ and $\overline{BLANK}$, respectively. The IDT75C457 outputs color information on each clock cycle. Four or five pixels are output sequentially, beginning with the {A} information, then the {B} information, until the cycle is completed with the {D} or {E} information. In this configuration, sync and blank are limited to multiples of four or five clock cycles.

The multiplexing factor, 4:1 or 5:1, is programmable from the command register, bit 7. In the 4:1 mode, the {E} color and overlay inputs are not used and the $\overline{LD}$ clock should be CLOCK divided by 4. The {E} color and overlay inputs must be connected to a valid logic level.

The overlay inputs (OL_0-OL_1) have the same timing as the pixel inputs (P_0-P_7). It is possible to use additional bit planes or external logic to control the overlay selection for cursor generation.

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INTERNAL MULTIPLEXING

$\overline{LD}$ is typically CLK divided by four or five and it latches color and overlay information on every rising edge, independent of CLK. A digital PLL allows $\overline{LD}$ to be phase independent of CLK. The only restriction is that only one rising edge of $\overline{LD}$ is allowed to occur per four (4:1 multiplexing) or five (5:1 multiplexing) CLK cycles.

Color Palette

On the rising edge of each CLK cycle, eight bits of color information (P_0-P_7) and two bits of overlay information (OL_0-OL_1) for each pixel are processed by the read mask, blink mask and command registers. This information provides the address to the dual-port color palette RAM. Note that P_0 is the LSB when addressing the color palette RAM. The value stored at a selected address determines the displayed color. Through the use of the control register, individual bit planes may be enabled or disabled for display and/or blinked at one of four blink rates and duty cycles.

The blink timing is based on vertical retrace intervals which are defined by at least 256 $\overline{LD}$ cycles since the last falling edge of $\overline{BLANK}$. The color changes during this normally blanked time.

The processed pixel data is then used to select which color palette entry or overlay register is used to provide color information. Table 2 illustrates the truth table used for color selection.

CR_6[1]	OL_1	OL_0	P_7-P_0	Palette Entry
1	0	0	$00	Color Palette Entry $00
1	0	0	$01	Color Palette Entry $01
	.			.
	.			.
	.			.
1	0	0	$FF	Color Palette Entry $FF
0	0	0	$xx	Overlay Color 0
x	0	1	$xx	Overlay Color 1
x	1	0	$xx	Overlay Color 2
x	1	1	$xx	Overlay Color 3

NOTE: 2523 tbl 02

1. CR_6 is bit 6 of the Command Register.

Table 2. Palette and Overlay Select

Video Generation, DACs

On every CLK cycle, the selected 8 bits of color information from the Color Palette RAM are presented to the 8-bit D/A converters. The IDT75C457 uses a 5 x 3 segmented approach where the five MSBs of the input data are decoded into a parallel "Thermometer" code which produces thirty two "coarse" output levels. The remaining three LSBs of input data drive three binary weighted current switches with a total contribution of one-thirty second of full scale. The MSB and LSB currents are summed at the output to produce 256 levels.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are pipelined to maintain synchronization with the pixel data. Both inputs drive appropriately weighted current switches which are summed at the output of the DACs to produce the specific output levels required by RS-343, as shown in Figure 3. Table 3 details the output levels associated with $\overline{SYNC}$, $\overline{BLANK}$ and data.

Monitor Interface

The analog outputs of the IDT75C457 are high-impedance current sources which are capable of directly driving a doubly terminated 75Ω coaxial cable to standard video levels. A typical output circuit is shown in Figure 4.

Description	S	B	DAC Data	I_{OUT} (mA)
WHITE	1	1	$FF	26.67
DATA	1	1	Data	Data + 9.05
DATA and SYNC	0	1	Data	Data + 1.44
BLACK	1	1	$0	9.05
BLACK and SYNC	0	1	$0	1.44
BLANK	1	0	X	7.62
SYNC	0	0	X	0

NOTE: 2523 tbl 03

1. Typical values with full scale I_{OUT} = 26.67mA, R_{SET} = 523Ω, V_{REF} = 1.235V, S is SYNC, B is BLANK.

Table 3. Video Output Truth Table

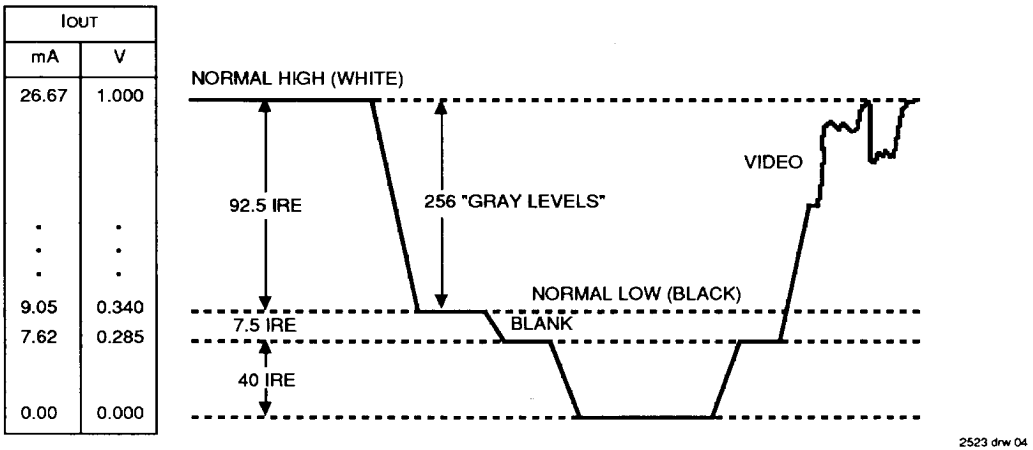

Figure 1. Composite Video Output Waveform

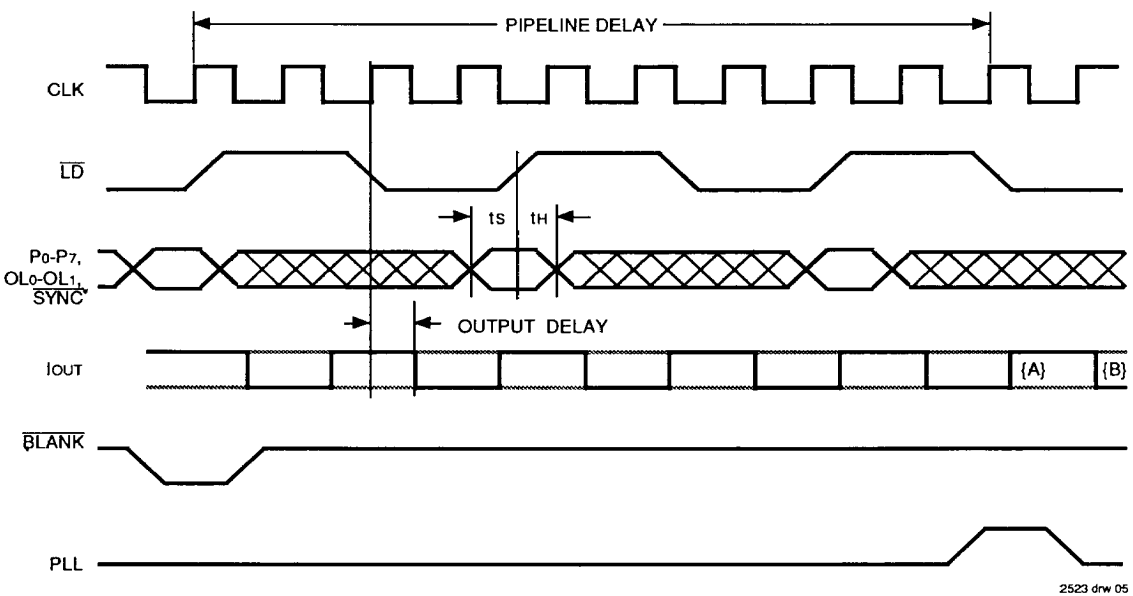

Figure 2. Pixel Timing

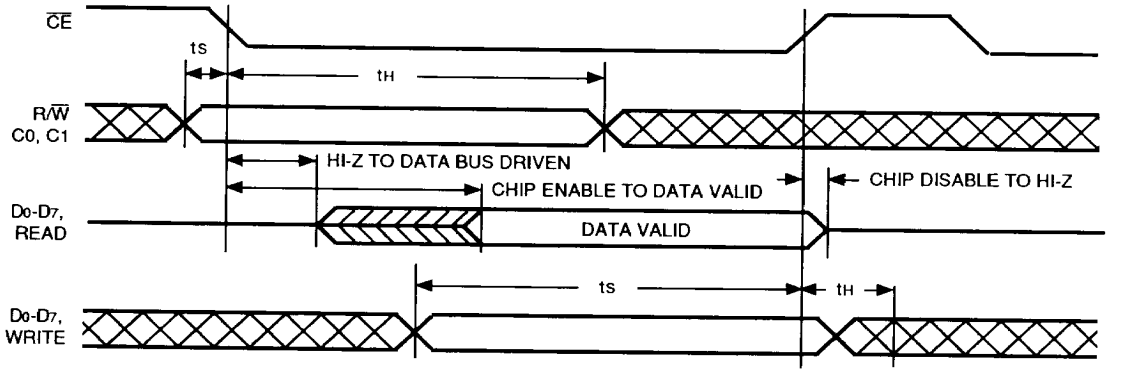

Figure 3. Data Bus Timing

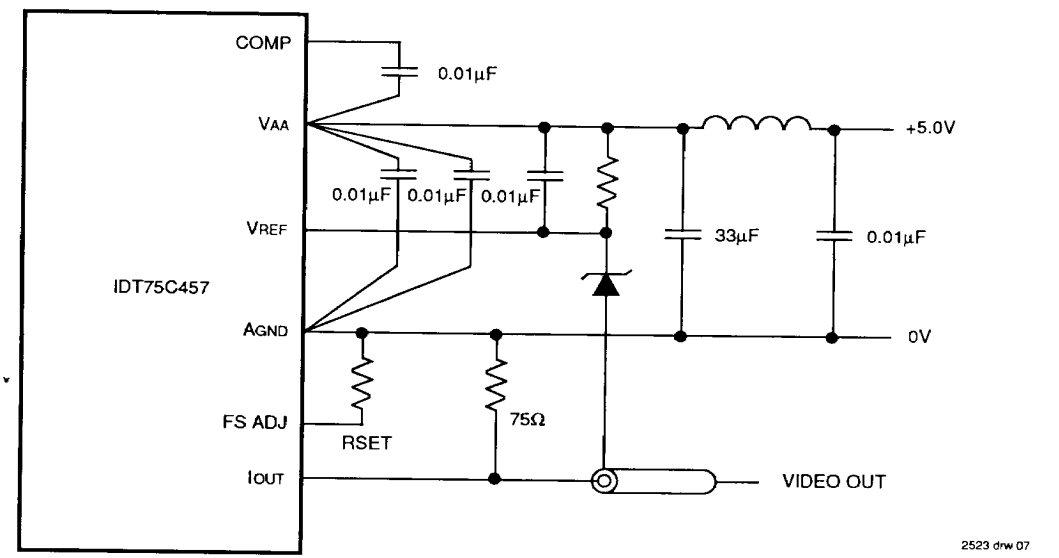

Figure 4. Typical Application

PIN DESCRIPTIONS

Pin Name	Description
Data Bus	
D_0-D_7	8-bit, bidirectional data bus. Data is input and output over this bus and the flow is controlled by R/$\overline{W}$ and $\overline{CE}$. D_7 is the most significant bit.
$\overline{CE}$	Chip Enable Input. The chip is enabled when this control pin is LOW. During a write cycle (R/$\overline{W}$ LOW), the data present on D_0-D_7 is internally latched on the LOW-to-HIGH transition of this pin.
R/$\overline{W}$	Read/Write Control input. The Read/Write input is latched on the HIGH-to-LOW transition of $\overline{CE}$ and determines the direction of the bidirectional data bus, D_0-D_7. If R/$\overline{W}$ is HIGH during the falling edge of $\overline{CE}$, a read cycle occurs. If R/$\overline{W}$ is LOW during the falling edge of $\overline{CE}$, a write cycle occurs and, additionally, D_0-D_7 are latched on the rising edge of $\overline{CE}$.
C0, C1	Register Control inputs. C0 and C1 determine which register or palette entry is accessed during a read or write cycle. These inputs are latched on the HIGH-to-LOW transition of $\overline{CE}$.
Pixel	
CLK, $\overline{CLK}$	Pixel Clock Inputs. These inputs are differential and may be driven by ECL operating from a +5V supply. The clock frequency is normally the system pixel clock rate.
$\overline{LD}$	Load Clock input. The Load Clock is normally CLK divided by 4 or 5 (determined by the Control Register bit 7). The pixel data, P_0-P_7 {A-E} and OL_0-OL_1 {A-E}, $\overline{BLANK}$ and $\overline{SYNC}$ are internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
P_0-P_7 {A-E}	Pixel Input Data. These inputs provide the address input to the color palette RAM. The data stored at a particular address is the color output by the DAC. Four or five consecutive pixels, as determined by bit 7 in the Command Register, are internally latched on the LOW-to-HIGH transition of $\overline{LD}$. The pixels are output sequentially, first {A} then {B}. After all four or five pixels have been output, the cycle repeats. Unused inputs must be connected to a valid logic level.
OL_0-OL_1{A-E}	Pixel Overlay Inputs. The Overlay inputs have the same timing as P_0-P_7 and select between either the color palette or the overlay palette. When the overlay palette is selected, the pixel information P_0-P_7 {A-E} is ignored. Bit 6 of the command register determines if Overlay = 0 displays overlay color 0 or the color palette entry. See Table 2 for details.
$\overline{BLANK}$	Composite Blank Input. A LOW on this input forces the analog outputs (I_{OUT}) to the blanking level. The $\overline{BLANK}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$. This input overrides all other pixel information.
$\overline{SYNC}$	Composite Sync Input. A LOW on this input subtracts approximately 7mA from the I_{OG} analog output and overrides no other pixel information. For the correct $\overline{SYNC}$ level, this input should be LOW only when $\overline{BLANK}$ is also LOW. The $\overline{SYNC}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
Analog	
AGND	Analog Ground Power Supply, 0V.
VAA	Analog Power Supply, 5V.
VREF	Voltage Reference Input, 1.235V. This input supplies a reference voltage for the DAC circuitry. Care must be taken to correctly decouple this voltage because noise on this pin will couple directly to the DAC outputs.
FS ADJ	Full-Scale Adjust Input. The current flowing from this pin to AGND is directly proportional to the full-scale analog output current. Normally, a resistor is connected between this pin and AGND. The voltage on this pin is approximately equal to VREF. The relationship I_{OUT} (mA) = 11.294 x VREF (V)/RSET (KΩ).
I_{OUT}	DAC current output.
COMP	Compensation Input. This pin provides the ability to compensate the internal reference operational amplifier.
PLL	Phase Lock Loop Current Output. This high impedance current source is used to enable multiple IDT75C457s to be synchronized with sub-pixel resolution when used with an external PLL. A logic one on the $\overline{BLANK}$ input results in no current being output onto this pin, while a logic zero results in the following current being output: PLL (mA) = 3227 * VREF (V)/RSET (ohm). If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a register up to 150 ohms).

2523 tbl 04

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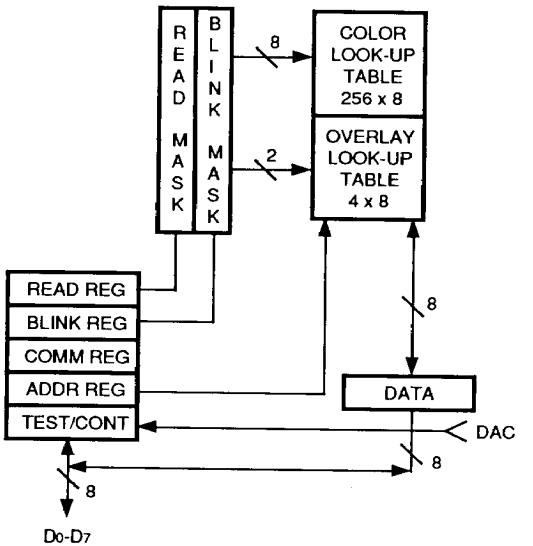


Figure 5. IDT75C457 Register Block Diagram

Command Register

The Command Register is accessed by reading or writing with the Address Register = $06, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

CR0 — OL0 Display Enable. This bit is ANDed internally with the data from OL0 prior to the palette selection. If CR0 is LOW, the internal OL0 bits are set LOW, allowing only overlay colors 0 and 2 to be selected.

CR1 — OL1 Display Enable. This bit is ANDed internally with the data from OL1 prior to the palette selection. If CR1 is LOW, the internal OL1 bits are set LOW, allowing only overlay colors 0 and 1 to be selected.

CR2 — OL0 Blink Enable. If this bit is set HIGH, the OL0 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR0 must be set HIGH for this function.

CR3 — OL1 Blink Enable. If this bit is set HIGH, the OL1 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR1 must be set HIGH for this function.

CR4, CR5 — Blink Rate Select. These bits select blink rates based on Vertical Sync cycles, defined as more than 256 $\overline{LD}$ cycles during BLANK.

CR6 — Color Palette RAM Enable. This bit specifies whether to use the Color Palette or the Overlay Palette when OL0 = OL1 = LOW.

CR7 — Multiplex Select. This bit selects between 4:1 (CR7 = 0) or 5:1 (CR7 = 1) multiplexing. When using 4:1 multiplexing the {E} inputs are never used and must be connected to a valid logic level.

Read Mask Register

The Read Mask Register is accessed by reading or writing with the Address Register = $04, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Blink Mask Register

The Blink Mask Register is accessed by reading or writing with the Address Register = $05, C0 = 0 and C1 = 1 (see Table 1). Each register bit causes the corresponding pixel bit (P0-P7) to internally switch between the input value and 0 at the blink rate specified in the Command Register. For this function to work, the corresponding enable bit in the Read Mask Register must be set HIGH. The Blink Mask Register may be read or written at any time. BMR7 (Blink Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Test/Control Register

The Test/Control Register is accessed by reading or writing with the Address Register = $07, C0 = 0 and C1 = 1 (see Table 1). This register allows the MPU to read the 8 input bits of the DAC. It may be written to or read by the MPU at any time, and is not initialized. The register bits are defined as follows:

D7-D4	DAC input data (one nibble)
D3	Upper (LOW) or Lower (HIGH) nibble select
D2	Blue enable
D1	Green enable
D0	Red enable

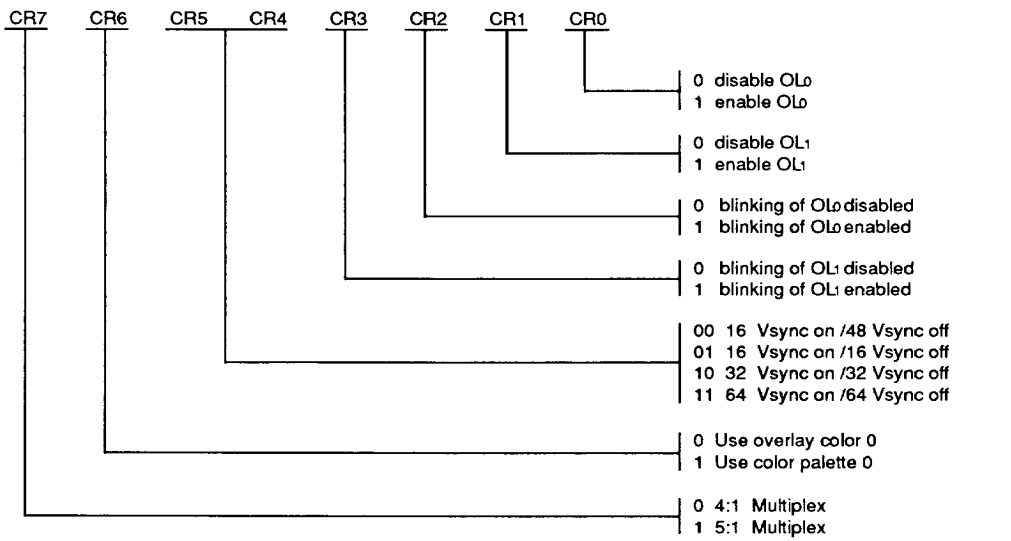
2523 tbl 05

When writing to the register, upper four bits (D4-D7) are ignored.

To use the test/control register, the MPU writes to it, specifying the upper or lower nibble of the 8-bit input information to the DAC. When the MPU reads the register, the four bits of color information from the DAC inputs are contained in the upper four bits of the register, and the lower four bits contain whatever was previously written to the register. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green and blue enable bits are also used to specify the mode of writing color data to, and reading color data from, the IDT75C457. If all three enable bits are a logic zero, each write cycle to the color palette or the overlay palette loads eight bits of color data. During each read cycle of the color palette or the overlay palette, eight bits of color data are output onto the data bus. If a 24-bit data bus is available, this enables three IDT75C457 to be accessed simultaneously.

If any of the red, green, blue bits are a logic one, the IDT75C457 assumes the MPU is reading or writing color information using red, green, blue cycles, such as are used on the IDT75C458. Setting the appropriate enable bit configures the IDT75C457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logic one, and a red, green, blue write cycle occurred, the IDT75C457 would input data only during the green write cycle. If a red, green, blue read cycle occurred, the IDT75C457 would output data only during the green read cycle. Note that $\overline{CE}$ must be a logic zero during each of the red, green, blue cycles. One, and only one, of the enable bits must be a logic one. This mode of operation is useful where only an 8-bit data bus is available and the software drivers are written for RGB operation.



2523 drw 09

Figure 6. Command Register Designations

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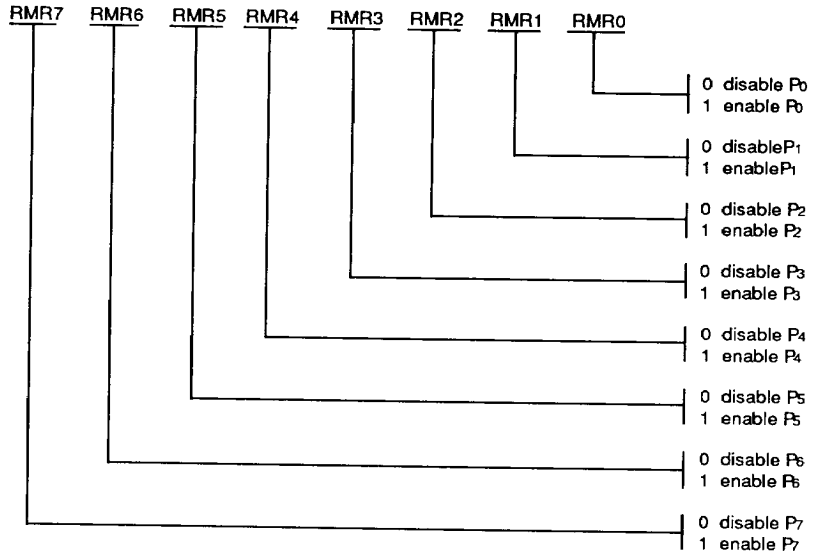

Figure 7. Read Mask Register Designations

2523 drw 010

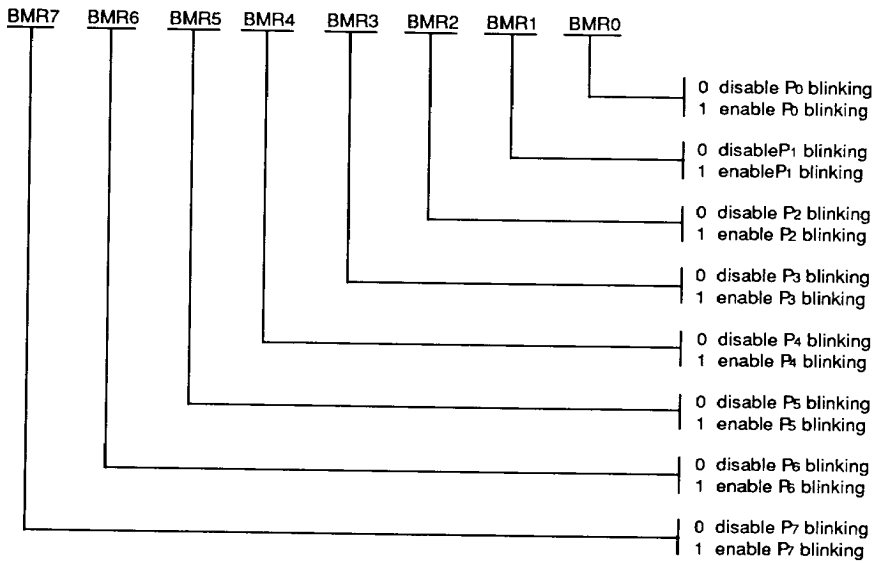

Figure 8. Blink Mask Register Designations

2523 drw 11

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
Power Supplies			
V_{AA}	Measured to AGND	−0.5 to +7.0	V
Input Voltage			
Applied Voltage (2)	Measured to AGND	−0.5 to V_{AA} +0.5	V
Output			
Applied Voltage (2)	Measured to AGND	−0.5 to V_{AA} +0.5	V
Applied Current (2, 3, 4)	Externally forced	−1.0 to +6.0	mA
Analog Output Short Circuit Duration	Analog output High to AGND	Indef	s
Temperature			
Operating	Military	−55 to +125	°C
Ambient	Commercial	0 to +70	°C
Storage	Military	−65 to +150	°C
	Commercial	−55 to +125	°C

2523 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{AA}	Power Supply	Measured to AGND	4.75	5.0	5.25	V
I_{AA}	Power Supply Current	V_{AA} = Typ., Static	–	120	–	mA
V_{IH} (1)	Input Voltage HIGH		2.0	–	V_{AA} + 0.5	V
V_{IL} (1)	Input Voltage LOW		AGND - 0.5	–	0.8	V
V_{CIH}	Clock Input Voltage HIGH		V_{AA} - 1.0	–	V_{AA} + 0.5	V
V_{CIL}	Clock Input Voltage LOW		AGND - 0.5	–	V_{AA} - 0.6	V
I_{IH}	Input Current HIGH	V_{IN} = 2.4V	–	–	1	µA
I_{IL}	Input Current LOW	V_{IN} = 0.4V	–	–	-1	µA
V_{OH}	Output Voltage HIGH	V_{AA} = Min., I_{OH} = -800µA	2.4	–	–	V
V_{OL}	Output Voltage LOW	V_{AA} = Min., I_{OL} = 6.4mA	–	–	0.4	V
I_{OZ}	Output 3-State Current		–	–	10	µA

NOTE:
1. All digital inputs except CLK and $\overline{CLK}$.

2523 tbl 07

AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0V, V_{IH} = 3V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} - 1.0V, V_{IL} = V_{AA} - 1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		'75C457-165(1)		'75C457-135(1)		'75C457-125		'75C457-110		'75C457-80		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
F_{CLK}	Clock Frequency	–	165	–	135	–	125	–	110	–	80	MHz
F_{CLD}	$\overline{LD}$ Clock Frequency	–	41	–	34	–	32	–	28	–	20	MHz
t_{CS}	Control Set-up Time, C0, C1, R/$\overline{W}$	0	–	0	–	0	–	0	–	0	–	ns
t_{CH}	Control Hold Time, C0, C1, R/$\overline{W}$	15	–	15	–	15	–	15	–	15	–	ns
t_{CEH}	$\overline{CE}$ HIGH Time	20	–	20	–	25	–	25	–	25	–	ns
t_{CEL}	$\overline{CE}$ LOW Time	30	–	30	–	50	–	50	–	50	–	ns
t_{CEZO}	$\overline{CE}$ to Data Bus Driven	10	–	10	–	10	–	10	–	10	–	ns
t_{CED}	$\overline{CE}$ to Data Valid	–	30	–	30	–	50	–	50	–	75	ns
t_{CEOZ}	$\overline{CE}$ to Data Bus Hi-Z	–	15	–	15	–	15	–	15	–	15	ns
t_{WDS}	Write Data Set-Up Time	30	–	30	–	35	–	35	–	50	–	ns
t_{WDH}	Write Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{CLKCY}	Clock Cycle Time	6	–	7.4	–	8	–	9	–	12	–	ns
t_{CLKPL}	Clock Pulse Width LOW	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{CLKPH}	Clock Pulse Width HIGH	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{LDCY}	$\overline{LD}$ Cycle Time	24	–	29	–	31	–	35	–	50	–	ns
t_{LDPH}	$\overline{LD}$ Pulse Width HIGH	10	–	12	–	13	–	15	–	20	–	ns
t_{LDPL}	$\overline{LD}$ Pulse Width LOW	10	–	12	–	13	–	15	–	20	–	ns
t_{PS}	Pixel Data Set-up Time	2	–	3	–	3	–	3	–	4	–	ns
t_{PH}	Pixel Data Hold Time	1	–	2	–	2	–	2	–	2	–	ns
I_{AAD}	Dynamic Supply Current Commercial Temp.	–	270	–	250	–	230	–	210	–	190	mA
I_{AAD}	Dynamic Supply Current Military Temp.	–	–	–	–	–	260	–	240	–	220	mA

NOTE:
1. 165 and 135 specification over commercial temperature only.

2523 tbl 08

ANALOG OUTPUT DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Res	Resolution			–	8	–	bits
I_{LSB}	LSB Current Size			–	69.1	–	µA
L_I			1 LSB Version	–	1/2	±1	LSB
			1/2 LSB Version	–	1/4	±1/2	LSB
L_D			1 LSB Version	–	1/2	±1	LSB
			1/2 LSB Version	–	1/4	±1/2	LSB
V_{OC}	Output Compliance Voltage			-1.0	–	1.2	V
R_{AOUT} (2)	Output Impedance				50		kΩ
C_{AOUT} (2)	Output Capacitance	f = 1MHz, I_{OUT} = 0mA			8	12	pF
I_{REF}	V_{REF} Input Current				10		µA
E_M	Matching Error (DAC to DAC)			–	2	5	%
PSRR	Power Supply Rejection Ratio			–	50	–	dB
I_W (1)	White Current	Measured to Blank		17.69	19.05	20.40	mA
I_B (1)	Black Current	Measured to Blank		0.95	1.44	1.90	mA
I_{BLANK}	Blank Current IO_R, IO_B			0	5	50	µA
I_{BLANK} (1)	Blank Current IO_G			6.29	7.62	8.96	mA
I_{SYNC}	Sync Current IO_G			0	5	50	µA

NOTES:
1. R_{SET} = 523Ω, V_{REF} = 1.235V
2. This parameter is guaranteed but not tested in production.

2523 tbl 09

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ANALOG OUTPUT AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} - 1.0V, V_{IL} = V_{AA} - 1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		'75C457-165 (3)			'75C457-135 (3)			'75C457-125			'75C457-110			'75C457-80			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
F_{CLK}	Clock Frequency	–	–	165	–	–	135	–	–	125	–	–	110	–	–	80	MHz
t_{VD}	Video Output Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns
t_{VT}	Video Output Transition Time	–	1.5	–	–	1.7	–	–	1.8	–	–	2	–	–	2	–	ns
t_S	Video Output Skew	–	0	<2	–	0	<2	–	0	<2	–	0	<2	–	0	<2	ns
t_S	Video Ouput Setting Time	–	6	–	–	7	–	–	8	–	–	8	–	–	12	–	ns
FT	Clock and Data Feedthrough	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
GE	Glitch Energy	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
CT	Crosstalk, DAC to DAC	–	100	–	–	100	–	–	100	–	–	100	–	–	100	–	pV-s
t_{VP}	Pipeline Delay	9	–	9	9	–	9	9	–	9	9	–	9	9	–	9	clock
t_{PLL}	PLL Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns

NOTES:
1. C_L = 10pF, 10%-90% points.
2. This parameter is guaranteed but not tested in production.
3. 165 and 135 MHz over commercial temperature range only.

2523 tbl 10

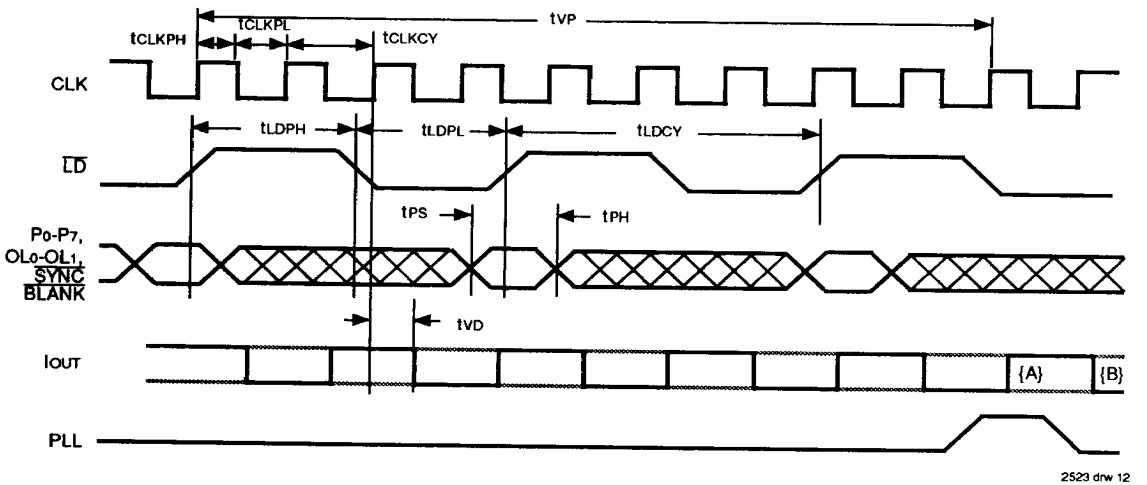


Figure 9. Video I/O Timing Diagram

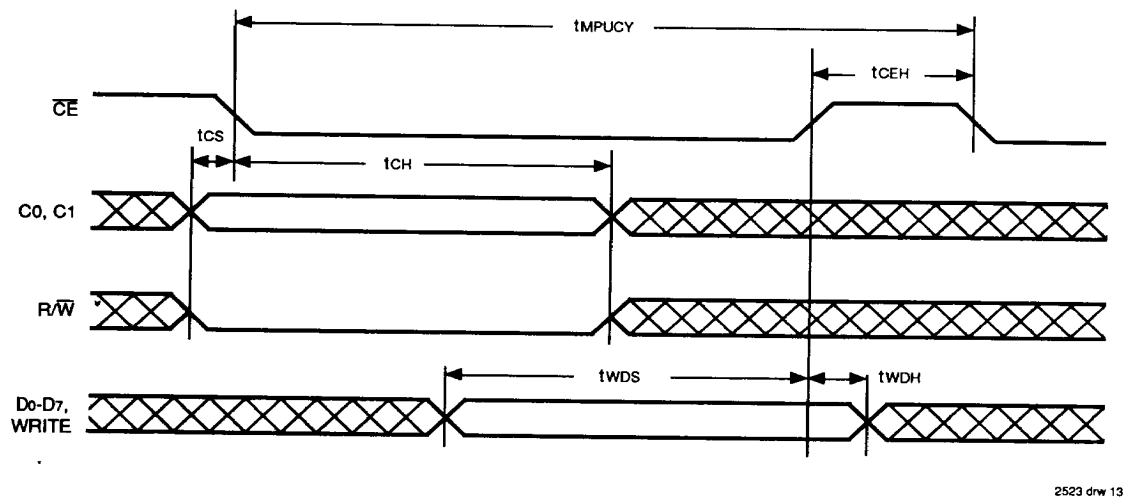


Figure 10. MPU WRITE Timing Diagram

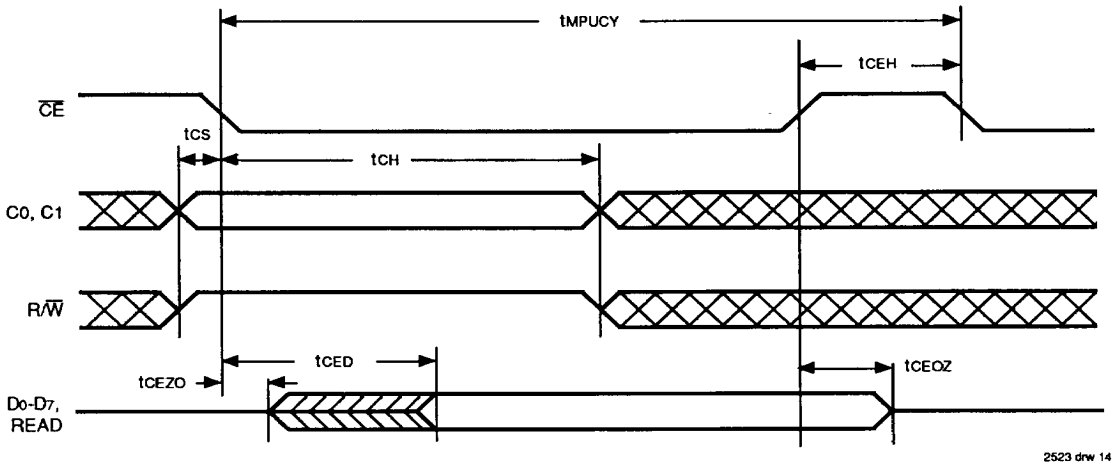
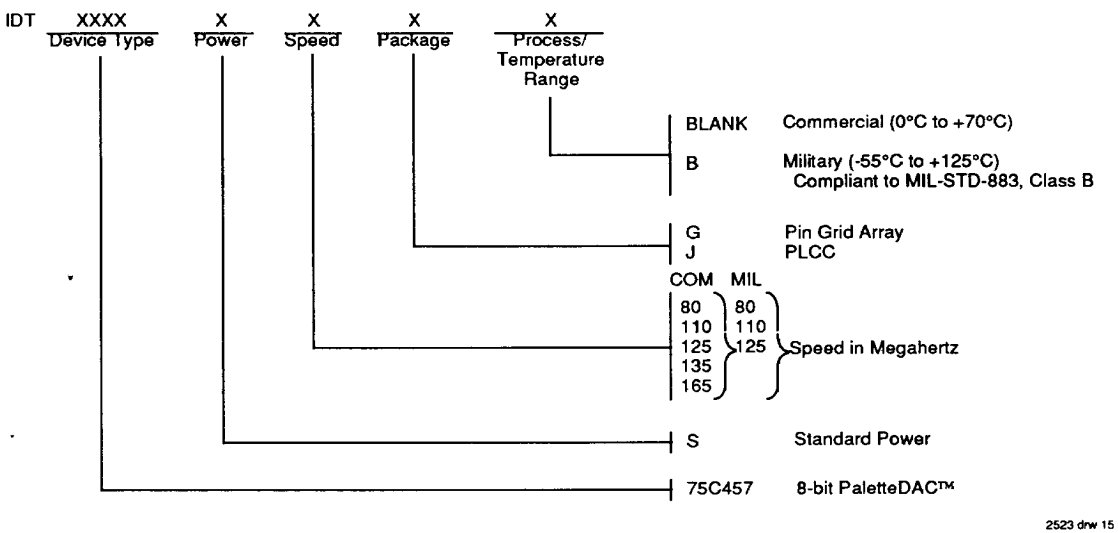


Figure 11. MPU READ Timing Diagram

ORDERING INFORMATION



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