Low Skew Output Buffer

General Description

The **ICS9176** is designed specifically to support the tight timing requirements of high-performance microprocessors and chip sets. Because the jitter of the device is limited to ±250ps, the **ICS9176** is ideal for clocking Pentium™ systems. The 10 high drive (40mA), low-skew (±250ps) outputs make the **ICS9176** a perfect fit for PCI clocking requirements.

The **ICS9176** has 10 outputs synchronized in phase and frequency to an input clock. The internal phase locked loop (PLL) acts either as a 1X clock multiplier or a 1/2X clock multiplier depending on the state of the input control pins T0 and T1. With metal mask options, any type of ratio between the input clock and output clock can be achieved, including 2X.

The PLL maintains the phase and frequency relationship between the input clock and the outputs by externally feeding back FBOUT to FBIN. Any change in the input will be tracked by all 10 outputs. However, the change at the outputs will happen smoothly so no glitches will be present on any driven input. The PLL circuitry matches rising edges of the input clock and the output clock. Since the input to FBIN skew is guaranteed to ±500ps, the part acts as a "zero delay" buffer.

The **ICS9176** has a total of eleven outputs. Of these, FBOUT is dedicated as the feedback into the PLL and another, Q/2, has an output frequency half that of the remaining nine. These nine outputs can either be running at the same speed as the input, or at half the frequency of the input. With Q/2 as the feedback to FBIN, the nine 'Q' outputs will be running at twice the input frequency in the normal divide-by-1 mode. In this case, the output can go to 120 MHz with a 60 MHz input clock. The maximum rise and fall time of an output is 14ns and each is TTL-compatible with a 40mA symmetric drive.

The **ICS9176** is fabricated using CMOS technology which results in much lower power consumption and cost compared with the gallium arsenide based 1086E. The typical operating current for the **ICS9176** is 60mA versus 115mA for the GA1086E.

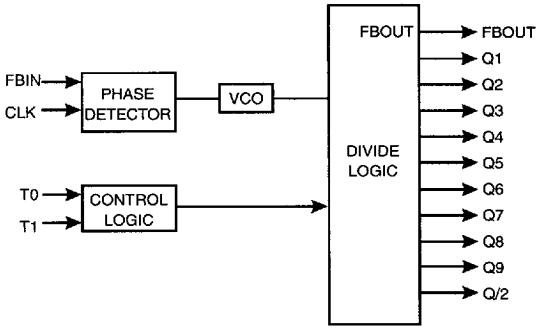
Features

- **ICS9176-01** is pin compatible with Triquint GA1086
- ±500ps skew (max) between input and outputs
- ±250ps skew (max) between outputs
- 10 symmetric, TLL-compatible outputs
- 28-pin PLCC surface mount package
- High drive, 40mA outputs
- Power-down option
- Output frequency range 20 MHz to 120 MHz
- Input frequency range 20 MHz to 100 MHz
- Ideal for PCI bus applications

Selection Table

T_1	T_0	DESCRIPTION
0	0	Power-down
0	1	Test Mode (PLL Off CLK=outputs)
1	0	Normal (PLL On)
1	1	Divide by 2 Mode

Block Diagram



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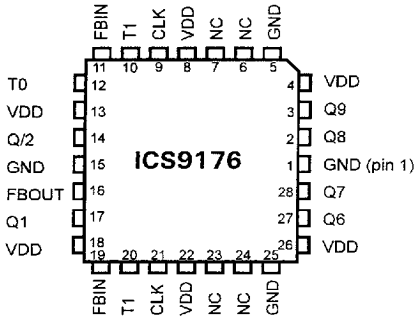
Pin Configuration

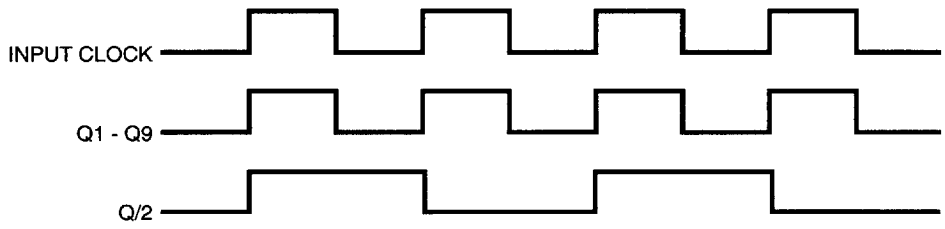


28-Pin PLCC
K-10

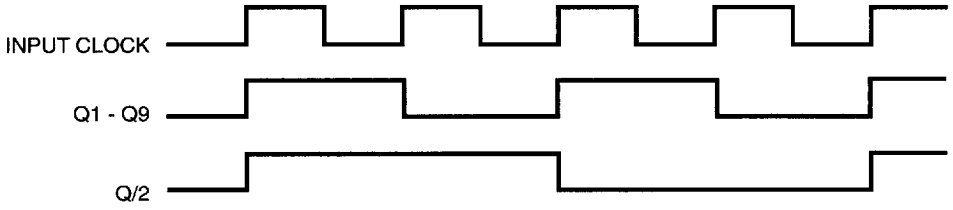
Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND.
2	Q8	Output	Output clock 8.
3	Q9	Output	Output clock 9.
4	VDD	-	Power supply (+5V).
5	GND	-	GROUND.
6	NC	-	No Connect.
7	NC	-	No Connect.
8	VDD	-	Power supply (+5V).
9	CLK	Input	Input for reference clock.
10	T1	Input	T1 selects normal operation, power-down, or test mode.
11	FBIN	Input	FEEDBACK INPUT from output FBOUT.
12	T0	Input	T0 selects normal operation, power-down, or test mode.
13	VDD	-	Power Supply (+5V).
14	Q/2	Output	Half-clock output.
15	GND	-	GROUND.
16	FBOUT	Output	FEEDBACK OUTPUT to Input FBIN.
17	Q1	Output	Output clock 1.
18	VDD	-	Power Supply (+5V).
19	GND	-	GROUND.
20	Q2	Output	Output clock 2.
21	Q3	Output	Output clock 3.
22	VDD	-	Power supply (+5V).
23	Q4	Output	Output clock 4.
24	Q5	Output	Output clock 5.
25	GND	-	GROUND.
26	VDD	-	Power Supply (+5V).
27	Q6	Output	Output clock 6.
28	Q7	Output	Output clock 7.

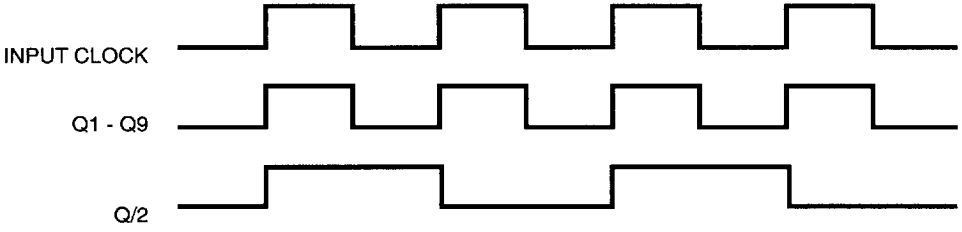
Timing Diagrams



Timing in Divide by 1 Mode

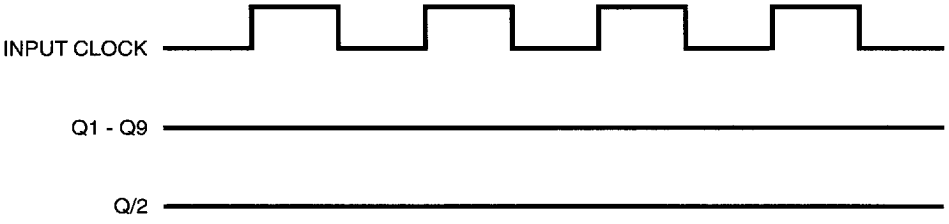


Timing in Divide by 2 Mode



Timing in Eliminate by Test Mode

Note: In test mode, the VCOs are bypassed. The test clock input is simply buffered, then output. The part is transparent. Damage to the device may occur if an output is shorted or forced to ground or VDD.



Timing in Power-down Mode

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating Temperature under bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on I/O pins referenced to GND ..... GND -0.5V to VDD +0.5V
Power Dissipation ..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

DC Characteristics

V_{DD} = +5V±5%, T_A=0°C to 70°C unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Current	I_i	V_{IN}=0V, 5V	-5	-	5	µA
Output Low Voltage	V_{OL}	@I_{OL}=14mA	-	0.25	0.4	V
Output Low Current	I_{OL}	@V_{OL}=0.8V	33	42	-	mA
Output High Voltage	V_{OH}	@I_{OH}=-38mA	2.4	-	-	V
Output High Current	I_{OH}	@V_{OH}=2.0V	-	-59	-41	mA

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Pulse Width*	CLK_W	Vdd=4.5V, f_{CLK}=100 MHz	2.5	-	7.5	ns
Output Rise time, 0.8 to 2.0V*	t_r	15 pf load	-	0.7	1	ns
Rise time, 20% to 80% V_{DD}*	t_r	15 pf load	-	1.5	2	ns
Output Fall time, 2.0V to 0.8V*	t_f	15 pf load	-	0.7	1	ns
Fall time, 80% to 20% V_{DD}*	t_f	15 pf load	-	1.2	2	ns
Output Duty cycle*	d_t	15 pf load	45	49/51	55	%
Jitter, 1 sigma*	T_{ls}			60		ps
Jitter, absolute*	T_{abs}		-250	±100	250	ps
Input Frequency	f_i		20		100	MHz
Output Frequency (Q outputs)	f_o		20		120	MHz
FBIN to IN skew	t_{skew1}	Note 1, 3. Input rise time <3ns	-500	250	0	ps
Skew between any 2 outputs at same frequency	t_{skew2}	Note 1, 3.	-250	50	250	ps
Skew between any 1 output and Q/2					3	ns

NOTES:
1. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
2. Duty cycle measured at 1.4V.
3. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

* Guaranteed by design and characterization. Not subject to 100% test.

Applications

FBOUT is normally connected to FBIN to facilitate input to output skew control. However, there is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. As long as the signal at FBIN is derived directly from the FBOUT pin and maintains its frequency, additional delays can be accommodated. The clock phase of the outputs (rising edge) will be adjusted so that the phase of FBIN and the input clock will be the same. See Figure 1 for an example.

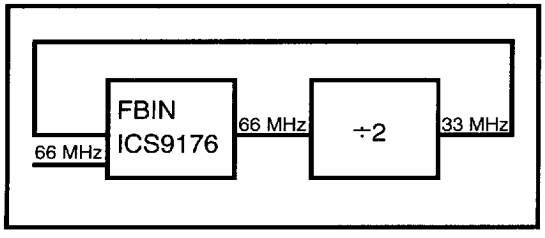


Figure 1

In Figure 1, the propagation delay through the divide by 2 circuit is eliminated. The internal phase-locked loop will adjust the output clock on the **ICS9176** to ensure zero phase delay between the FBIN and CLK signals, as a result, the rising edge at the output of the divide by two circuit will be aligned with the rising edge of the 66 MHz input clock. This type of configuration can be used to eliminate propagation delay as long as the signal at FBIN is continuous and is not gated or conditional.

The **ICS9176** is also ideal for clocking multi-processor systems. The 10 outputs can be used to synchronize the operation of CPU cache and memory banks operating at different speeds. Figure 2 depicts a 2-CPU system in which processors and associated peripherals are operating at 66 MHz. Each of the nine outputs operating at 66 MHz are fully utilized to drive the appropriate CPU, cache and memory control logic. The 33 MHz output is used to synchronize the operation of the slower memory bank to the restart of the system.

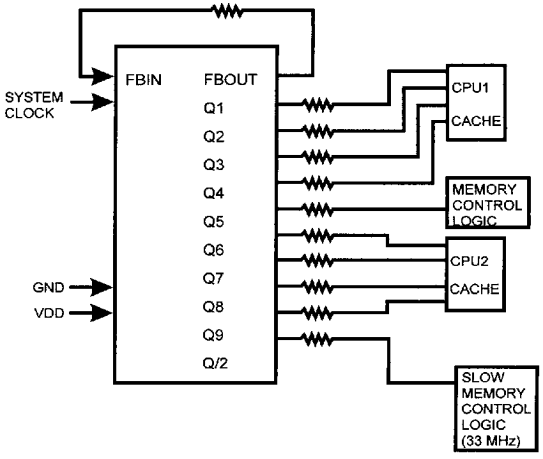


Figure 2

Ordering Information

ICS9176-01CQ28

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
Q=PLCC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device