

DESCRIPTION

The Hyundai HY51C264 is high-speed, dual access 262, 144 bit (256K) CMOS dynamic random-access memory components. Fabricated with CMOS technology, the HY51C264 offers TURBOMODE operation of the serial output data to achieve hesitation free operation at serial data lengths up to the full 256 (64K×4).

Refresh is accomplished by performing $\overline{\text{RAS}}$ only cycles, read cycles, write cycles or read-modify-write cycles to each of the 256 row addresses during a 4 ms period. Refreshing can also be accomplished by $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles using the internal refresh counter.

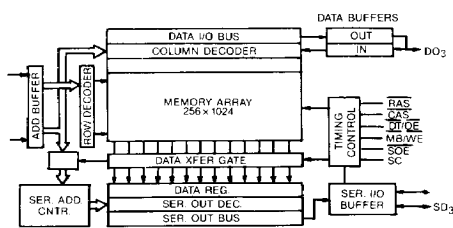
All inputs and outputs are TTL compatible. Address lines and data-in are latched on-chip to simplify system design. Data-out is unlatched for system flexibility. Operation of the HY51C264 is guaranteed over a temperature range of 0°C to 70°C and at a V_{CC} of 4.5 to 5.5 VDC. The HY51C264 is packaged in 24 pin dual-in-line packages for insertion into mounting holes on 400 mil (10.16mm) centers.

FEATURES

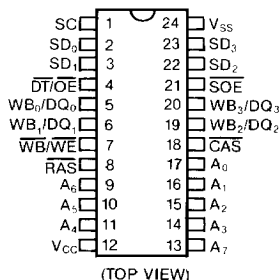
- ▲ 64K×4 CMOS dynamic RAM
- ▲ Dual accessibility.... one serial read port, one random access port
- ▲ Fast serial read output..25 ns cycle time (HY51C264A)
- ▲ TURBOMODE operation on serial read port allows serial transfer of entire memory content without interruption.
- ▲ RAM port exactly like 64K×4 dynamic RAM
- ▲ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- ▲ All outputs and inputs fully TTL compatible
- ▲ 3-State unlatched outputs for random and serial access
- ▲ Low power dissipation (HY51C264)
 - Operating current 70mA (max)
 - Standby (TTL) 3 mA (max)
 - Standby (CMOS) 100 μA (max)

RANDOM ACCESS PORT	HY51C264-12	HY51C264-15
Maximum Access Time (ns)	120	150
Minimum Cycle Time (ns)	230	260
Maximum Column Address Access Time (ns)	60	70
SERIAL ACCESS PORT		
Maximum Shift Frequency (MHz)	40	25

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{\text{SOE}}$	Serial Output Enable
$\text{SD}_{0,3}$	Serial Read Output
$\overline{\text{DT/OE}}$	Data Transfer/Output Enable
$\text{WB}_{0,3}$	Write Sel. in per Bit
$\text{DQ}_{0,3}$	Data in and Data Out
$\overline{\text{WB/WE}}$	Write per Bit/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\text{A}_{0,7}$	Address Inputs
V_{CC}	5V Supply
$\overline{\text{CAS}}$	Column Address Strobe
SC	Serial Clock
V_{SS}	Ground