HM62A932 Series — Preliminary

32k x 9 Data Cache RAM

■ DESCRIPTION

The Hitachi HM62A932 is a high speed 288-kbit synchronous static cache RAM optimized for use in secondary caches for 32-bit microprocessor system. This RAM has a 32-kword x 9-bit organization for building a 32k x 32-bit cache data array, with byte parity by using four of these chips. The HM62A932 is available in a 44-pin PLCC for high density mounting.

(CP-44)

■ FEATURES

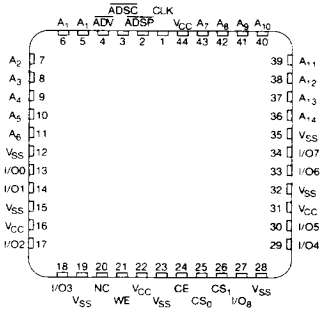
- 32-kword x 9-bit organization
- Synchronous read and write
- Internal burst read/write address counter
- Self-timed write
- Matches timing of 50 MHz 32-bit micro processor
- Additional address strobe input for implementing extended burst

■ ORDERING INFORMATION

Type No.	Access Time	CPU Clock Rate	Package
HM62A932CP-14	14 ns	50 MHz	44-pin PLCC
HM62A932CP-19	19 ns	40 MHz	
HM62A932CP-24	24 ns	33 MHz	
HM62A932CP-34	34 ns	25 MHz	

■ PIN ARRANGEMENT

HM62A932 Series



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
CLK	Clock Input
$\overline{ADSP}$	Address Status Input from MPU
$\overline{ADSC}$	Address Status Input from the Cache Controller
CS0, $\overline{CS_1}$	Complementary Chip Select Input
A0-A14	Base Address Input
$\overline{ADV}$	Synchronous Address Advance Input
$\overline{WE}$	Synchronous Write Enable Input
$\overline{OE}$	Asynchronous Data Output Enable Input
I/O0–I/O7, I/O8	Input/Output Data Pin
NC	No Connection

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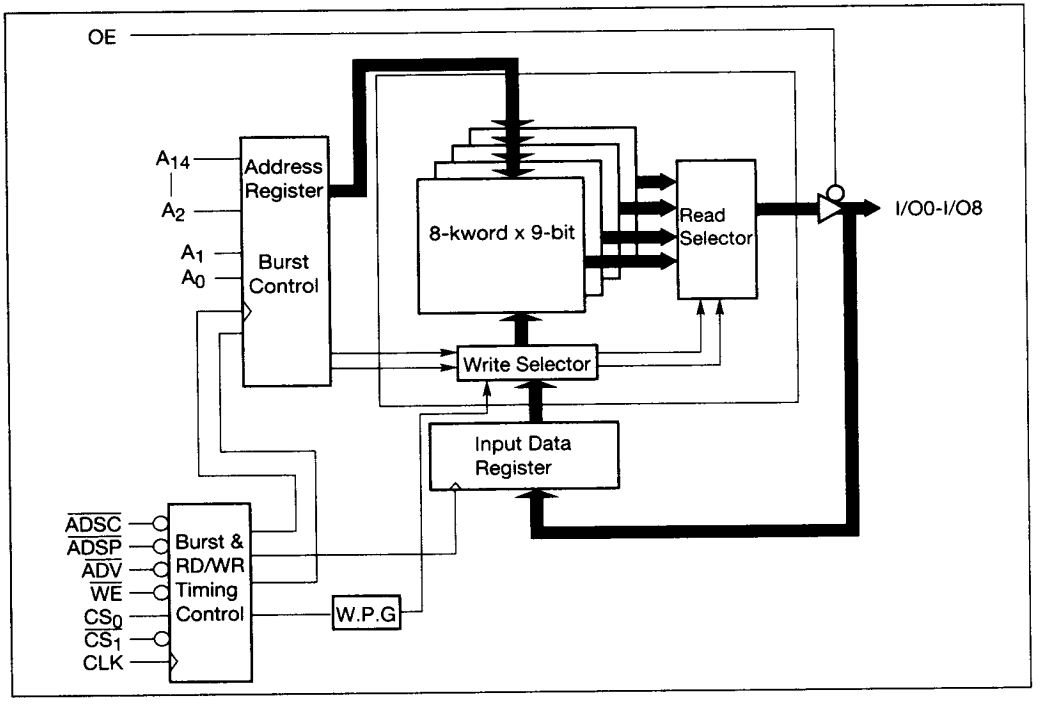
■ BLOCK DIAGRAM



■ FUNCTION TABLE

Table 1. Synchronous Operation

CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	CLK	I/O Pin	Function
X	H	X	X	X	X	↗	High-Z	Disable
L	X	X	X	X	X	↗	High-Z	Disable
H	L	L	X	X	X	↗	Output	Latch Base Address Read Address
H	L	H	L	X	L	↗	Input	Latch Base Address Sample Write Data Start a Self-Timed Write
H	L	H	L	X	H	↗	Output	Latch Base Address Read Access
H	L	H	H	L	L	↗	Input	Sample Write Data Advance Burst Count Start a Self-Timed Write
H	L	H	H	L	H	↗	Output	Advance Burst Count Read Access
H	L	H	H	H	L	↗	Input	Start a Self-Timed Write
H	L	H	H	H	H	↗	Output	Read Access

X = Don't care, H = High, L = Low, High-Z = High Impedance

Table 2. Asynchronous Output Control (See Notes 2 and 3 Below)

$\overline{OE}$	I/O Pin
L	Output
H	High-Z

Notes:
1. Two separate address strobe inputs are provided and both will load a new base address. $\overline{ADSP}$, from the MPU will override all other functions and cause a read access to the base address. $\overline{ADSC}$, from the controller, is affected by $\overline{WE}$ if $\overline{ADSP}$ is inactive, and $\overline{ADSC}$ will start either a read or write cycle to the base address.
2. The CS_0 and $\overline{CS_1}$ inputs are sampled with the addresses when $\overline{ADSP}$ or $\overline{ADSC}$ is sampled active. Only if CS_0 and $\overline{CS_1}$ are sampled active will $\overline{WE}$ or $\overline{OE}$ affect the chip.
3. Any time $\overline{WE}$ is active when $\overline{ADSP}$ is inactive, a self-timed write will start.
4. During data read cycles, data is always presented asynchronously with clock after $\overline{OE}$ becomes low.
5. If the asynchrous $\overline{OE}$ signal is activated during a self-timed write cycle, I/O pins will be in High-Z state.
6. $\overline{OE}$ must not be driven by any controller when setting up for a write cycle, since the data collision would corrupt the write data.

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Pin Description

CLK	Clock input signal. It samples all of the input signals except $\overline{OE}$.
$\overline{ADSP}$	Address status input signal from MPU. When activated, a new "base" address is latched and an internal read access is performed. All other synchronous inputs are ignored when it is sampled active.
$\overline{ADSC}$	Address status input signal from the cache controller. When activated, a new "base" address is latched. Used during extended burst, and write-back cases when the cache controller must tell the device what addresses to access.
CS_0, $\overline{CS_1}$	Complementary chip select input signals. These are sampled along with the addresses when $\overline{ADSP}$ or $\overline{ADSC}$ is sampled. For any read/write or data bus activity to occur, CS_0 must be sampled high and $\overline{CS_1}$ must be sampled low.
A_0, A_{14}	Base address input signals. They are sampled when $\overline{ADSP}$ or $\overline{ADSC}$ is active. A_0–A_{14} may change after $\overline{ADSP}$ or $\overline{ADSC}$ samples them. A_1 and A_0 are latched and modified by the internal burst counter which XORs the bits in a certain burst order.
$\overline{ADV}$	Address advance input signal. When $\overline{ADV}$ is sampled active, and $\overline{ADSP}$ and $\overline{ADSC}$ are both sampled inactive, $\overline{ADV}$ will increment the burst counter prior to a read or write access. If $\overline{ADV}$ and $\overline{WE}$ are sampled active, the address will be incremented before a self-timed write starts. If $\overline{ADV}$ is sampled active with $\overline{WE}$ inactive, the address will be incremented before a read access starts.
$\overline{WE}$	Write enable input signal. When $\overline{WE}$ is sampled active and $\overline{ADSP}$ is sampled inactive, a self-timed write will start. When $\overline{WE}$ is sampled inactive, a self-timed write will start. When $\overline{WE}$ is sampled inactive, a read access will start. Active $\overline{WE}$ with $\overline{ADSC}$ active will cause a write to occur.
$\overline{OE}$	Asynchronous data output enable signal input. When active, the I/O pins will be driven will be driven with the read data available inside chip. $\overline{OE}$ activated while an internal self-timed write is in progress will cause the I/O pins to be High-Z. $\overline{OE}$ must be activated while an internal self-timed write is in progress will cause the I/O pins to be High-Z. $\overline{OE}$ must be inactive with enough margin before a self-timed write is started to guarantee that no data bus contention occurs.
I/O_0, I/O_8	Input/Output data pins.

■ FUNCTIONAL DESCRIPTION

This cache RAM contains both data and address edge triggered latches to perform high speed synchronous accesses. These latches, combined with internal self-timed write logic, allow the write decision to be postponed until it is known that a write must be done.

An internal burst address counter is provided to support burst read and burst write cycles. The counter sequences through the four internal bytes on the rising edge of the clock when input is sampled active. If the device reaches end of the normal burst sequence, the counter will wrap-around to the initial base address.

The rules for handling the low order address bits during a burst sequence is shown here (the low order address bits):

Initial access:	Use base address provided with $\overline{ADSC}$ or $\overline{ADSP}$
Next burst access:	Invert only base address A_0
Next burst access:	Invert only base address A_1
Next burst access:	Invert only base address A_1–A_0
Next burst access:	Wrap-around, use initial base address

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.2	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_T min = −2.5 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Active Operating Power Supply Current	I_{CC}	—	—	TBD	mA	TBD
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} =3.2 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −2.0 mA

Note: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading

■ CAPACITANCE (T_a = 25°C, f = 1 MHz)*1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

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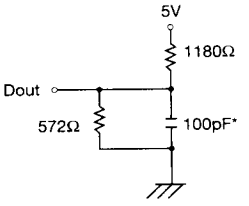
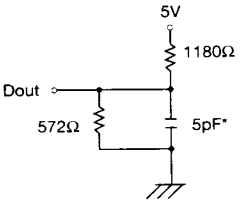
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Test Conditions

- Input and Output timing reference levels: 1.5V
- Input pulse levels: V_{SS} to 3V
- Input rise and fall times: 3ns
- Output load: See figures



Output Load (A)



Output Load (B)
(for t_{OLZ} & t_{OHZ})

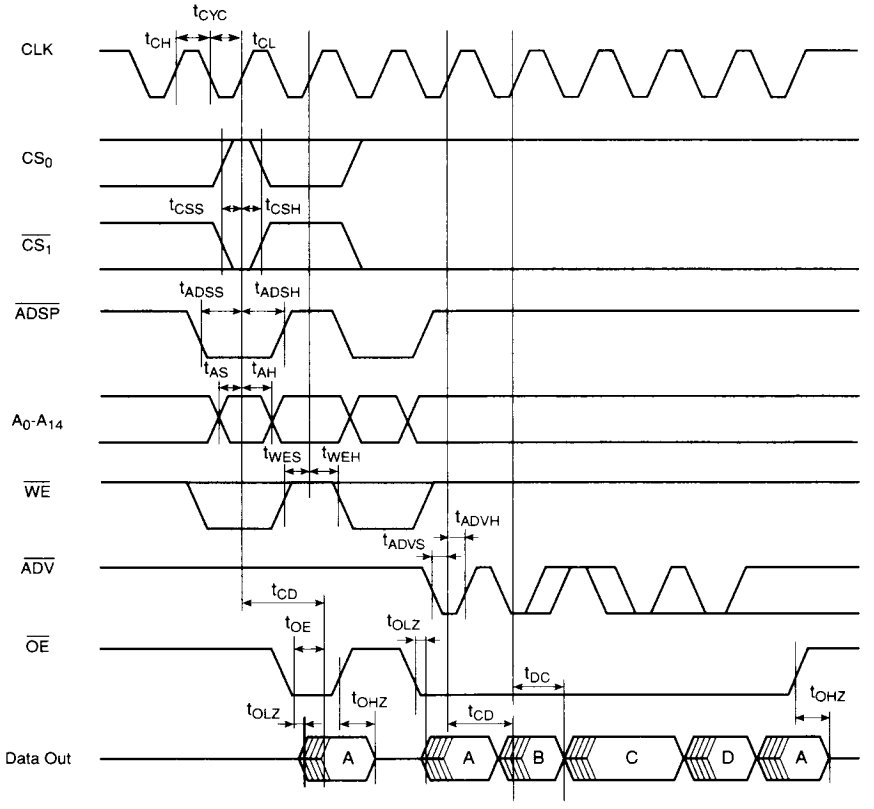
* Including scope & jig.

Parameter	Symbol	HM62A932-14		HM62A932-19		HM62A932-24		HM62A932-34		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tCYC	20	—	25	—	30	—	40	—	ns
Clock Pulse High	tCH	8	—	9.5	—	11	—	14	—	ns
Clock Pulse Low	tCL	8	—	9.5	—	11	—	14	—	ns
Address Setup Time	tAS	3	—	3	—	5	—	5	—	ns
ADS Setup Time	tADSS	3	—	3	—	5	—	5	—	ns
Output Select Setup Time	tCSS	3	—	3	—	5	—	5	—	ns
Address Hold Time	tAH	2	—	2	—	3	—	3		ns
ADS Hold Time	tADSH	2	—	2	—	3	—	3	—	ns
Chip Select Hold Time	tCSH	2	—	2	—	3	—	3		ns
Input Data Setup Time	tDS	3	—	3	—	5	—	5	—	ns
ADV Setup Time	tADVS	3	—	3	—	5	—	5	—	ns
Write Enable Setup Time	tWES	3	—	3	—	5	—	5	—	ns
Input Data Hold Time	tDH	2	—	2	—	3	—	3	—	ns
ADV Hold Time	tADVH	2	—	2	—	3	—	3	—	ns
Write Enable Hold Time	tWEH	2	—	2	—	3	—	3	—	ns
Clock to Output Valid	tCD	—	14	—	19	—	24	—	34	ns
Output Enable Low to Output Valid	tOE	—	7	—	8	—	9	—	10	ns
Output Enable Low to Output Low-Z	tOLZ*1,*2	0	—	0	—	0	—	0	—	ns
Read Data Hold After New Clock	tDC	3	—	3	—	3	—	3	—	ns
Output Enable High to Output High-Z	tOHZ*1,*2	—	7	—	8	—	9	—	10	ns
System Clock Skew	tSKEW	—	1	—	1	—	1	—	1	ns
Frequency		50		40		33		25		MHz

Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORMS

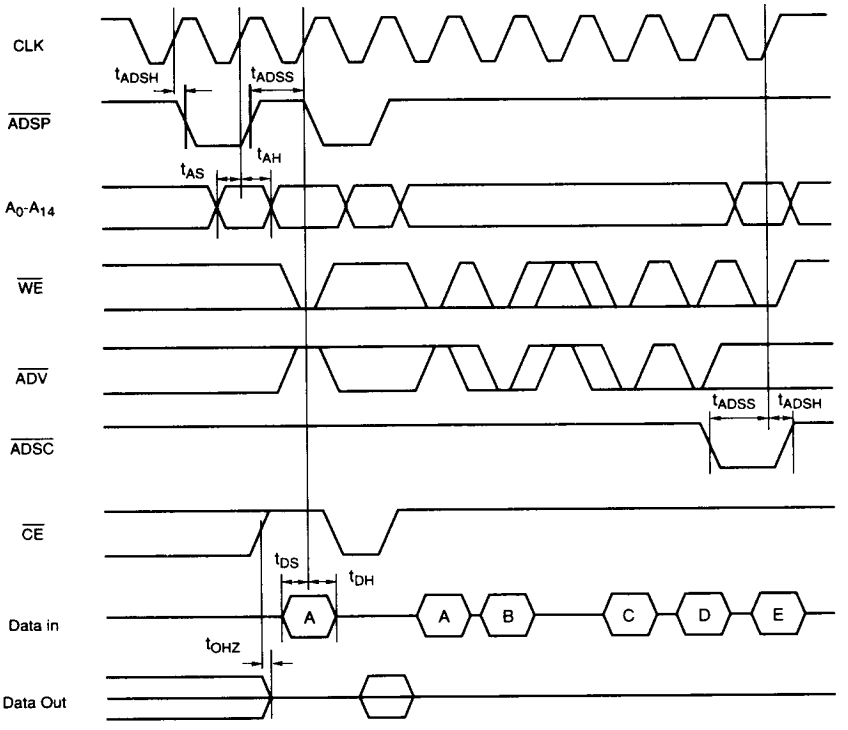
(1) Read Cycle Followed by Burst with Wait State Added to Data C



A–Data from Base ADDR
B–Data from Base ADDR except A_0 is now $\overline{A_0}$
C–Data from Base ADDR except A_1 is now $\overline{A_1}$
D–Data from Base ADDR except A_0 and $\overline{A_1}$ are now $\overline{A_0}$ and $\overline{A_1}$

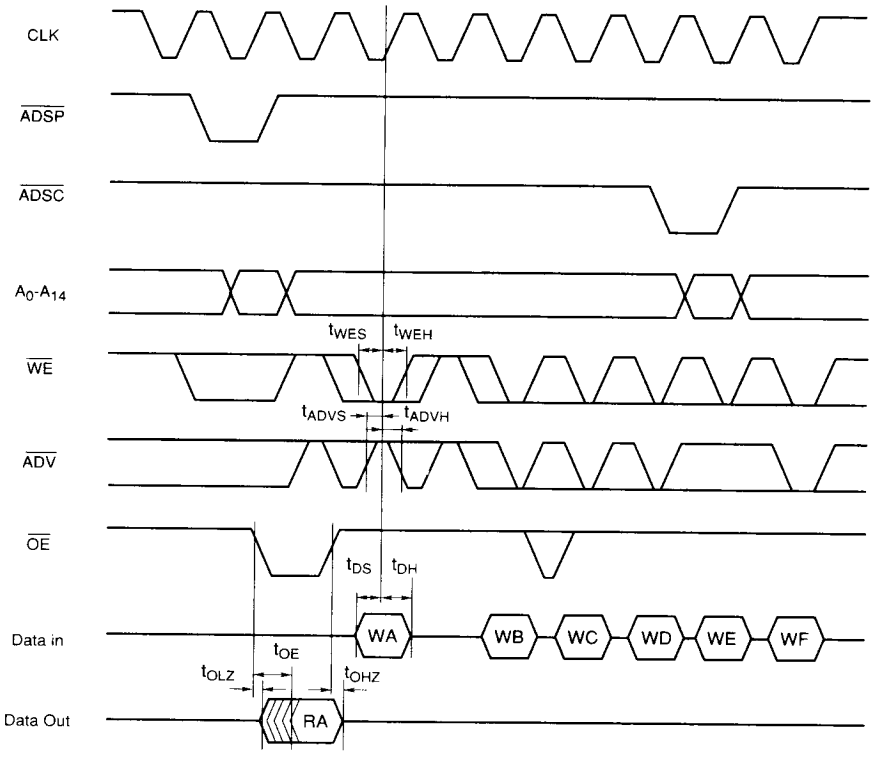
Note: 1. If $\overline{ADSP}$ or $\overline{ADSC}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.

(2) Write Cycle Followed by Burst Write with Wait State Added to Data C



A–Data to be written to Base ADDR
B–Data to be written to Base ADDR except A_0 is now $\overline{A}_0$
C–Data to be written to Base ADDR except A_1 is now $\overline{A}_1$
D–Data to be written to Base ADDR except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$
E–Data to be written to new Base ADDR loaded by $\overline{ADSC}$

(3) Burst Mixed Read/Write Cycles



RA–Data from Base ADDR
WA–Data to be written to Base ADDR
WB–Data to be written to Base ADDR except A_0 is now $\overline{A}_0$
WC–Data to be written to Base ADDR except A_1 is now $\overline{A}_1$
WD–Data to be written to Base ADDR except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$
WE–Data to be written to new Base ADDR
WF–Data to be written to new Base ADDR except A_0 is now $\overline{A}_0$

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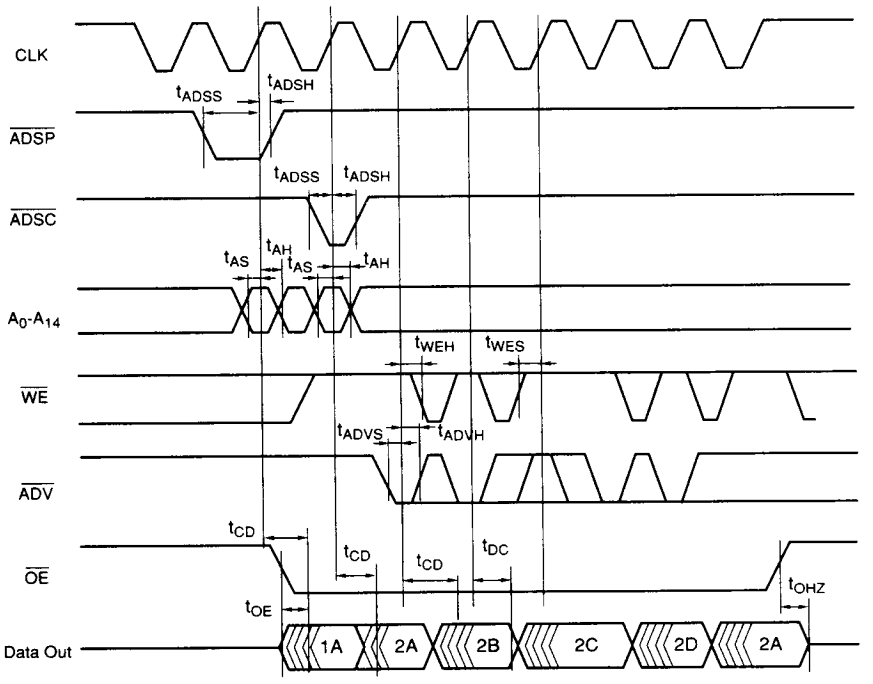
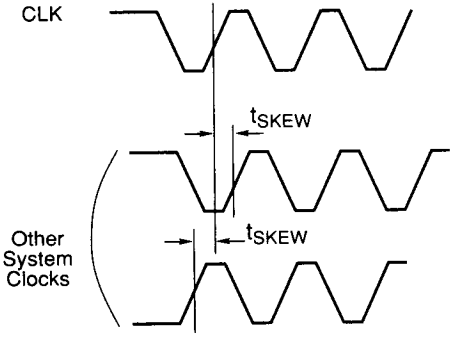
(4) Sequencial $\overline{ADSP}$/$\overline{ADSC}$ Cycles



1A–Data from Base ADDR1
2A–Data from Base ADDR2
2B–Data from Base ADDR2 except A_0 is now $\overline{A}_0$
2C–Data from Base ADDR2 except A_1 is now $\overline{A}_1$
2D–Data from Base ADDR2 except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$

(5) System Clock Skew Requirements



For this synchronous memory to meet its system timing requirements, the system clock skew must not exceed the specified range. Larger clock skews will require smaller clock-to-access times (t_{CD}).