Data Sheet | March 9, 2006 | FN7490.1

Micropower, Single Supply, Rail-to-Rail Input-Output Instrumentation Amplifiers

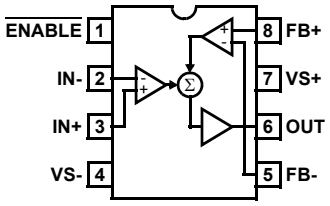
The EL8170 and EL8173 are micropower instrumentation amplifiers optimized for operation at 2.9V to 5V single supplies. Inputs and outputs can operate rail-to-rail. As with all instrumentation amplifiers, a pair of inputs provide very high common-mode rejection and are completely independent from a pair of feedback terminals. The feedback terminals allow zero input to be translated to any output offset, including ground. A feedback divider controls the overall gain of the amplifier.

The EL8170 is compensated for a gain of 100 or more, and the EL8173 is compensated for a gain of 10 or more. The EL8170 and EL8173 have bipolar input devices for best offset and 1/f noise performance.

The amplifiers can be operated from one lithium cell or two Ni-Cd batteries. The EL8170 and EL8173 input range includes ground to slightly above positive rail. The output stage swings to ground and positive supply - no pull-up or pull-down resistors are needed.

Pinout

EL8170, EL8173
(8 LD SO)
TOP VIEW



Features

- 78µA maximum supply current
- Maximum offset voltage
  - 250µV (EL8170)
  - 1000µV (EL8173)
- 500pA input bias current
- 2µV/°C offset voltage drift
- 396kHz -3dB bandwidth (G = 10)
- 192kHz -3dB bandwidth (G = 100)
- 0.5V/µs slew rate
- Single supply operation
  - Input voltage range is rail-to-rail
  - Output swings rail-to-rail
- Output sources and sinks ±29mA load current
- 0.2% gain error
- Pb-free plus anneal available (RoHS compliant)

Applications

- Battery- or solar-powered systems
- Strain gauges
- Current monitors
- Thermocouple amplifiers

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL8170IS	8170IS	-	8 Ld SO	MDP0027
EL8170IS-T7	8170IS	7”	8 Ld SO	MDP0027
EL8170IS-T13	8170IS	13”	8 Ld SO	MDP0027
EL8170ISZ (See Note)	8170ISZ	-	8 Ld SO (Pb-free)	MDP0027
EL8170ISZ-T7 (See Note)	8170ISZ	7”	8 Ld SO (Pb-free)	MDP0027
EL8170ISZ-T13 (See Note)	8170ISZ	13”	8 Ld SO (Pb-free)	MDP0027

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL8173IS	8173IS	-	8 Ld SO	MDP0027
EL8173IS-T7	8173IS	7”	8 Ld SO	MDP0027
EL8173IS-T13	8173IS	13”	8 Ld SO	MDP0027
EL8173ISZ (See Note)	8173ISZ	-	8 Ld SO (Pb-free)	MDP0027
EL8173ISZ-T7 (See Note)	8173ISZ	7”	8 Ld SO (Pb-free)	MDP0027
EL8173ISZ-T13 (See Note)	8173ISZ	13”	8 Ld SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Description

EL8170/EL8173	PIN NAME	PIN FUNCTION
1	$\overline{\text{ENABLE}}$	Active Low. When pulled up above 2V, the in-amp conserves 3µA disabled supply current and the output is in a high impedance state. An internal pull down defines the $\overline{\text{ENABLE}}$ low when left floating.
2	IN-	Inverting (IN-) and non-inverting (IN+) high impedance input terminals.
3	IN+	
4	VS-	Negative supply terminal.
5	FB-	High impedance feedback terminals. The feedback terminals have a very similar equivalent circuit as the input terminals. They also have an Input Bias Compensation/Cancelling Circuit. The negative feedback (FB-) pin connects to an external resistive network to set the gain of the in-amp. The positive feedback (FB+) can be used to shift the DC level of the output or as an output offset.
8	FB+	
7	VS+	Positive supply terminal.
6	VOUT	Output Voltage.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage, V_S 5.5V
Differential Input Current 5mA
Differential Input Voltage 0.5V
V_{EN} . . . . . - 0.5V, V_S+ + 0.5V
ESD 3kV
Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature . . . . . .-40°C to +85°C
Storage Temperature . . . . . .-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = GND, VCM = 1/2V_S+, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	EL8170			100	250	µV
		EL8173			400	1000	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	Temperature = -40°C to 85°C			2		µV/°C
I_{OS}	Input Offset Current between IN+, and IN- and between FB+ and FB-				0.5	2	nA
I_B	Input Bias Current (IN+, IN-, FB+, and FB- terminals)				0.5	2	nA
e_N	Input Noise Voltage	EL8170	f = 0.1Hz to 10Hz		2		$µV_{P-P}$
		EL8173			10		$µV_{P-P}$
	Input Noise Voltage Density	EL8170	f_o = 1kHz		50		nV/√Hz
		EL8173			200		nV/√Hz
i_N	Input Noise Current Density	f_o = 1kHz			0.1		pA/√Hz
R_{IN}	Input Resistance	EL8170			8		MΩ
		EL8173			14		MΩ
V_{IN}	Input Voltage Range	Guaranteed by CMRR test		0		5	V
CMRR	Common Mode Rejection Ratio	EL8170	V_{CM} = 0V to +5V	80	108		dB
		EL8173		80	104		dB
PSRR	Power Supply Rejection Ratio	EL8170	V_S = 2.9V to 5V	80	104		dB
		EL8173		70	90		dB
E_G	Gain Error	EL8170	R_L = 100kΩ to 2.5V	-1.5	+0.3	+1.5	%
		EL8173		-0.8	+0.2	+0.8	%
V_{OUT}	Maximum Voltage Swing	Output low, 100kΩ to 2.5V		0	4	10	mV
		Output low, 1kΩ to 2.5V			0.13	0.25	V
		Output high, 100kΩ to 2.5V		4.990	4.996		V
		Output high, 1kΩ to GND		4.75	4.88		V
SR	Slew Rate	R_L = 1kΩ to GND		0.3	0.5	0.7	V/µs

Electrical Specifications V_S+ = +5V, V_S- = GND, VCM = 1/2V_S+, T_A = 25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
-3dB BW	-3dB Bandwidth	EL8170	Gain = 100V/V		192		kHz
			Gain = 200		93		kHz
			Gain = 500		30		kHz
			Gain = 1000		13		kHz
		EL8173	Gain = 10		396		kHz
			Gain = 20		221		kHz
			Gain = 50		69		kHz
			Gain = 100		30		kHz
$I_{S,EN}$	Supply Current, Enabled			40	60	78	µA
$I_{S,DIS}$	Supply Current, Disabled	$\overline{EN}$ = V_S+		1.5	2.9	5	µA
V_{ENH}	$\overline{Enable}$ Pin for Shut-down			2			V
V_{ENL}	$\overline{Enable}$ Pin for Power-on					0.8	V
V_S	Minimum Supply Voltage				2.2	2.4	V
I_O	Output Current into 10Ω to V_S/2	V_S = 5V		±18	±29		mA
		V_S = 2.9V		±4	±7.5		mA

Typical Performance Curves

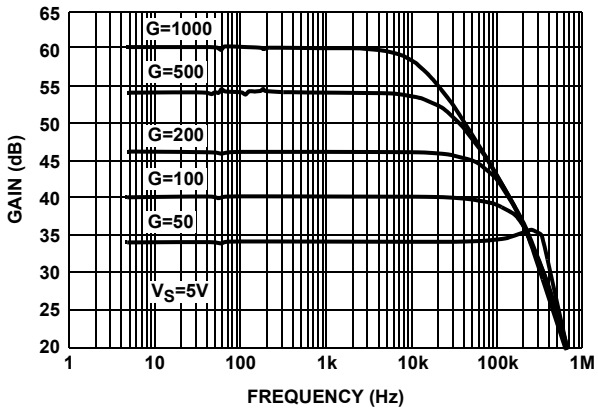


FIGURE 1. EL8170 FREQUENCY RESPONSE vs CLOSED LOOP GAIN

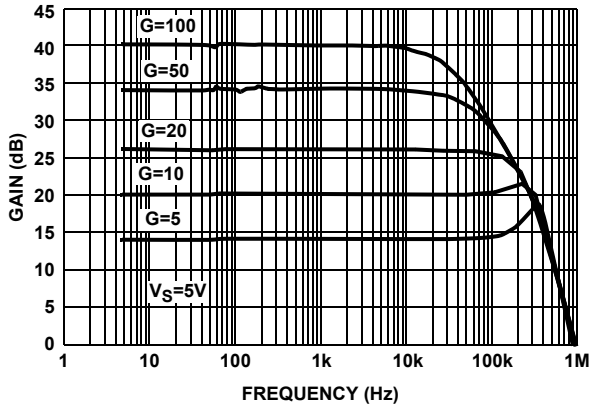


FIGURE 2. EL8173 FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves (Continued)

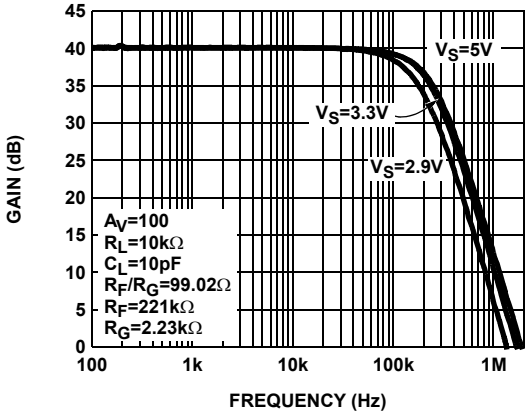


FIGURE 3. EL8170 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

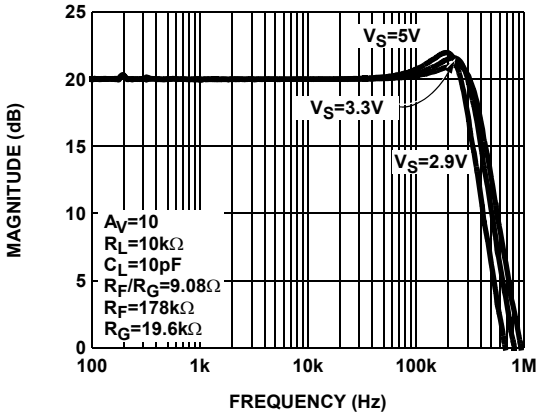


FIGURE 4. EL8173 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

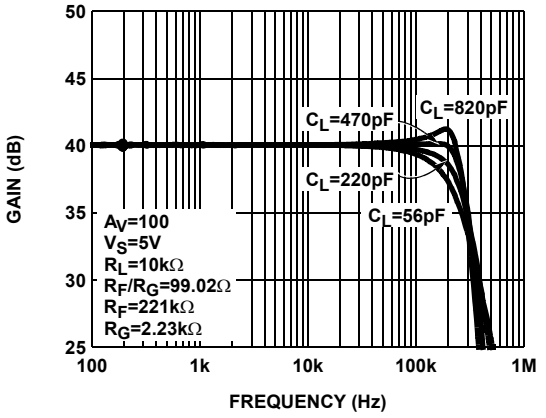


FIGURE 5. EL8170 FREQUENCY RESPONSE vs C_{LOAD}

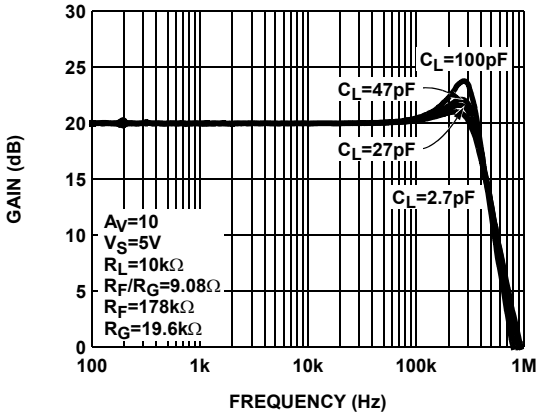


FIGURE 6. EL8173 FREQUENCY RESPONSE vs C_{LOAD}

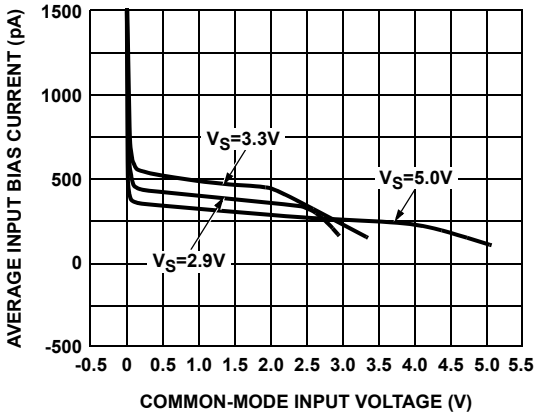


FIGURE 7. EL8170 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ 25°C

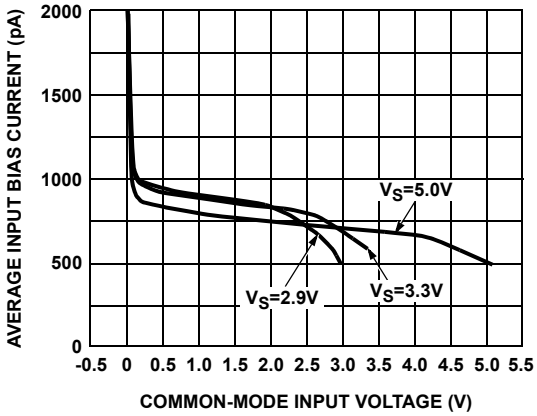


FIGURE 8. EL8173 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ 25°C

Typical Performance Curves (Continued)

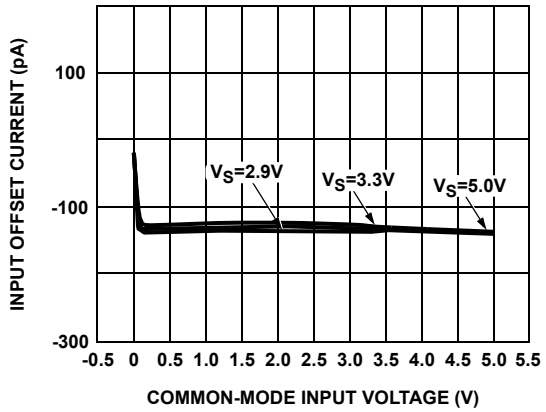


FIGURE 9. EL8170 INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE @ 25°C

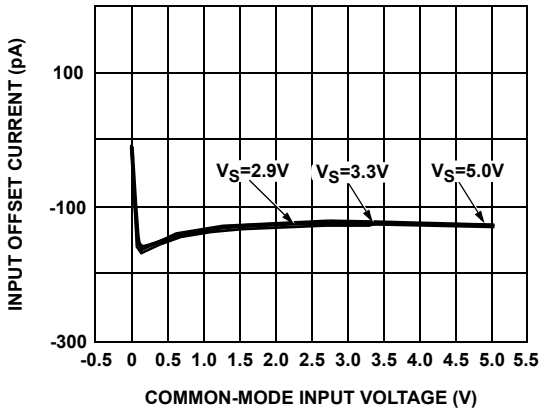


FIGURE 10. EL8173 INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE @ 25°C

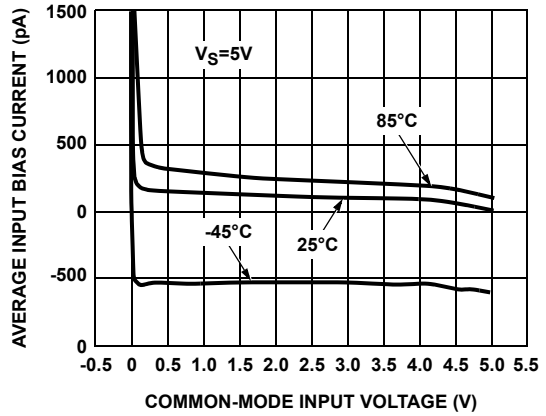


FIGURE 11. EL8170 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ V_S = 5V, TEMPERATURE = -45°C, 25°C, AND 85°C

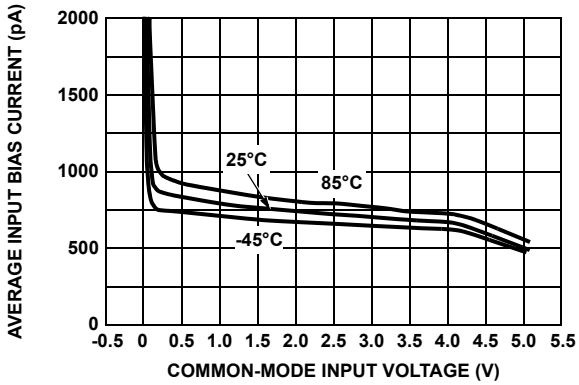


FIGURE 12. EL8173 AVERAGE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE @ V_S = 5V, TEMPERATURE = -45°C, 25°C, AND 85°C

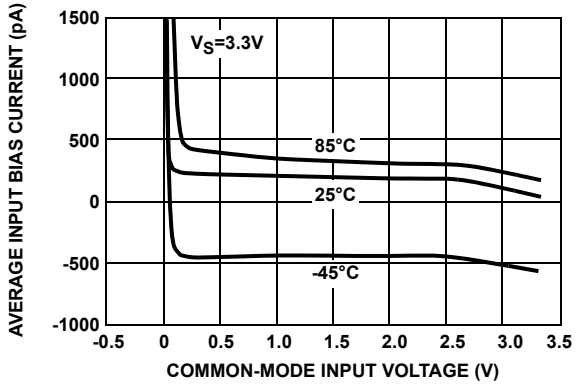


FIGURE 13. EL8170 AVERAGE INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE @ V_S = 3.3V, TEMPERATURE = -45°C, 25°C, AND 85°C

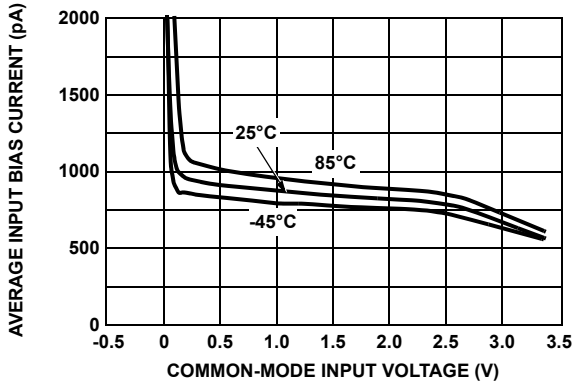


FIGURE 14. EL8173 AVERAGE INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE @ V_S = 3.3V, TEMPERATURE = -45°C, 25°C, AND 85°C

Typical Performance Curves (Continued)

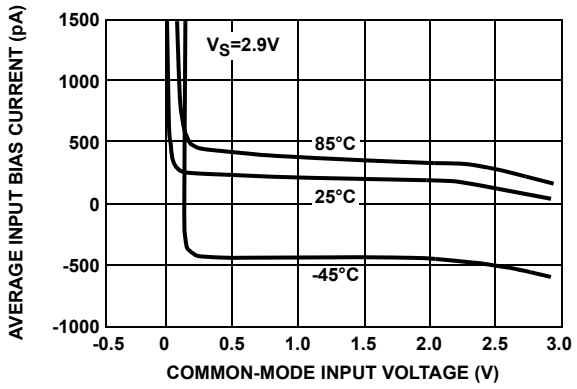


FIGURE 15. EL8170 AVERAGE INPUT BIAS CURRENTS vs COMMON-MODE INPUT VOLTAGE @ V_S = 2.9V, TEMPERATURE = -45°C, 25°C, AND 85°C

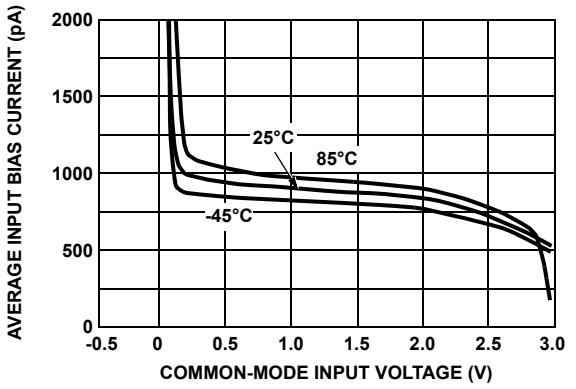


FIGURE 16. EL8173 AVERAGE INPUT BIAS CURRENTS vs COMMON-MODE INPUT VOLTAGE @ V_S = 2.9V, TEMPERATURE = -45°C, 25°C, AND 85°C

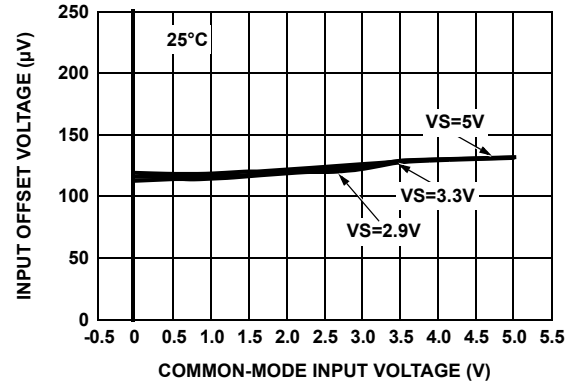


FIGURE 17. EL8170 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 5V, 3.3V AND 2.9V AND TEMPERATURE = 25°C

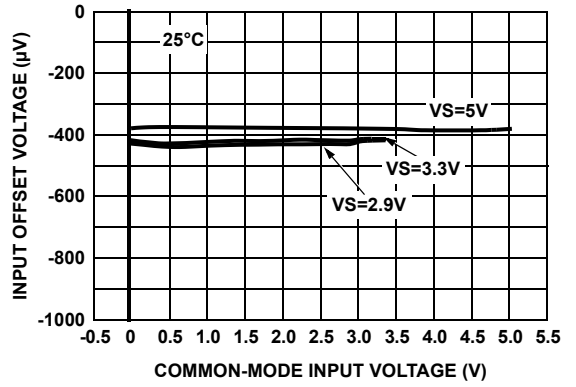


FIGURE 18. EL8173 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 5V, 3.3V, AND 2.9V AND TEMPERATURE = 25°C

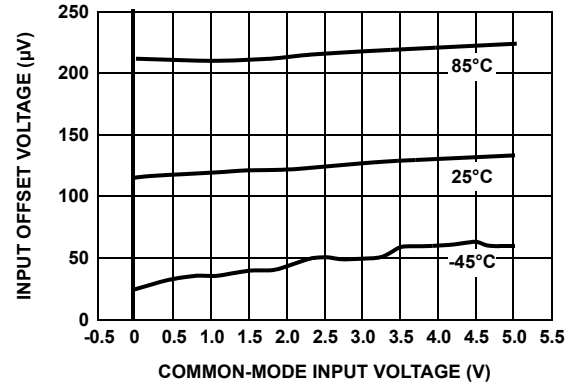


FIGURE 19. EL8170 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 5.0V, TEMPERATURE = -45°C, 25°C, AND 85°C

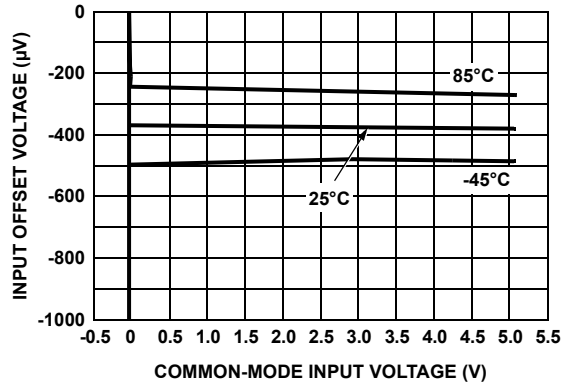


FIGURE 20. EL8173 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 5.0V, TEMPERATURE = -45°C, 25°C, AND 85°C

Typical Performance Curves (Continued)

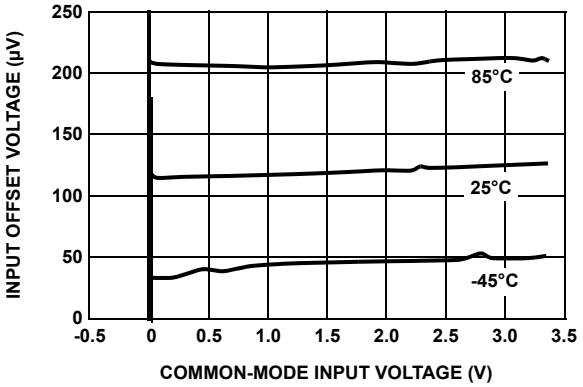


FIGURE 21. EL8170 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 3.3V, TEMPERATURE = -45°C, 25°C, AND 85°C

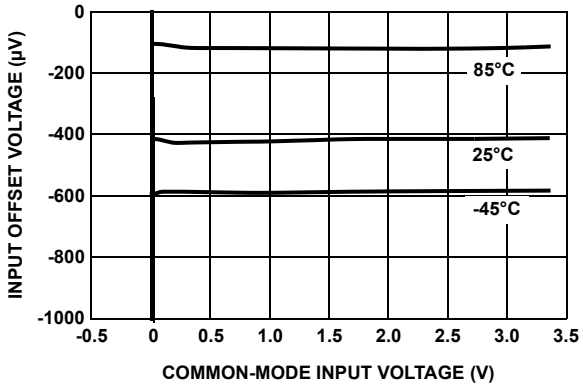


FIGURE 22. EL8173 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 3.3V, TEMPERATURE = -45°C, 25°C, AND 85°C

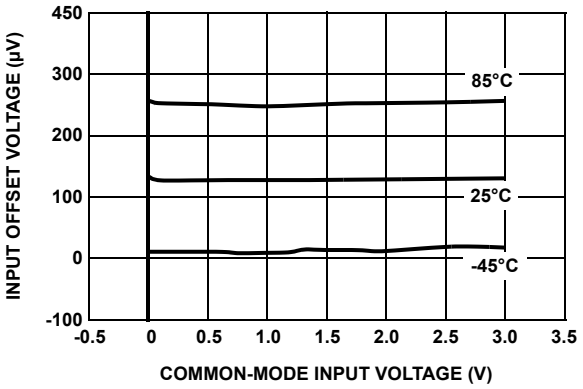


FIGURE 23. EL8170 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 2.9V, TEMPERATURE = -45°C, 25°C, AND 85°C

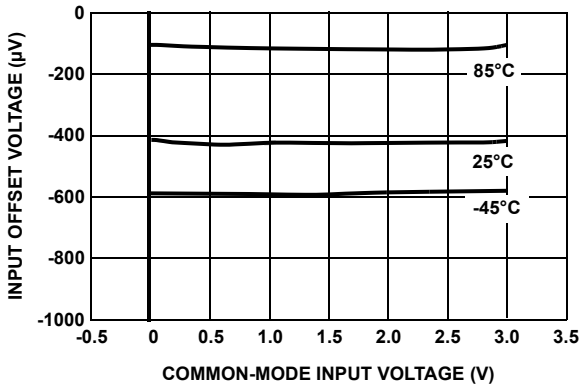


FIGURE 24. EL8173 INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE @ V_S = 3.3V, TEMPERATURE = - 45°C, 25°C, AND 85°C

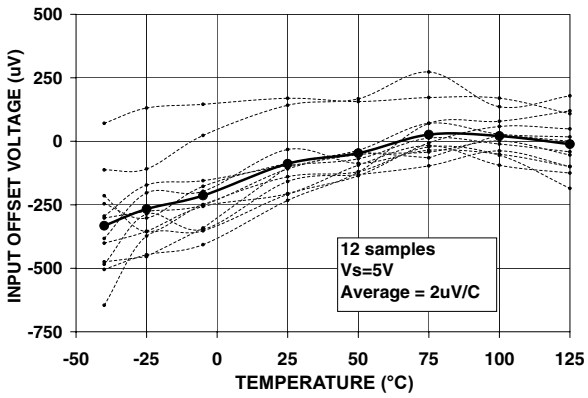


FIGURE 25. EL8170 INPUT OFFSET VOLTAGE vs TEMPERATURE @ V_S = 5.0V

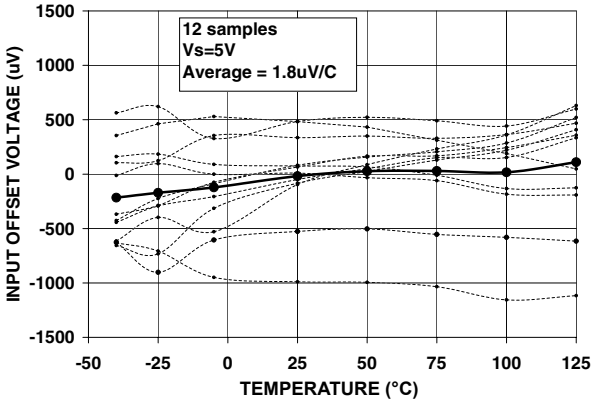


FIGURE 26. EL8173 INPUT OFFSET VOLTAGE vs TEMPERATURE @ V_S = 5.0V

Typical Performance Curves (Continued)

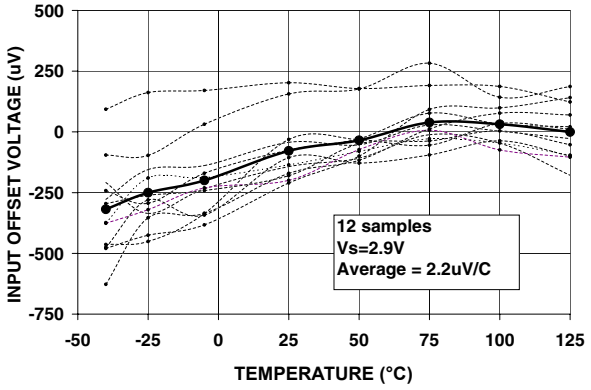


FIGURE 27. EL8170 INPUT OFFSET VOLTAGE vs TEMPERATURE @ V_S = 2.9V

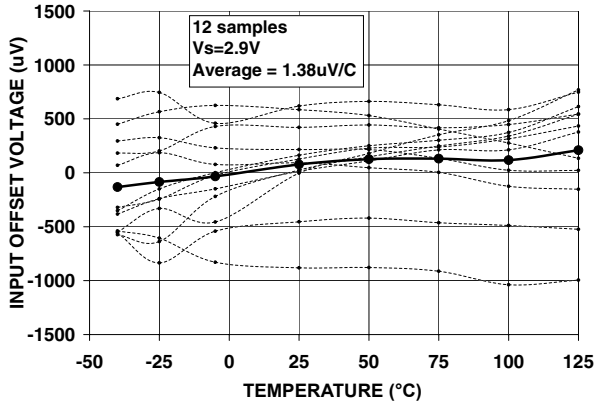


FIGURE 28. EL8173 INPUT OFFSET VOLTAGE vs TEMPERATURE @ V_S = 2.9V

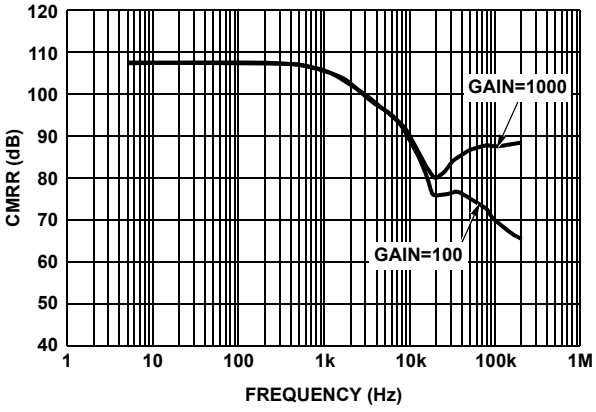


FIGURE 29. EL8170 CMRR vs FREQUENCY

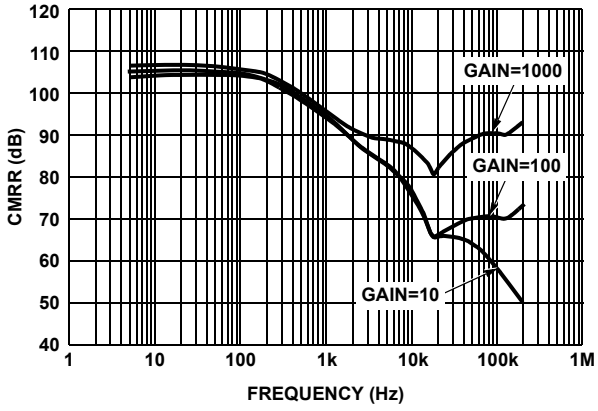


FIGURE 30. EL8173 CMRR vs FREQUENCY

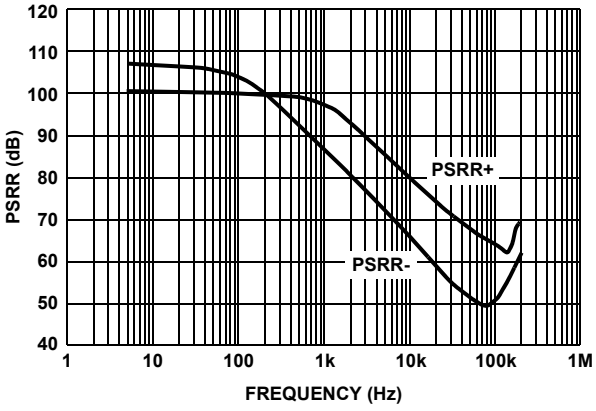


FIGURE 31. EL8170 PSRR vs FREQUENCY

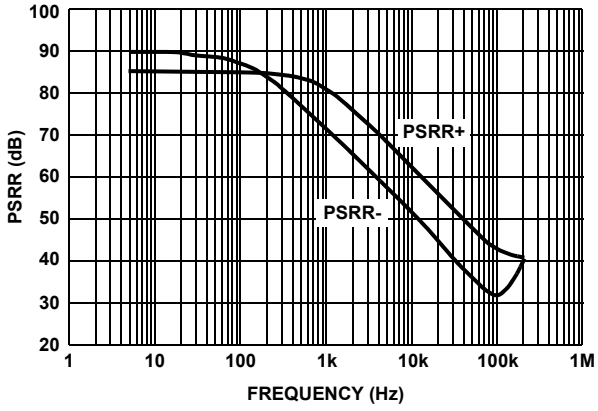


FIGURE 32. EL8173 PSRR vs FREQUENCY

Typical Performance Curves (Continued)

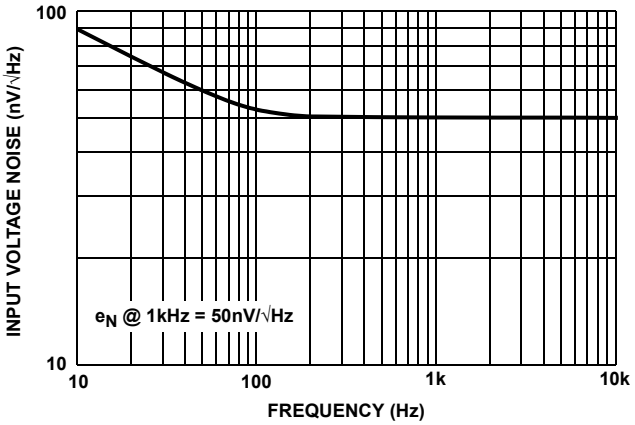


FIGURE 33. EL8170 VOLTAGE NOISE DENSITY

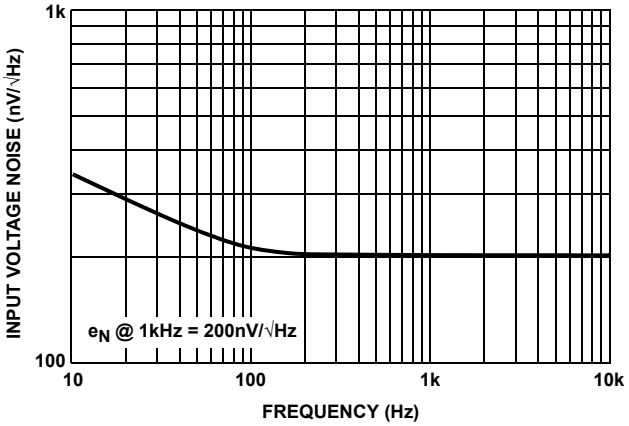


FIGURE 34. EL8173 VOLTAGE NOISE DENSITY

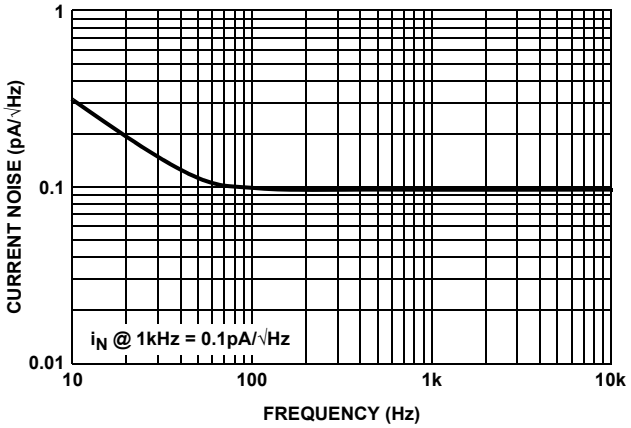


FIGURE 35. EL8170 AND EL8173 CURRENT NOISE DENSITY

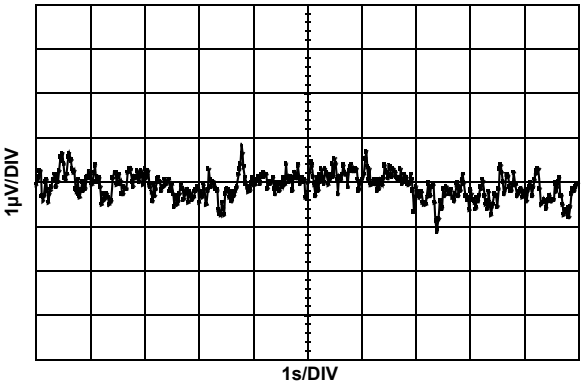


FIGURE 36. EL8170 0.1Hz TO 10Hz INPUT VOLTAGE NOISE (GAIN = 100)

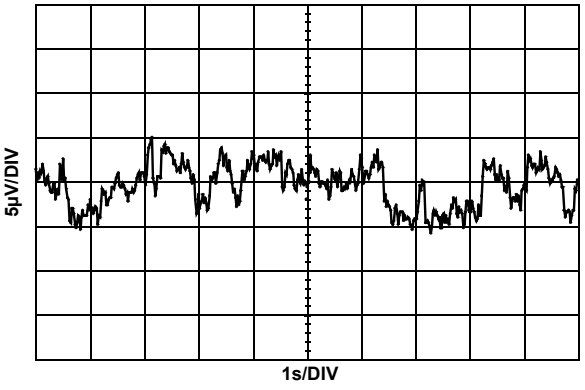


FIGURE 37. EL8173 0.1Hz TO 10Hz INPUT VOLTAGE NOISE (GAIN = 10)

Typical Performance Curves (Continued)

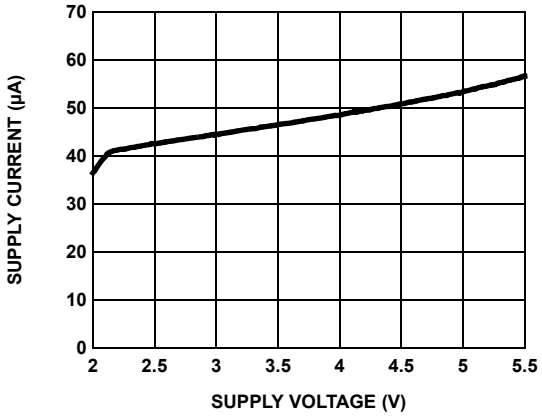


FIGURE 38. EL8170 AND EL8173 SUPPLY CURRENT vs SUPPLY VOLTAGE

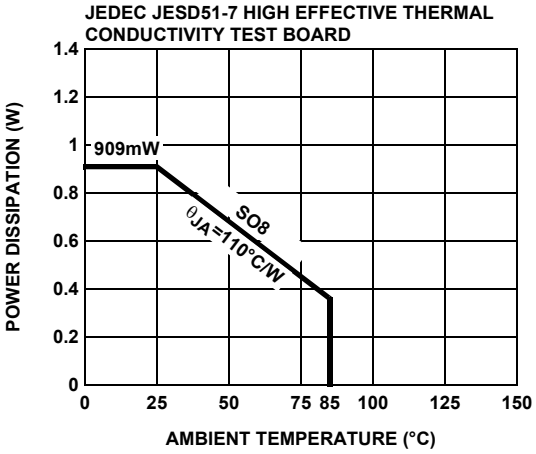


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

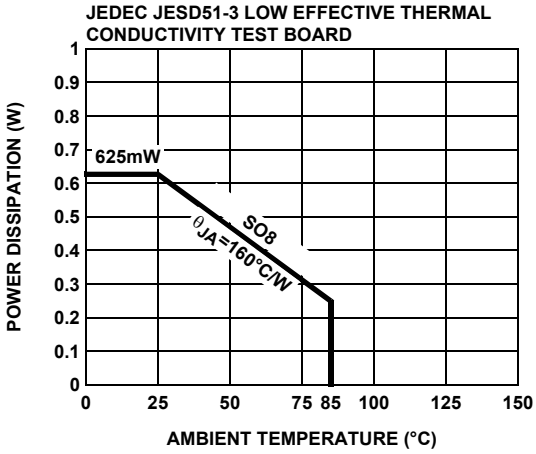


FIGURE 40. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Description of Operation and Applications Information

Product Description

The EL8170 and EL8173 are micropower instrumentation amplifiers (in-amps) which deliver rail-to-rail input amplification and rail-to-rail output swing on a single 2.9V to 5V supply. The EL8170 and EL8173 also deliver excellent DC and AC specifications while consuming only 60µA typical supply current. Because the EL8170 and EL8173 provide an independent pair of feedback terminals to set the gain and to adjust output level, these in-amps achieve high common-mode rejection ratio regardless of the tolerance of the gain setting resistors. The EL8173 is internally compensated for a minimum closed loop gain of 10 or greater, well suited for moderate to high gains. For higher gains, the EL8170 is internally compensated for a minimum gain of 100. An $\overline{\text{ENABLE}}$ pin is used to reduce power consumption, typically 2.9µA, while the instrumentation amplifier is disabled.

Input Protection

All input and feedback terminals of the EL8170 and EL8173 have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode drop beyond the supply rails. The EL8170 has additional back-to-back diodes across the input terminals and also across the feedback terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. On the other hand, the EL8173 has no clamps to limit the differential voltage on the input terminals allowing

higher differential input voltages at lower gain applications. It is recommended however, that the input terminals of the EL8173 is not overdriven beyond 1V to avoid offset drift. An external series resistor may be used as an external protection to limit excessive external voltage and current from damaging the inputs.

Input Stage and Input Voltage Range

The input terminals (IN+ and IN-) of the EL8170 and EL8173 are single differential pair bipolar PNP devices aided by an Input Range Enhancement Circuit to increase the headroom of operation of the common-mode input voltage. The feedback terminals (FB+ and FB-) also have a similar topology. As a result, the input common-mode voltage range of both the EL8170 and EL8173 is rail-to-rail. These in-amps are able to handle input voltages that are at or slightly beyond the supply and ground making these in-amps well suited for single 5V or 3.3V low voltage supply systems. There is no need then to move the common-mode input of the in-amps to achieve symmetrical input voltage.

Input Bias Cancellation/Compensation

Inside the EL8170 and EL8173 is an Input Bias Cancellation/Compensation Circuit for both the input and feedback terminals (IN+, IN-, FB+ and FB-), achieving a low input bias current all throughout the input common-mode range and the operating temperature range. While the PNP bipolar input stages are biased with an adequate amount of biasing current for speed and increased noise performance, the Input Bias Cancellation/Compensation Circuit sinks most of the base current of the input transistor leaving a small portion as input bias current, typically 500pA. In addition, the Input Bias Cancellation/Compensation Circuit maintains a smooth and flat behavior of input bias current over the common mode range and over the operating temperature range. The Input Bias Cancellation/Compensation Circuit operates from input voltages of 10mV above the negative supply to input voltages slightly above the positive supply. See Average Input Bias Current vs Common-Mode Input Voltage in the performance curves section.

Output Stage and Output Voltage Range

A pair of complementary MOSFET devices drives the output VOUT to within a few millivolts of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply, while the NMOS sinks current and pulls the output down to 4mV above the negative supply, or ground in the case of a single supply operation. The current sinking and sourcing capability of the EL8170 and EL8173 are internally limited to 29mA.

Gain Setting

VIN, the potential difference across IN+ and IN-, is replicated (less the input offset voltage) across FB+ and FB-. The obsession of the EL8170 and EL8173 in-amp is to maintain the differential voltage across FB+ and FB- equal to IN+ and IN-; (FB+ - FB-) = (IN+ - IN-). Consequently, the transfer function can be derived. The gain of the EL8170 and EL8173 is set by two external resistors, the feedback resistor RF, and the gain resistor RG.

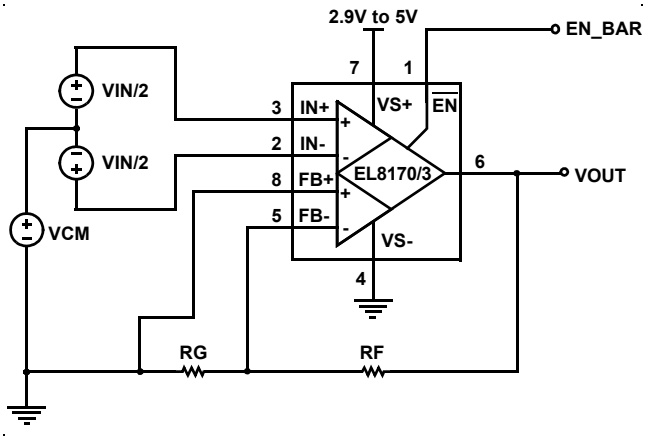


FIGURE 41. GAIN IS SET BY TWO EXTERNAL RESISTORS, R_F AND R_G

$$VOUT = \left(1 + \frac{R_F}{R_G}\right) VIN$$

In Figure 41, the FB+ pin and one end of resistor RG are connected to GND. With this configuration, the above gain equation is only true for a positive swing in VIN; negative input swings will be ignored and the output will be at ground.

Reference Connection

Unlike a three-op amp instrumentation amplifier, a finite series resistance seen at the REF terminal does not degrade the EL8170 and EL8173's high CMRR performance eliminating the need for an additional external buffer amplifier. Figure 42 uses the FB+ pin to provide a high impedance REF terminal.

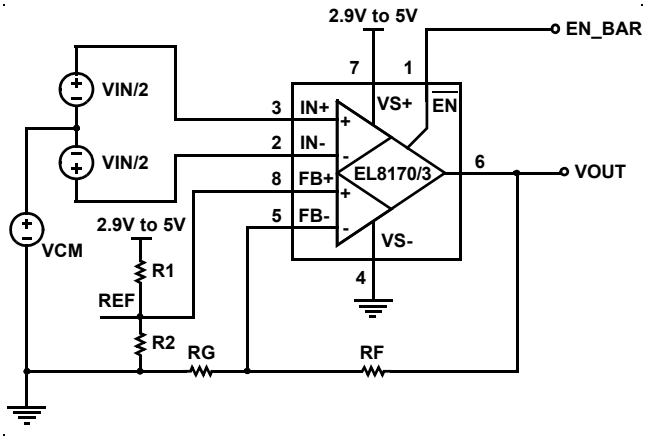


FIGURE 42. GAIN SETTING AND REFERENCE CONNECTION

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + \left(1 + \frac{R_F}{R_G}\right)(VREF)$$

The FB+ pin is used as a REF terminal to center or to adjust the output. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal without degrading or affecting the CMRR performance. Any voltage applied to the REF terminal will shift VOUT by VREF times the closed loop gain, which is set by resistors RF and RG. See Figure 42.

The FB+ pin can also be connected to the other end of resistor, RG. See Figure 43. Keeping the basic concept that the EL8170 and EL8173 in-amps maintain constant differential voltage across the input terminals and feedback terminals (IN+ - IN- = FB+ - FB-), the transfer function of Figure 43 can be derived.

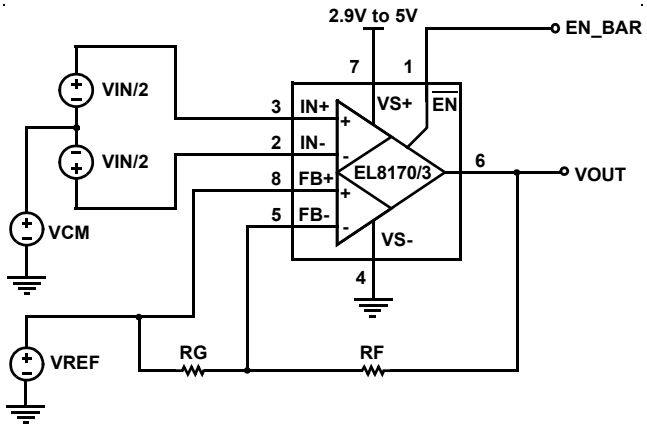


FIGURE 43. REFERENCE CONNECTIONWITH AN AVAILABLE VREF

$$VOUT = \left(1 + \frac{R_F}{R_G}\right)(VIN) + (VREF)$$

A finite resistance RS in series with the VREF source, adds an output offset of VIN*(RS/RG). As the series resistance Rs approaches zero, the gain equation is simplified to the above equation for Figure 43. VOUT is simply shifted by an amount VREF.

External Resistor Mismatches

Because of the independent pair of feedback terminals provided by the EL8170 and EL8173, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three op amp and especially a two op amp in-amp, the EL8170 and EL8173 reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The EL8170 and EL8173 CMRR will be 108dB regardless of the tolerance of the resistors used.

Gain Error and Accuracy

The EL8173 has a Gain Error, EG, of 0.2% typical. The EL8170 has an EG of 0.3% typical. The gain error indicated in the electrical specifications table is the inherent gain error of the EL8170 and EL8173 and does not include the gain error contributed by the resistors. There is an additional gain error due to the tolerance of the resistors used. The resulting non-ideal transfer function effectively becomes:

$$VOUT = \left(1 + \frac{R_F}{R_G}\right) \times [1 - (E_{RG} + E_{RF} + E_G)] \times VIN$$

Where:

ERG = Tolerance of RG

ERF = Tolerance of RF

EG = Gain Error of the EL8170 or EL8173

The term [1 - (ERG +ERF +EG)] is the deviation from the theoretical gain. Thus, (ERG +ERF +EG) is the total gain error. For example, if 1% resistors are used for the EL8170, the total gain error would be:

$$= \pm(E_{RG} + E_{RF} + E_G(\text{typical}))$$

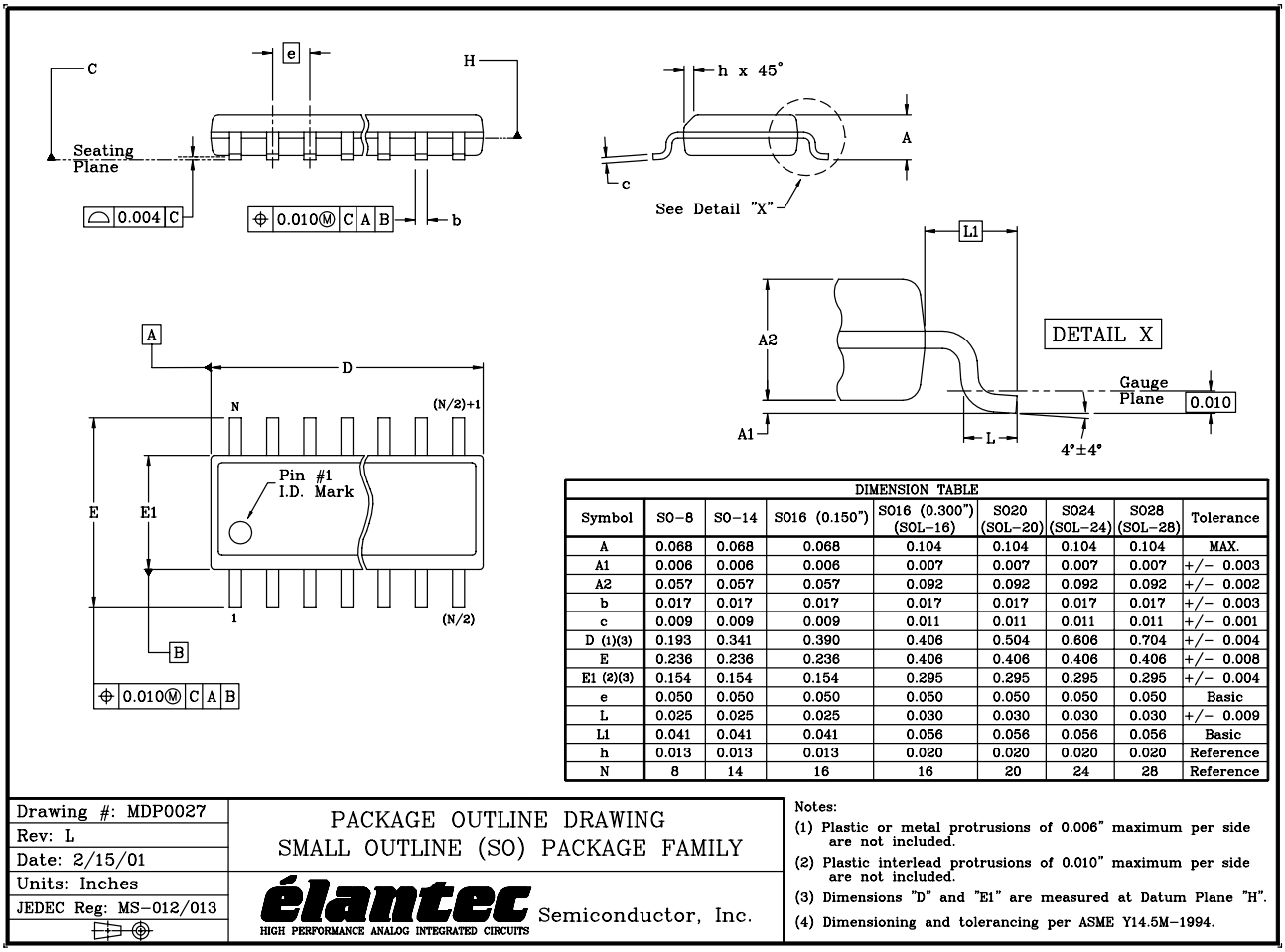
$$= \pm(0.01 + 0.01 + 0.003)$$

$$= \pm 2.3\%$$

Disable/Power-Down

The EL8170 and EL8173 can be powered down reducing the supply current to typically 2.9µA. When disabled, the output is in a high impedance state. The active low $\overline{\text{ENABLE}}$ bar pin has an internal pull down and hence can be left floating and the in-amp enabled by default. When the $\overline{\text{ENABLE}}$ bar is connected to an external logic, the in-amp will power down when $\overline{\text{ENABLE}}$ bar is pulled above 2V, and will power on when $\overline{\text{ENABLE}}$ bar is pulled below 0.8V.

Package Outline Drawing



DIMENSION TABLE								
Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MS-012/013	

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp