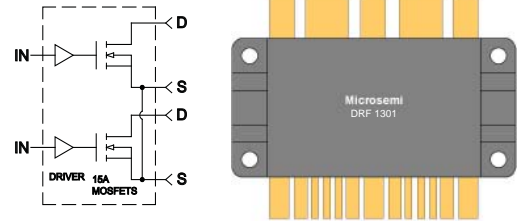


## MOSFET Push-Pull Hybrid

The DRF1301 is a push-pull hybrid containing two high power gate drivers and two power MOSFETs. It was designed to provide the system designer increased flexibility, higher performance, and lowered cost over a non-integrated solution. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground, Anti-Ring function Invert and Non-invert select pin provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency ISM applications.



### FEATURES

- Switching Frequency: DC TO 30MHz
- Inverting Non-Inverting Select
- Low Pulse Width Distortion
- Single Power Supply (Per Section)
- 1V CMOS Schmitt Trigger Input 1V Hysteresis
- Switching Speed 3-4ns
- $B_{V_{ds}} = 1000V$
- $I_{ds} = 15A$  max. Per-section
- $R_{ds(on)} \leq 1 \text{ Ohm}$
- $P_D = 550W$  Per-section
- RoHS Compliant

### TYPICAL APPLICATIONS

- Class C, D and E RF Generators
- Switch Mode Power Amplifiers
- HV Pulse Generators
- Ultrasound Transducer Drivers
- Acoustic Optical Modulators

### Driver Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
$V_{DD}$	Supply Voltage	15	V
IN, FN	Input Single Voltages	-.7 to +5.5	
$I_{O\text{PK}}$	Output Current Peak	8	A
$T_{JMAX}$	Operating Temperature	175	°C

### Driver Specifications

Symbol	Parameter	Min	Typ	Max	Unit
$V_{DD}$	Supply Voltage	10		15	V
IN	Input Voltage	3	5		
$IN_{(R)}$	Input Voltage Rising Edge		3		ns
$IN_{(F)}$	Input Voltage Falling Edge		3		
$I_{DDQ}$	Quiescent Current		2		mA
$I_O$	Output Current		8		A
$C_{iss}$	Input Capacitance		3		
$R_{IN}$	Input Parallel Resistance		1		MΩ
$V_{T(ON)}$	Input, Low to High Out (See Truth Table)	0.8		1.1	V
$V_{T(OFF)}$	Input, High to Low Out (See Truth Table)	1.9		2.2	
$T_{DLY}$	Time Delay (throughput)		38		ns
$t_r$	Rise Time		5		ns
$t_f$	Fall Time		5		

## Driver Output Characteristics

DRF1301

Symbol	Parameter	Min	Typ	Max	Unit
$C_{out}$	Output Capacitance		2500		pF
$R_{out}$	Output Resistance		.8		$\Omega$
$L_{out}$	Output Inductance		3		nH
$F_{MAX}$	Operating Frequency CL = 3000nF + 50 $\Omega$	30			MHz
$F_{MAX}$	Operating Frequency RL = 50 $\Omega$	50			

## Driver Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.5		$^{\circ}\text{C}/\text{W}$
$R_{\theta JHS}$	Thermal Resistance Junction to Heat Sink		2.5		
$T_{JSTG}$	Storage Temperature		-55 to 150		$^{\circ}\text{C}$
$P_{DJHS}$	Maximum Power Dissipation @ $T_{SINK} = 25^{\circ}\text{C}$		60		W
$P_{DJC}$	Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$		100		

## MOSFET Absolutes Maximum Ratings (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
$BV_{DSS}$	Drain Source Voltage	1000			V
$I_D$	Continuous Drain Current $T_{HS} = 25^{\circ}\text{C}$			15	A
$R_{DS(on)}$	Drain-Source On State Resistance		1		$\Omega$
$T_{jmax}$	Operating Temperature			175	$^{\circ}\text{C}$

## MOSFET Dynamic Characteristics (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
$C_{ISS}$	Input Capacitance		1800		pF
$C_{OSS}$	Output Capacitance		335		
$C_{RSS}$	Reverse Transfer Capacitance		75		

## MOSFET Thermal Characteristics (Total Package)

Symbol	Parameter	Min	Type	Max	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance		.06		$^{\circ}\text{C}/\text{W}$
$R_{\theta JHS}$	Junction to Heat Sink Thermal Resistance		.14		
$T_{JSTG}$	Storage Junction Temperature		-55 to 150		$^{\circ}\text{C}$
$P_{DHS}$	Maximum Power Dissipation @ $T_{SINK} = 25^{\circ}\text{C}$		1.07		KW
$P_{DC}$	Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$		2.5		

## Section A and B Output Switching Performance

Symbol	Characteristic	Min	Typ	Max	Unit
$T_{ON}$	Leading Edge 10% to 90%	2	3	4	ns
$T_{OFF}$	Trailing Edge 10% to 90%	45	TBD	49	
$T_{DLY(ON)}$	Total Throughput Delay Time, ON	45	TBD	47	
$T_{DLY(OFF)}$	Total Throughput Delay Time, OFF	49	50	51	
$\Delta T_{DLY(ON)}$	Delta $T_{ON}$ Delay between Section A and B	-0.5	0	1.5	
$\Delta T_{DLY(OFF)}$	Delta $T_{OFF}$ Delay between Section A and B	0	0.6	1.3	

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

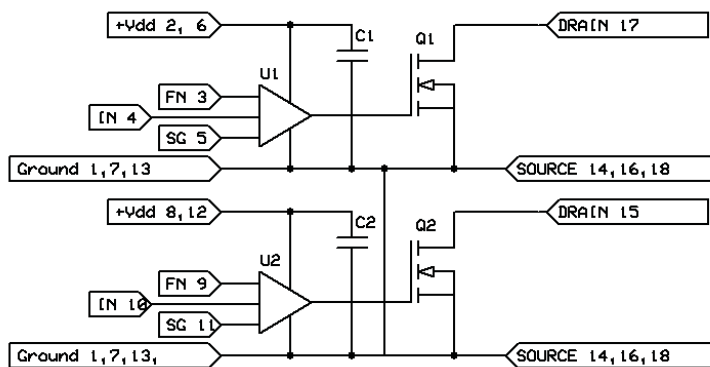


Figure 1, DRF1301 Circuit Diagram

The DRF1301 is configured as a Push Pull Hybrid incorporating two independent channels configured with a common source each consisting of a driver, a high voltage MOSFET and by-pass capacitors. The function of the by-pass capacitors C1 and C2 is to reduce the internal parasitic loop inductance. This coupled with the tight geometry of the hybrid allows optimal gate drive to the MOSFET. This low parasitic approach coupled with the Schmitt trigger input (IN), Kelvin signal ground (SG) and the Anti-Ring function; provide improved stability and control in Kilowatt to Multi-Kilowatt high frequency applications. The IN pin should be referenced to the Kelvin Ground (SG) and is applied to a Schmitt Trigger. The SG pin is a Kelvin return for the IN pin only. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. To further increase the utility of the device the driver die and the MOSFET die are adjacent die selected. This provides a very close match in the turn on and propagation delays.

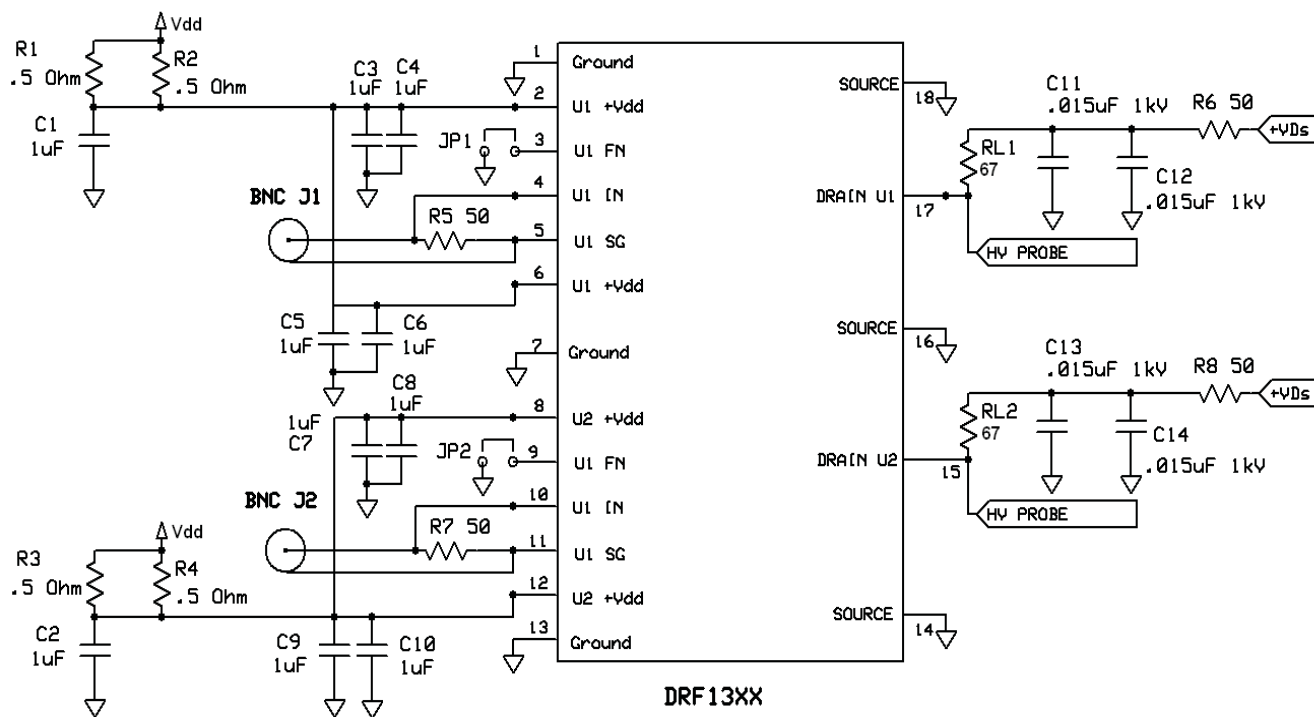


Figure 2, DRF1301 Test Circuit

The test circuit illustrated in Figure 2 was used to evaluate the DRF1301 (available as an evaluation board DRF13XX/EVALSW.) The input control signal is applied via IN and SG pins using RG188. This provides excellent noise immunity and control of the signal ground currents. The  $+V_{DD}$  inputs (pins 2, 6, 8 and 12) should be heavily by-passed by 1uF capacitors as close to the pins as possible. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load.  $R_L$  set for  $I_{DM}$  at  $V_{DS}$  max this load is used to evaluate the output performance.

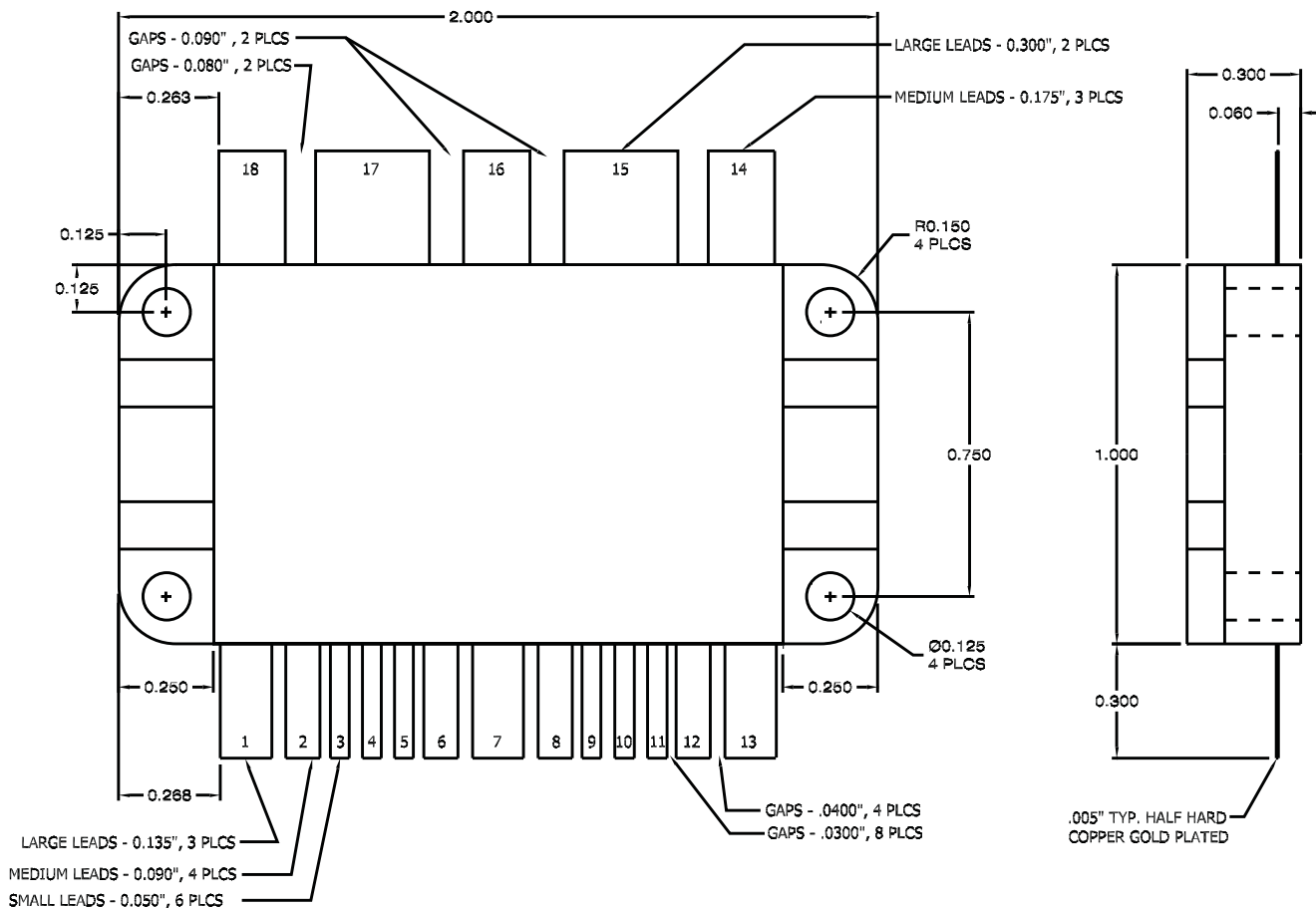
Pin Assignments	
Pin 1	Ground
Pin 2	U1 +Vdd
Pin 3	U1 FN
Pin 4	U1 IN
Pin 5	U1 SG
Pin 6	U1 +Vdd
Pin 7	Ground
Pin 8	U2 +Vdd
Pin 9	U2 FN
Pin 10	U2 IN
Pin 11	U2 SG
Pin 12	U2 +Vdd
Pin 13	Ground
Pin 14	Source
Pin 15	U2 Drain
Pin 16	Source
Pin 17	U1 Drain
Pin 18	Source

None of the inputs to U1 or U2 of the DRF1300 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to the application is the responsibility of the end user.** It is imperative that high output currents be restricted to the Source (14, 16, 18) and drain (15, 17) pins by design. See DRF100 for more information on Driver IC used in the device.

The Function (FN, pin 3 or pin 9) is the invert or non-invert select Pin, it is Internally held high.

Truth Table * Referenced to SG		
FN (pin 3)	IN (pin 4)	MOSFET U1
HIGH	HIGH	ON
HIGH	LOW	OFF
LOW	HIGH	OFF
LOW	LOW	ON

Truth Table * Referenced to SG		
FN (pin 9)	IN (pin 10)	MOSFET U2
HIGH	HIGH	ON
HIGH	LOW	OFF
LOW	HIGH	OFF
LOW	LOW	ON



All dimensions are ± .005

Figure 4, DRF1301 Mechanical Outline