



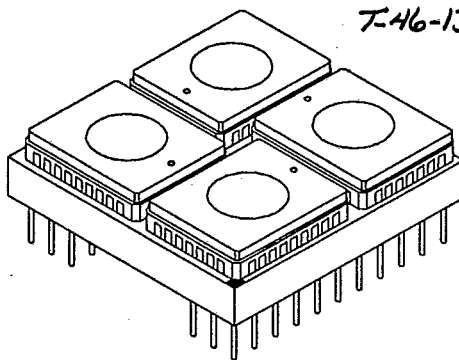
DPV12832V
128K X 32 UVEPROM VERSAPAC

T-46-13-29

DESCRIPTION:

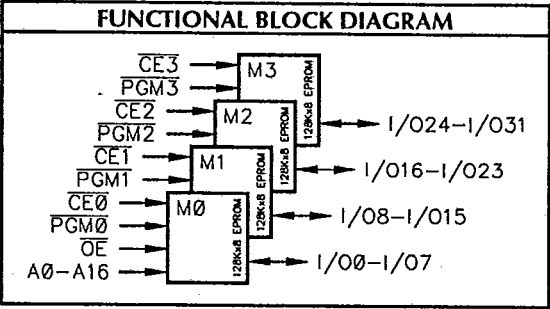
The DPV12832V is a 66-pin Pin Grid Array (PGA) consisting of four 128K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matching thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors (important for proper operation).



FEATURES:

- Organizations Available:
512K X 8, 265K X 16 or 128K X 32
- Access Times: -200, -250ns
- Fully Static Operation - No clock or refresh required
- Single Byte and Page Mode Programming
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (0.2ms Pulses Typ.)
- Common Data Inputs and Outputs
- Power Consumption:
440µW (Standby)
660mW (Active)
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data In/Out
CE0 - CE3	Chip Enables
PGM0 - PGM3	Program Enables
OE	Output Enable
VDD	Power (+5V)
Vss	Ground
Vpp	Programming Voltage
N.C.	No Connect

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PIN-OUT DIAGRAM

1 I/O8	12 PGM1	23 I/O15	34 I/O24	45 VDD	56 I/O31
2 I/O9	13 CET	24 I/O14	35 I/O25	46 CE3	57 I/O30
3 I/O10	14 VSS	25 I/O13	36 I/O26	47 PGM3	58 I/O29
4 A13	15 I/O11	26 I/O12	37 A6	48 I/O27	59 I/O28
5 A14	16 A10	27 OE	38 A7	49 A3	60 A0
6 A15	17 A11	28 N.C.	39 VPP	50 A4	61 A1
7 A16	18 A12	29 PGM0	40 A8	51 A5	62 A2
8 N.C.	19 VDD	30 I/O7	41 A9	52 PGM2	63 I/O23
9 I/O0	20 CE0	31 I/O6	42 I/O16	53 CE2	64 I/O22
10 I/O1	21 N.C.	32 I/O5	43 I/O17	54 VSS	65 I/O21
11 I/O2	22 I/O3	33 I/O4	44 I/O18	55 I/O19	66 I/O20

DPV12832V

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ABSOLUTE MAXIMUM RATINGS¹

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ²	-0.6 to +7.0	V
V _{I/O}	Input/Output Voltage ²	-0.6 to +7.0	V
V _{PP}	Programming Voltage ²	-0.6 to +13.0	V

RECOMMENDED OPERATING RANGE²

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage ⁴	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +1.0	V
V _{IL}	Input LOW Voltage	-0.3		0.8	V
V _{PP}	V _{PP} Supply Voltage ⁵	12.25	12.5	12.75	V

CAPACITANCE³: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	15	pF	V _{IN} = 0V
C _{ADR}	Address Input	50		
C _{OE}	Output Enable	50		
C _{I/O}	Data Input/Output	25		
C _{PGM}	Program	15		

AC TEST CONDITIONS: Including Programming

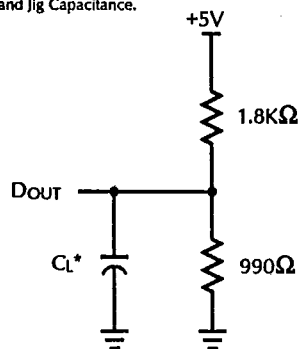
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

Output Load

Float	C _L	Parameters Measured
1	100 pF	except t _{DF} and t _{DFP}
2	5 pF	t _{DF} and t _{DFP}

Figure 1. Output Load

* Including Scope and Jig Capacitance.

DC OPERATING CHARACTERISTICS⁶: Over operating ranges

Symbol	Characteristics	Test Conditions	X8		X16		X32		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = V _{DD}	-8	8	-8	8	-8	8	μA
I _{OUT}	Output Leakage Current	CE = V _{IH} , V _{IN} = V _{DD} or V _{SS}	-8	8	-4	4	-2	2	μA
I _{CC1}	V _{DD} Active Current, Read	V _{IN} = V _{IH} or V _{IL} CE = V _{IL} , I _{OUT} = 0mA		25		50		100	mA
I _{CC2}	V _{DD} Operating Current, Read	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA Cycle = min. Duty = 100%		30		60		120	mA
I _{SB1}	V _{DD} Standby Current I _{OUT} = 0mA	CE = V _{IH} , V _{IN} = V _{IH} or V _{IL}		5		5		5	mA
I _{SB2}	V _{DD} Standby Current	CE = V _{DD} ± 0.3V V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		80		80		80	μA
I _{PP1}	V _{PP} Supply Current Byte Write	CE, PGM = V _{IL} , OE = V _{IH}		40		80		160	mA
I _{PP2}	V _{PP} Supply Current Page Write	CE, OE = V _{IH} , PGM = V _{IL} , V _{PP} = V _{DD}		50		100		200	mA
I _{PP3}	V _{PP} Supply Current Read	CE, OE = V _{IL} , PGM = V _{IH} , I _{OUT} > 0mA		80		80		80	μA
V _{OL}	Output LOW Voltage	I _{OUT} = 2.1mA		0.45		0.45		0.45	V
V _{OH1}	Output HIGH Voltage	I _{OUT} = -400μA	2.4		2.4		2.4		V
V _{IL}	Input LOW Level		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V _{IH}	Input HIGH Level		2.2	V _{DD} +1	2.2	V _{DD} +1	2.2	V _{DD} +1	V

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FUNCTIONS AND PIN CONNECTIONS

Mode	Function	PGM	CE	OE	V _{PP}	V _{DD}	I/O0 - I/O31	Power
Read Operations	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	X	X	H			High Impedance	
	Standby	X	H	X			High Impedance	
Program Operations (T _A = +25 ± 5°C)	Program	L	L	H	12.5V	6V	Data In	Standby
	Program Inhibit	H	H	X			High Impedance	
	Page Programming	L	H	H			High Impedance	
	Program Verify	H	L	L			Data Out	

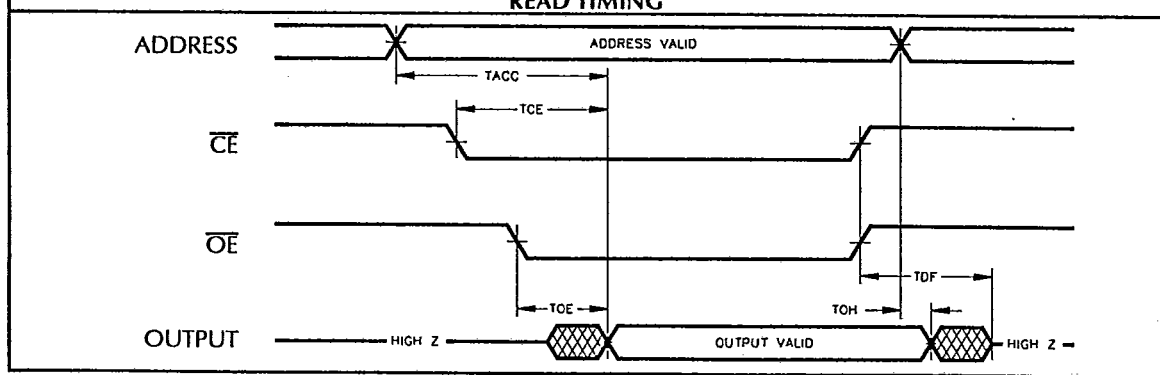
AC OPERATING CONDITIONS AND CHARACTERISTICS: Over operating ranges

No.	Symbol	Parameter	-200		-250		Unit
			Min.	Max.	Min.	Max.	
1	t _{ACC}	Address Access Time		200		250	ns
2	t _{CE}	Chip Enable to Output Valid ⁷		200		250	ns
3	t _{OE}	Output Enable to Output Valid ^{7, 8}		70		100	ns
4	t _{DF}	OE or CE HIGH to Output Float ^{3, 9}	0	50	0	60	ns
5	t _{OH}	Output Hold from Address	0		0		ns

AC PROGRAMMING CONDITIONS AND CHARACTERISTICS¹¹: Over operating ranges

No.	Symbol	Parameter	Min.	Max.	Unit
6	t _{AS}	Address Set-up Time	2		μs
7	t _{CEs}	Chip Enable Set-up Time	2		μs
8	t _{OE}	Output Enable Set-up Time	2		μs
9	t _{DS}	Data Set-up Time	2		μs
10	t _{VCS}	V _{DD} Set-up Time ¹⁰	2		μs
11	t _{VPS}	V _{PP} Set-up Time ¹⁰	2		μs
12	t _{AH}	Address Hold Time	0		μs
13	t _{OEh}	Output Enable Hold Time	2		μs
14	t _{DH}	Data Hold Time	2		μs
15	t _{CEP}	Chip Enable to Data Valid		150	ns
16	t _{DFP}	Output Enable HIGH Output Float Delay ³	0	130	ns
17	t _{PW}	Programming Pulse Width ¹⁰	0.19	0.21	ms
18	t _{OPW}	Over Programming Pulse Width ¹¹	0.19	5.25	ms
19	t _{AHL}	Address Latch Hold Time	2		μs
20	t _{LW}	Output Enable Pulse Width During Data Latch	1		μs
21	t _{PGMS}	Page Programming Setup Time	2		μs
22	t _{CEH}	Chip Enable Hold Time	2		μs

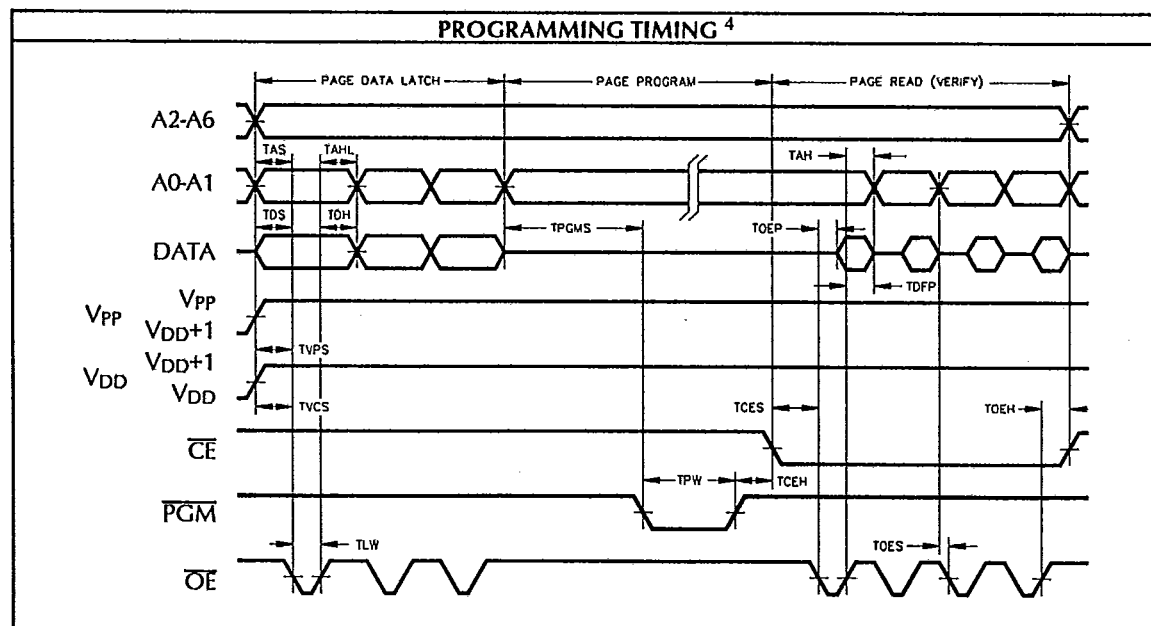
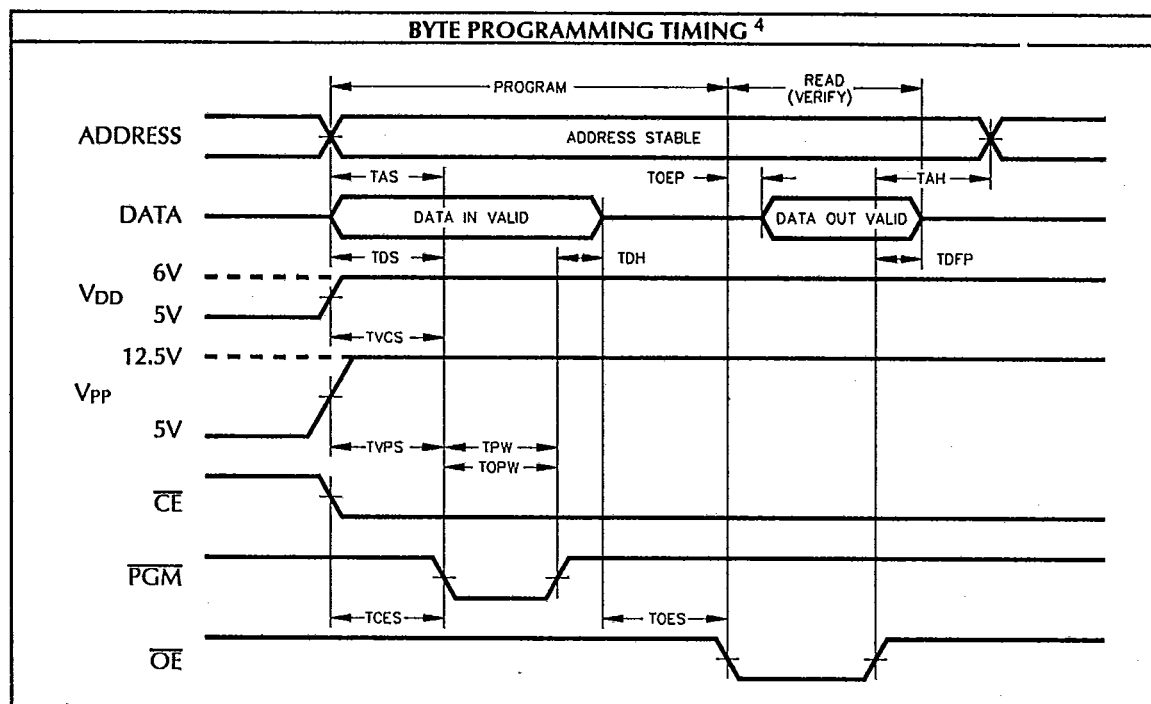
READ TIMING



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DPV12832V

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PROGRAMMING AND ERASING INFORMATION

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Programming

Upon delivery from Dense-Pac, or after erasure (See *Erasure section*), the DPV12832V contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV12832V through the procedure of programming. A 0.1 μ F capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.0V and +12.5V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the byte mode programming algorithm shown in Figure 2. In byte programming mode, $\overline{CE}$ is set at V_{IL} and $\overline{OE}$ is set at V_{IH} . After the applied address and input data signals are stable, programming is accomplished by a 0.2ms V_{IL} pulse on the $\overline{PGM}$ pin (refer to the *Byte Mode Programming Timing Diagram*).

The DPV12832V's fast page mode programming algorithm (shown in Figure 3) provides a great reduction in programming time by writing four bytes simultaneously. Each of these four bytes may contain different data. In page programming mode, $\overline{CE}$ and $\overline{PGM}$ are at V_{IH} while input data is strobed into internal holding registers by V_{IL} pulses on the $\overline{OE}$ pin. The

EPROM is then programmed by a 0.2ms V_{IL} pulse on the $\overline{PGM}$ pin while $\overline{CE}$ and $\overline{OE}$ are held at V_{IH} (refer to the *Page Programming Timing Diagram*).

System design consideration must be taken to avoid inadvertent page mode programming which can occur when $\overline{CE}$ and $\overline{OE}$ are at V_{IH} and $\overline{PGM}$ is at V_{IL} . A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

To clear all locations of their programmed contents it is necessary to expose the DPV12832V to an ultraviolet light source. A dosage of 15W-seconds/cm² is required to completely erase a DPV12832V. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å) with an intensity of 12,000 μ W/cm²] for 21 minutes.

The DPV12832V and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV12832V. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

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NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to V_{SS} .
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP} .
5. V_{PP} must not be greater than 13.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with $V_{PP} = 13.0V$. Also, during $\overline{CE} = V_{IL}$, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. $t_A = -55^\circ C$ to $+125^\circ C$, $V_{DD} = 5.0V \pm 0.5V$, and $V_{PP} = V_{DD}$ reading. $t_A = +25^\circ C \pm 5^\circ C$, $V_{DD} = 6.0V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$ programming.
7. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the following edge of $\overline{CE}$ without impact on t_{CE} .
8. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the following Address is valid without impact on t_{ACC} .
9. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
10. Initial Program Pulse Width Tolerance is $0.2ms \pm 5\%$.
11. The length of the overprogram pulse may vary from 0.19ms to 5.25ms as a function of the iteration counter value X.

```

graph TD
    START([START]) --> VDD[VDD=6.0V  
VPP=12.5V]
    VDD --> FIRST_ADDR[FIRST ADDRESS]
    FIRST_ADDR --> X0[X=0]
    X0 --> BYTE_MODE[BYTE MODE PROGRAM  
Tpw=0.2ms±5%]
    BYTE_MODE --> XINC[X = X + 1]
    XINC --> VERIFY_BYTE{VERIFY  
BYTE}
    VERIFY_BYTE -- PASS --> BYTE_MODE_2[BYTE MODE PROGRAM  
Tpw=0.2Xms]
    VERIFY_BYTE -- FAIL --> X25{X=25?}
    X25 -- YES --> FAIL1([FAIL])
    X25 -- NO --> BYTE_MODE
    BYTE_MODE_2 --> LAST_ADDR{LAST  
ADDRESS?}
    LAST_ADDR -- NO --> NEXT_ADDR[NEXT ADDRESS]
    NEXT_ADDR --> X0
    LAST_ADDR -- YES --> VDD_2[VDD=VPP=5.0V±10%]
    VDD_2 --> READ_ADDRESSES{READ ALL  
ADDRESSES}
    READ_ADDRESSES -- PASS --> END([END])
    READ_ADDRESSES -- FAIL --> FAIL1
  
```

X = COUNTER VALUE

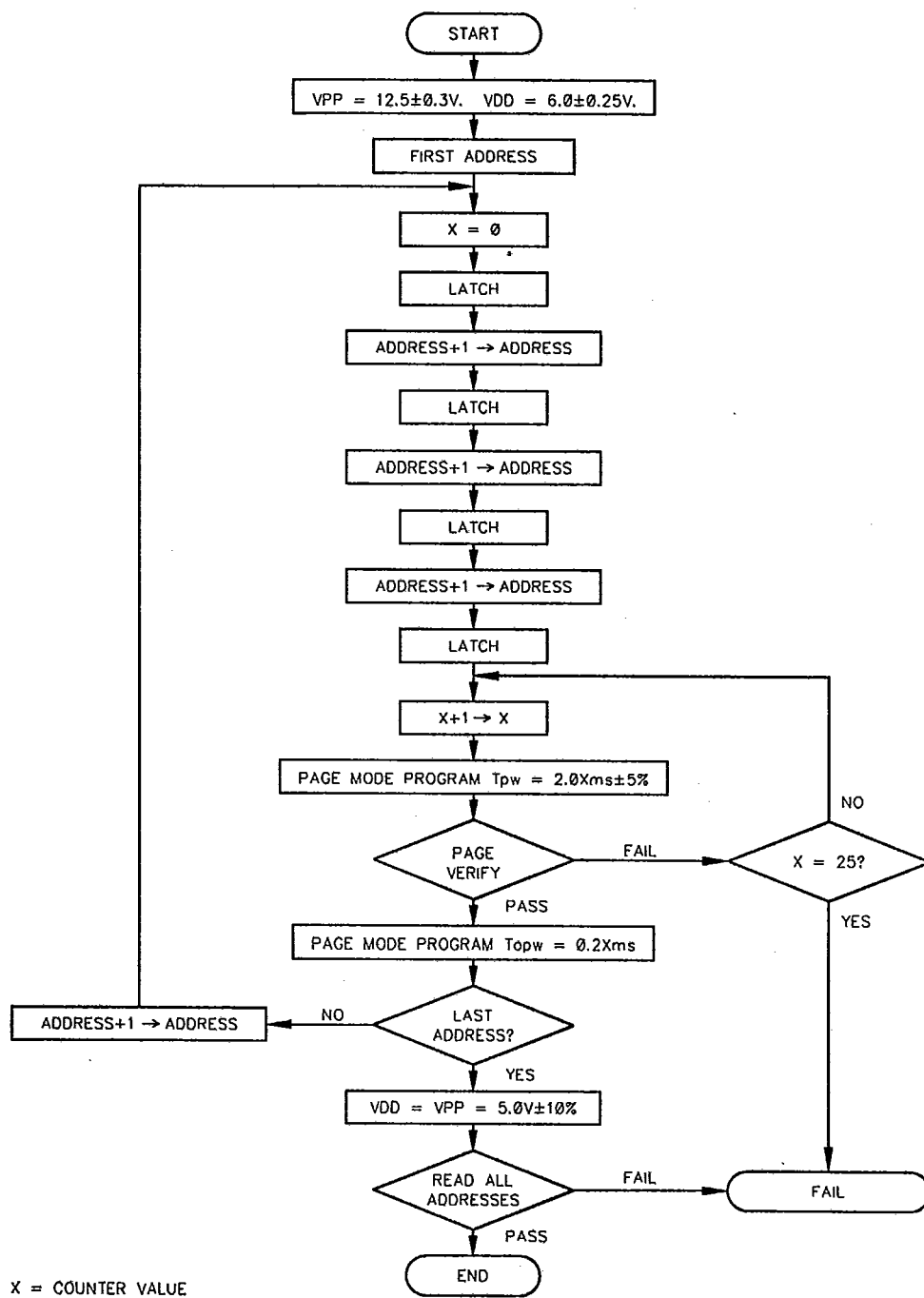
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Figure 3. High Performance Page Programming Flow Chart

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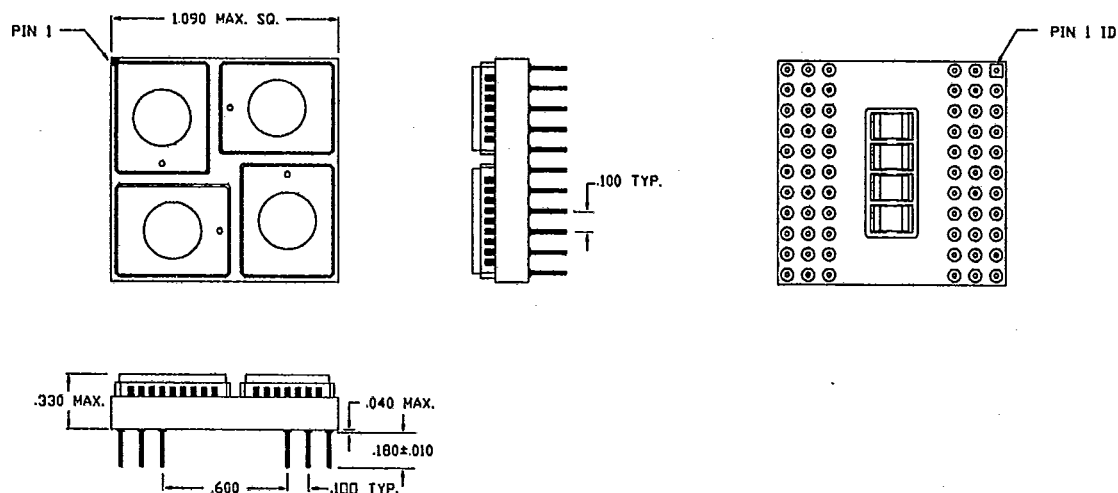
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ORDERING INFORMATION

DP	V12832	V	- XXX	X		
PREFIX	DEVICE TYPE	PACKAGE	SPEED	GRADE		
					C	COMMERCIAL 0° to +70°C
					I	INDUSTRIAL -40° to +85°C
					M	MILITARY -55° to +125°C
					B*	MIL-PROCESSED -55° to +125°C
			200		200	200ns
			250		250	250ns
		V			V	66-PIN PGA VERSAPAC
						UVEPROM 512KX8, 256KX16 OR 128KX32

* B grade modules are not built with 883 devices.

MECHANICAL DIAGRAMS**Dense-Pac Microsystems, Inc.**

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