DPS9245EB Evaluation Board
User's Guide

LSI LOGIC®

Contents

1	**Introduction**		**3**
2	**Product and Applications Overview**		**3**
3	**Driving the Analog Inputs**		**4**
	3.1	Differential Drive from a Differential Source	5
	3.2	Single-Ended to Differential Configuration (Using Amplifiers)	6
	3.3	Single-Ended to Differential Configuration (Transformer Coupled)	7
	3.4	True Single-Ended Operation of the DPS9245	7
	3.5	Suggested External Signal Sources and Signal Conditioning Techniques	7
4	**Programmable Gain Amplifier (PGA) Gain Control**		**8**
5	**Clock**		**9**
	5.1	DC-Coupling the Clock	9
	5.2	AC-Coupling the Clock	9
6	**16-Bit Parallel ADC Outputs**		**10**
7	**Various Digital Inputs/Outputs**		**10**
	7.1	OE	10
	7.2	OVR_RNG	10
	7.3	RESETB	10
	7.4	BUSYB	11
8	**Power Supplies**		**11**
9	**References, Bandgap and Common-Mode Voltage**		**12**
	9.1	ADC References	13
	9.2	Bandgap/External Bias Capacitor and Resistor	13
	9.3	The Common-Mode Voltage RXCMIN	13
10	**Initializing the DPS9245EB Board**		**14**
11	**Layout Guidelines**		**15**
	11.1	Layers	15

11.2 Power Planes 15
11.3 Routing the 16 “AD” Output Lines 15
11.4 Signal Isolation Issues 15
11.5 High Speed Clock Line 15
11.6 Matching Differential Signals 16
11.7 ADC References 16
11.8 Supply Bypass 16
11.9 Critical Placement 16

Figures

1 Functional Block Diagram of the DPS9245 3
2 Various Options to Drive the PGA Inputs 5
3 Circuit Options to Drive the DPS9245 with a Low Jitter Clock Source 9
4 Power Supply Hook Up to the Evaluation Board 12
5 External Passive Connections for the Bandgap, References and Common Mode Pins 13
6 Top Layer Silk 18
7 Plot of the Top Layer [Signal] 19
8 Plot of the Second Layer [Ground] 20
9 Plot of the Third Layer [Power] 21
10 Plot of the Bottom Layer [Signal] 22
11 Top Level Schematic of the DPS9245E 23

Tables

1 PGA Gain Control 8
2 Quick Reference to the Header Options Available 14
3 Bill of Materials (DPS9245EB, Rev A) 17

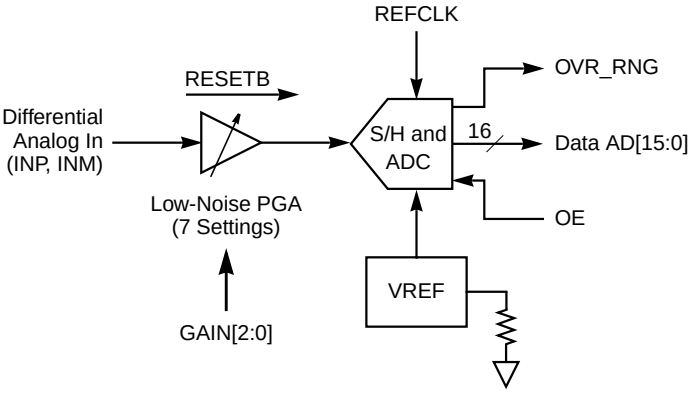
1 Introduction

The DPS9245EB evaluation board is a platform to verify the performance of the DPS9245, 16-bit, 5 Megasamples/s ADC. The purpose of this document is to provide complete details of the functionality and operation of the DPS9245EB. The application note will also focus on the equipment requirements and the various circuit options available on-board. This is followed by suggested guidelines for board layout. The top-level schematic of the board is shown in Figure 11. The board consists of 4 layers; the top and bottom are predominantly signal, the 2nd layer ground and the third layer for power supply. The plot for each layer is shown in Figures 7–10. The silk for the top layer is shown in Figure 6. In addition to the basic hardware (clocks, supplies and input signal generators), the user must also have a logic analyzer or some equivalent means to acquire digital data, along with FFT processing software to fully evaluate the ADC.

2 Product and Applications Overview

The DPS9245 is a 16-bit ADC with a maximum sampling rate of 5 Megasamples/s. The combination of an integrated, on-chip low noise programmable gain amplifier (PGA), sample and hold function and internal reference makes the DPS9245 a self-contained data acquisition sub-system. A functional diagram of the chip is shown in Figure 1.

Figure 1 Functional Block Diagram of the DPS9245



The PGA has an input-referred noise of 8 nV/MHz and a typical dynamic range of 100 dB at the maximum PGA gain of 20 dB. The high level of integration, greater than 1 kΩ input impedance of the PGA, simple initialization and 16-bit parallel output interface synchronized to the sampling clock makes the DPS9245 very user friendly.

This versatile CMOS ADC has low power dissipation of 465 mW at the highest sampling rate and is available in a 44-lead LQFP.

Possible applications for this ADC are listed below:

- Analog front end for high-end DSP processors
- Data acquisition
- Automatic test equipment
- Instrumentation
- MRI, imaging
- High performance scanners and copiers
- DSL/copper line test equipment applications
- CCD cameras and video imaging
- Wireless base station receivers

3 Driving the Analog Inputs

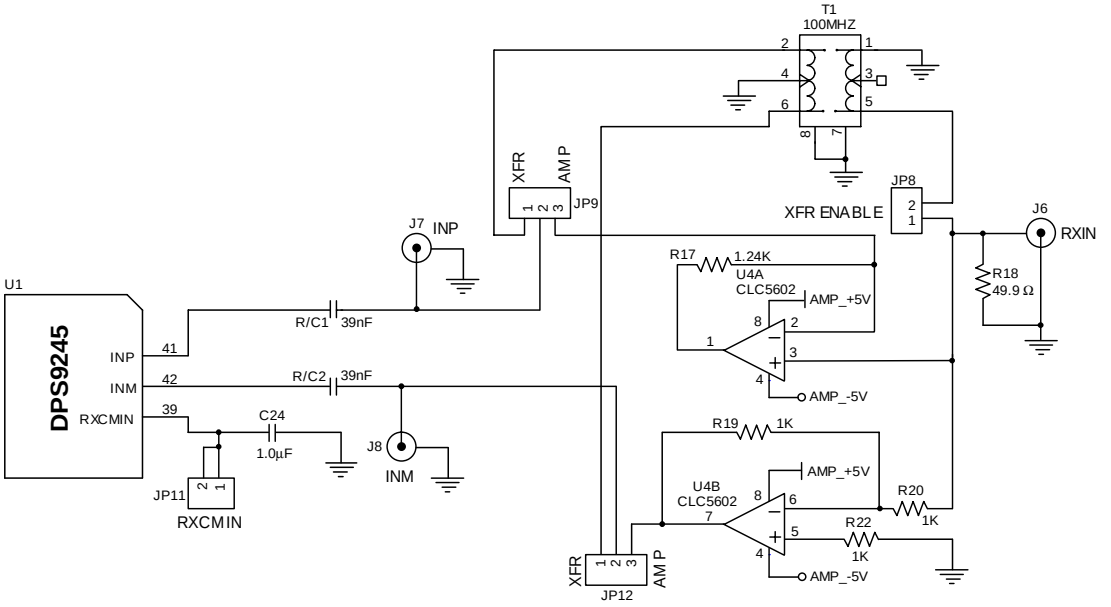
Figure 2 shows the various hardware configurations available on the evaluation board to drive the analog inputs of the ADC.

Note: The amplifier U4A is connected in unity gain. Tapping the output from the noninverting terminal gives the best performance. This is not an error.

R/C1 or R/C2 should be stuffed with a capacitor if the inputs are AC-coupled or stuffed with a 0 Ω resistor if the inputs are DC-coupled.

The common-mode voltage RXCMIN is generated internally.

Figure 2 Various Options to Drive the PGA Inputs



3.1 Differential Drive from a Differential Source

The DPS9245 performs best when driven with a fully balanced differential signal between INP and INM centered on common-mode voltage RXCMIN. Balanced differential inputs can directly be connected to the SMBs J7 (INP) and J8 (INM) bypassing the on-board amplifiers and transformer. The center pins of headers JP9 and JP12 can also be used to interface with the PGA inputs. Driving differentially helps reduce the even order harmonics.

The maximum peak to peak differential voltage swing between INP and INM should be no more than 5 Vppd.

If a differential source is not available, the board has two ways to convert a single-ended input signal into a differential one, as described in sections 3.2 and 3.3.

3.2 Single-Ended to Differential Configuration (Using Amplifiers)

Note: There is gain of 2 from J6 to the inputs of the PGA when using the on-board amplifiers. Hence the inputs should be attenuated to compensate for this gain.

The single-ended to differential conversion is done using Comlinear's dual low-noise CLC5602 amplifiers.

3.2.1 AC-Coupled Inputs

To enable the amplifiers:

1. Keep header JP8 open.
2. Connect the center pins of headers JP9 and JP12 to the pin marked AMP i.e. Short pins 2 and 3.
3. To ac-couple the inputs stuff R/C1 and R/C2 with 39 nF, low ESR caps. Using these dc blocking caps between the amplifier outputs and the converter inputs a simple level-shifting scheme is implemented.

WARNING: This evaluation board is NOT optimized for dc-coupled inputs. The DPS9245 has no loss of performance when operated either in the ac or dc-coupled mode. To fully evaluate the performance in the dc-coupled mode, LSI Logic, recommends using the AD8138 low distortion differential ADC driver. The AD8138 converts single-ended signals into differential ones and permits reference to an external common mode voltage.

3.2.2 DC-Coupled Inputs without Level Shift

If the analog input signal is biased around the common-mode voltage, then to dc-couple the inputs stuff R/C1 and R/C2 with 0 Ω resistors. Follow steps [1–2] as described in Section 3.2.1, "AC-Coupled Inputs."

3.2.3 3.2.3 DC-Coupled Inputs with Level Shift

This mode of operation is possible when using the AD8138 amplifier.

3.3 Single-Ended to Differential Configuration (Transformer Coupled)

To be used only when the input frequency is > 100 kHz (the transformer is a DC block).

1. Close header JP8.
2. Connect the center pins of headers JP9 and JP12 to the pins marked XFR i.e., Short pins 2 and 1.

To AC-couple the inputs stuff R/C1 and R/C2 with 39 nF, low ESR caps. The common-mode voltage is set internally.

3.4 True Single-Ended Operation of the DPS9245

Even though the ADC performs best when driven differentially, it is possible to drive the device single-ended. In that case, all of the above configurations still apply to one of the two analog inputs; the other analog input should be connected to the RXCMIN reference voltage, or to an external common mode reference.

The performance with a single-ended input will depend strongly on the amount of common mode signal present at the chip RXINP/RXINM inputs. The on-chip PGA performs a single-ended to differential conversion. Hence, the signal entering the ADC is balanced.

3.5 Suggested External Signal Sources and Signal Conditioning Techniques

1. Krohn-hite Model 4402B Ultra pure wave sine wave oscillator. The low noise specification makes it good for SNR measurements. A typical measured value is 82 dB for –1.0 dBFS input. Signal bandwidth of the instrument is limited to 200 kHz.
2. Stanford Research Model-DS335 function generator. Allows good linearity measurements over its entire frequency range. The bandwidth is limited to 3.1 MHz and signals distort when the amplitude exceeds 1.5 Vpp.

LSI Logic uses an in-house board to generate balanced differential single and two-tone inputs. Typical SFDR measurements for a 70 kHz sinewave sampled at 5 MHz is > 90 dB.

To maximize performance select sources with the lowest noise and THD numbers. LSI Logic also recommends using a combination of series inline bandpass/lowpass filters to further condition the input signal for lab testing e.g., TTE filters (KC4-75k-3.75k-50-720B and LE182-1M-50-720B).

4 Programmable Gain Amplifier (PGA) Gain Control

The seven gain steps of the PGA are set using the switch S2. When the switch is in the “OFF” position, the bit value is “0” and when in the “ON” position the bit value is “1”. Table 1 shows the various settings for the switch. The default setting for Gain[2:0] is 0b000 or 0 dB. The gain setting 0b111 is not permitted.

Note: The input impedance changes with PGA gain.

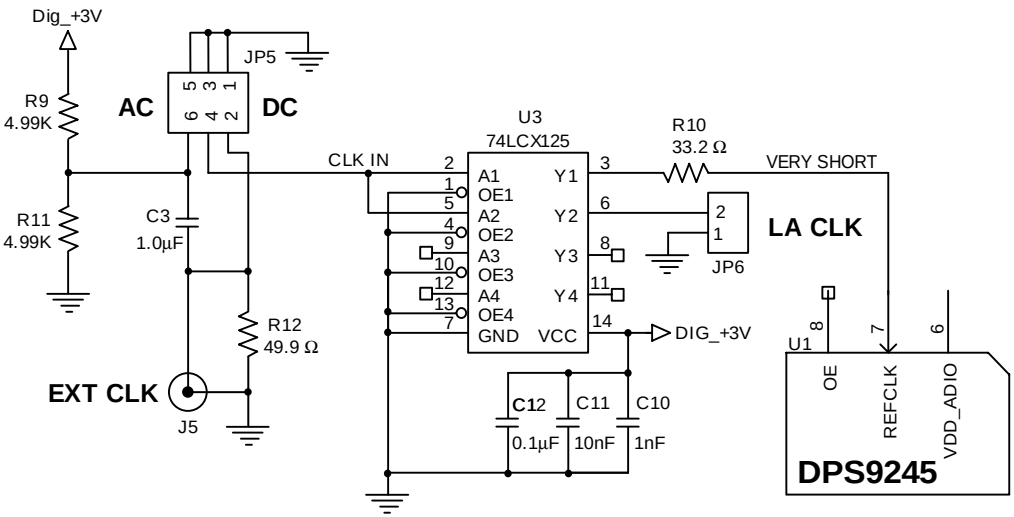
Table 1 PGA Gain Control

GAIN2	GAIN1	GAIN0	PGA Gain [dB]	Input Resistance [KΩ]	Comments
0	0	0	0	5.57	Min. gain
0	0	1	2.9	4.65	
0	1	0	5.8	3.97	
0	1	1	11.8	2.23	
1	0	0	14.8	1.66	
1	0	1	17.5	1.25	
1	1	0	19.5	1	Max. gain
1	1	1	–	–	Not allowed

5 Clock

The DPS9245 requires a low jitter (less than 10 ps), 50% duty cycle clock. Lack of a good source will degrade linearity performance. The maximum clock frequency is 5 MHz. Input the clock at the SMB marked J5 as shown in Figure 3. A 50 Ω resistor terminates the input. If the source impedance of the generator is different, change the value of R12 accordingly. The signal is buffered (using U3) to clean up the rising and falling edges of the clock. A 33 Ω damping resistor is placed in series with the REFCLK pin to prevent signal undershoot at the pin. The clock can either be AC or DC-coupled into the chip.

Figure 3 Circuit Options to Drive the DPS9245 with a Low Jitter Clock Source



5.1 DC-Coupling the Clock

Connect pins 2 and 4 of header JP5 (that is, pins marked DC and RCLK). This is the default setting.

5.2 AC-Coupling the Clock

Connect pins 4 and 6 of header JP5 (that is, pins marked AC and RCLK).

LSI Logic uses the Hewlett Packard HP33120A, a 15 MHz Function Gen./AWG.

6 16-Bit Parallel ADC Outputs

The 16 ADC outputs are buffered using a 16 bit CMOS line driver (U5) and are available at header JP10. The AD0 (LSB) and AD15 (MSB) bits have been labeled. Pin 2 (marked LA CLK) of header JP6 provides a sampling clock for the logic analyzer. The outputs are valid when OE is high, or 3-stated when OE is low. The 16-bit external buffer [U5] is used to decrease the loading on the ADC output pins and help minimize the output switching noise.

The outputs AD[15:0] change on the rising edge of the REFCLK and are valid after 40 ns MAX. (See the *DPS9245 High-Resolution ADC with PGA Datasheet* for more details.)

7 Various Digital Inputs/Outputs

7.1 OE

OE is the output enable signal. The 16 ADC outputs are valid when OE is high or 3-stated when OE is low. OE is pin 8 on-chip and is HIGH during normal operation.

7.2 OVR_RNG

This signal is available at test pin TP5 (marked OVR RNG). A HIGH on this output signal indicates the range of the ADC has been exceeded. To correct the situation, either attenuate the input to the PGA or decrease the PGA gain. OVR_RNG is pin 25 on-chip and is low during normal operation.

7.3 RESETB

The push button switch S1 initializes the ADC. This MUST be done after the power supplies and reference clock are stable. This signal can be monitored at pin 4 (marked RESETB_IN) of header JP7. A buffered version of RESETB_IN is fed directly to the chip. Calibration starts on the

rising edge of this signal. When RESETB is LOW, registers (excluding the ones in the calibration circuitry) are initialized. RESETB is level sensitive and should be held low for at least three clock cycles. RESETB is pin 30 on-chip and is HIGH during normal operation.

7.4 BUSYB

This output signal is available at test pin TP4. This signal goes low on the rising edge of RESETB. A LOW on this pin indicates the ADC is in calibration/initialization mode. Once the calibration is complete, BUSYB turns HIGH and ADC is ready for operation. BUSYB is pin 33 on-chip and is HIGH during normal operation.

8 Power Supplies

The DPS9245EB requires the following power supplies:

- +5 V for the analog and digital sections of the ADC
- +5 and –5 V for the on-board amplifiers
- +3.3 V for the ADC outputs and on board logic ICs.

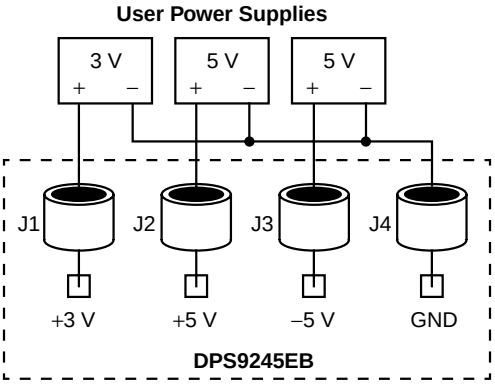
The board has an option to power the ADC outputs with either +3.3 V or +5 V, using the header JP4 (marked ADIO VOLTAGE SELECTOR). This way the entire ADC can be powered from a single +5 V supply, if needed. Powering the ADC outputs off the +3.3 V supplies reduces power consumption and noise generation due to output switching. The +5 V supply is split into three planes (using on-board low pass LC filters) minimizing the coupling between the analog and digital sections, buffer amp, and the ADIO supplies. The supply banana plugs are labeled +3 V, +5 V, –5 V and GND.

When using a bias resistor R21 of 1.43 kΩ, the nominal current drawn from the three supplies is +5 V (100 mA), –5 V (–10 mA) and +3 V (2 mA).

WARNING: Ensure that the supplies are correctly hooked up and a return path is provided to ground (see Figure 4). Failure to do so could destroy the DPS9245, as there are no supply clamping diodes on-board. When the on-board LED's are

lit, the power supplies are correctly hooked up. Do not exceed the supply voltage for any of the input pins.

Figure 4 Power Supply Hook Up to the Evaluation Board



If the proposed application has separate analog and digital power supplies, LSI Logic recommends connecting the VDD_ADC (pins 28 and 44) to the analog section, while connecting VDD_ADIO (pin 6) and VDDD_ADC (pin 3 and 4) to the digital section.

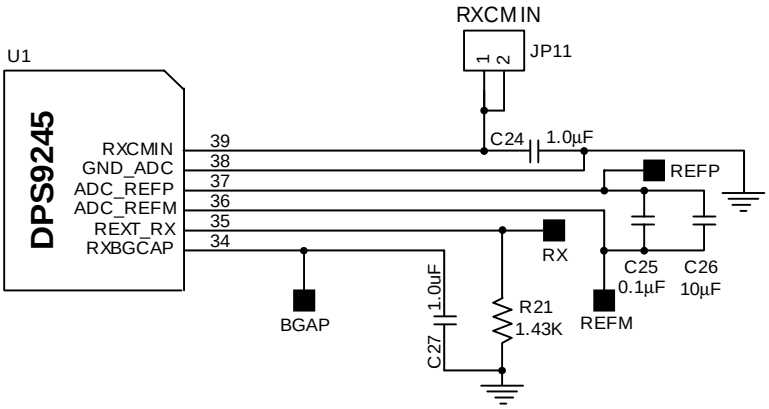
If the proposed application has separate analog and digital ground planes, LSI Logic recommends connecting the GND_ADC (pins 1, 29 and 38) to the analog section, while connecting GND_ADIO (pin 5) and GNDD_ADC (pin 2) to the digital section.

All ground pins of the DPS9245 are shorted to one common ground on the DPS9245EB evaluation board.

9 References, Bandgap and Common-Mode Voltage

This section details the reference voltages and bandgap/bias settings for the board.

Figure 5 External Passive Connections for the Bandgap, References and Common Mode Pins



9.1 ADC References

The ADC full-scale reference voltages are generated on-chip. The high and low reference voltages are available at pins ADC_REFP (pin 37) and ADC_REFM (pin 36) respectively. The references are decoupled by connecting a 10 µF low-ESR/ESL capacitor between the two pins (see Figure 5). The voltage difference across these pins is nominally 2.5 V.

Note: The internal references of the DPS9245 cannot be disconnected or overdriven.

9.2 Bandgap/External Bias Capacitor and Resistor

Connecting a precision resistor R21 to pin 35 (REXT_RX) sets the power dissipation of the ADC. Trade-off between power dissipation and linearity at higher sampling rates (> 5 MHz) and/or for high input frequencies (greater than Nyquist) is done by changing R21. As a general guideline REXT_RX should always be in the range of 800 and to 3.0 kΩ. RXBGCAP (pin 34) is a voltage associated with the bandgap. The external capacitor C27 is used for noise filtering. A value of 1 µF is recommended. The default value of R21 is 1.43 kΩ.

9.3 The Common-Mode Voltage RXCMIN

This voltage is generated internally and is typically 2.40 V. For best results all analog inputs should be centered on this value. The maximum

output drive capability of RXCMIN (pin39) is 47 A (50 kΩ to ground). Output impedance is typically 1 kΩ, and a 1 µF decoupling capacitor is used.

10 Initializing the DPS9245EB Board

Below is a set of basic debugging checks.

1. Set ADIO, the digital output supply to 3.3 V [header JP4].
2. DC-coupled reference clock [header JP5 and SMB J5]. Check amplitude and DC offset of the source.
3. PGA gain set to 0 dB [switch S2].
4. Analog inputs, driving the ADC differentially [check JP12 and JP9, SMB J6 and R/C1, R/C2]. Check the amplitude of the input. Check common-mode (~2.4 V) if the inputs are DC-coupled.
5. Is power supply and return path to ground provided? Are the LED's lit? Are the current specifications being met?
6. Provide a clean clock supply at SMB J5.
7. Once clock and supplies are settled, initialize the ADC by using the RESETB push-button switch.
8. Verify the DC voltage at test points marked BGAP (1.25 V), RX (1.26 V), REFP (3.65 V), and REFM (1.15 V) and RXCMIN (2.4 V). Typical values included for reference only.
9. Using a scope check the 16 ADC outputs before and after the buffer U5.

Table 2 Quick Reference to the Header Options Available

Header	Function
JP4	Digital output power supply selector
JP5	AC or DC coupling for REFCLK
JP9 and JP12	Selecting on board transformer or amplifier option
JP8	Enable transformer

11 Layout Guidelines

Please refer to Figure 7 through Figure 10 in combination with the following suggestions.

11.1 Layers

Multilayer boards are recommended as they offer the advantages of reducing ground impedance and separating the sensitive analog signal from the noisy digital ones. Four layers were used on the board and the layer sequence is signal/ground/power/signal.

11.2 Power Planes

Multiple power planes of +5 V, –5 V, and +3 V are used. This helps to isolate the sensitive signals from the switching digital signals. Low pass LC filters have been used to isolate sections powered by the same supply. The –5 V is used to power the external amplifier U4. The +3 V is used to power the on-board CMOS logic ICs and the 16-bit ADC outputs. The buses back to the main supply jacks should be at least 100 mils wide, WIDER is BETTER.

11.3 Routing the 16 “AD” Output Lines

The routing for these digital wires has been done on one layer (top layer). Constant jumping between the two outside signal layers will degrade the return path of the circulating current.

11.4 Signal Isolation Issues

The most sensitive analog pins are pin 34 through pin 42. These pins are INM, INP, RXCMIN, ADC_REFP and ADC_REFM, REXT_RX and RXBGCAP. It is very important to keep the digital routing (“AD outputs”) far from these analog signals.

11.5 High Speed Clock Line

It is also important to keep the clock line REFCLK [pin7] isolated. The trace carrying the clock signal should be as short as possible. Also

prevent crossing this trace with any varying analog or switching digital signals.

11.6 Matching Differential Signals

INP and INM are differential analog input signals and should be matched and balanced as well as possible. The SMB jacks J7 and J8 should be grouped as a pair.

11.7 ADC References

Keep all traces routed from these pins 36 and 37 (ADC_REFM and ADC_REFP) balanced and as short as possible. Failure to do so will degrade the linearity of the ADC. The most critical components are the decoupling capacitors, especially the 10 µF capacitor between the reference outputs: ADC_REFP and ADC_REFM. Place the capacitor as close as possible to the pins.

11.8 Supply Bypass

The 1000 pF 0805 capacitors should be placed as close as possible to the VDD pins.

11.9 Critical Placement

The capacitor (C27) and resistor (R21) connected to RXBGCAP and REXT_RX should be as close as possible to the main chip. Traces from these pins to the passive components should be kept as short as possible and isolated from any noisy signals on-board.

Table 3 Bill of Materials (DPS9245EB, Rev A)

Item	Reference	Part	Tol	Type	Pwr	Footprint	Manufacturer	Manufacture #	Qty
1	C1,C3,C24,C27	1.0 µF	10%	X7R	10 V	805	MURATA	GRM40X7R105K010AL	4
2	C2,C12,C13,C15, C17,C19,C23,C25, C30,C32	0.1 µF	10%	X7R	25 V	805	MURATA	GRM40X7R104K025AL	10
3	C4,C5,C6,C7,C8, C9,C26	10 µF	80/20	*	16 V	1210	MURATA	GRM235Y5V106Z016AL	7
4	C10,C14,C16,C18, C20,C22,C29,C31	1 nF	5%	COG	50 V	805	MURATA	GRM40COG102J050AD	8
5	C21,C11	10 nF	5%	*	50 V	1206	PANASONIC	ECH-U1H103JB5	2
6	D1,D2,D3	RED	*	*	20 mA	SMDLED	PANASONIC	LN1271R	3
7	JP4,JP9,JP12	1 x 3	*	*	*	HDR1X3	REGAL	4070-SH-3	3
8	JP5	2 x 3	*	*	*	HDR2X3	REGAL	4071-DH-6	1
9	JP6,JP8,JP11,JP15	1 x 2	*	*	*	HDR1X2	REGAL	4070-SH-2	4
10	JP7	2 x 2	*	*	*	HDR2X2	REGAL	4071-DH-4	1
11	JP10	2 x 16	*	*	*	HDR2X16	REGAL	4071-DH-32	1
12	J1,J2,J3,J4	Banana Jack_AM	*	*	*	BANANA JACK_ AM	JOHNSON	108-0740-001	4
13	J5,J6,J7,J8	SMB_413990-1-00	*	*	*	SMB	AMP	413990-1-00	4
14	L1,L2,L3,L4,L5,L6	3.3 µH	5%	*	*	1210	DELEVAN	1210-332J	6
15	R/C1,R/C2	39 nF	5%	*	50 V	1210	PANASONIC	ECH-U1H393JB5	2
16	RP1,RP2	33	*	*	*	RP16W	BOURNS	4816P-T01-330	2
17	R1,R19,R20,R22	1 kΩ	1%	*	1/8 W	1206	PANASONIC	ERJ-8ENF1001V	4
18	R2,R3,R4,R5,R9, R11,R13,R14,R15,R16	4.99 kΩ	1%	*	1/8 W	1206	PANASONIC	ERJ-8ENF4991V	10
19	R6,R7,R8	499 Ω	1%	*	1/8 W	1206	PANASONIC	ERJ-8ENF4990V	3
20	R10	33.2 Ω	1%	*	1/8 W	1206	PANASONIC	ERJ-6ENF33R2V	1
21	R18,R12	49.9 Ω	1%	*	1/8 W	1206	PANASONIC	ERJ-8ENF49R9V	2
22	R17	1.24 kΩ	1%	*	1/8 W	1206	PANASONIC	ERJ-8ENF1241	1
23	R21	1.43 kΩ	1%	*	1/8 W	1206	PANASONIC	ERJ-8ENF1431V	1
24	S1	EVQ-11G05R	*	*	*	SMALL-PUSH	PANASONIC	EVQ-11G05R	1

Table 3 Bill of Materials (DPS9245EB, Rev A) (Cont.)

Item	Reference	Part	Tol	Type	Pwr	Footprint	Manufacturer	Manufacture #	Qty
25	S2	TPST	*	*	*	SWDIP6	CandK	CKN3002-ND	1
26	TP1,TP2,TP3,TP4,TP5	1514-2	*	*	*	ST1514	KEYSTONE	1514-2	5
27	T1	100 MHZ	*	*	*	XFORM	MINI-CIRCUITS	TTM01-1	1
28	U1	DPS9245	*	*	*	44QFP	LSI Logic	DPS9245	1
29	U2	74HC14	*	*	*	SO14	FAIRCHILD	74HC14M	1
30	U3	74LCX125	*	*	*	SO14	FAIRCHILD	74LCX125	1
31	U4	CLC5602	*	*	*	SO8	COMLINEAR	CLC5602M	1
32	U5	74LCX16244	*	*	*	SSOP48	FAIRCHILD	74LCX16244MEA	1

Figure 6 Top Layer Silk

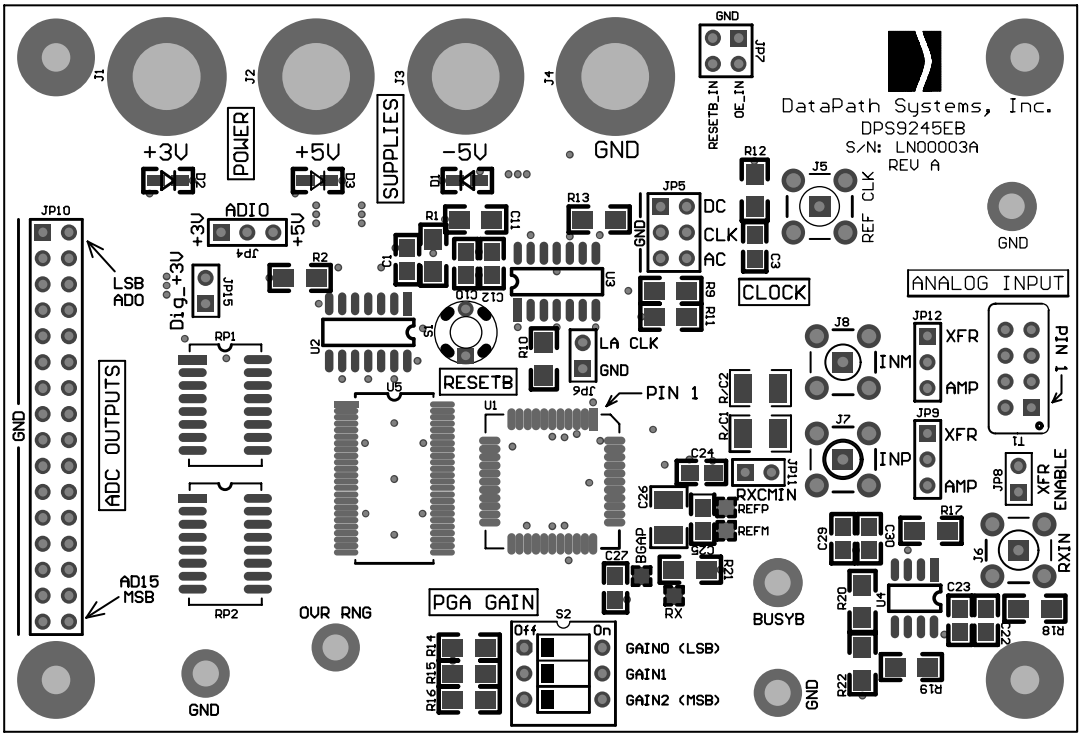


Figure 7 Plot of the Top Layer [Signal]

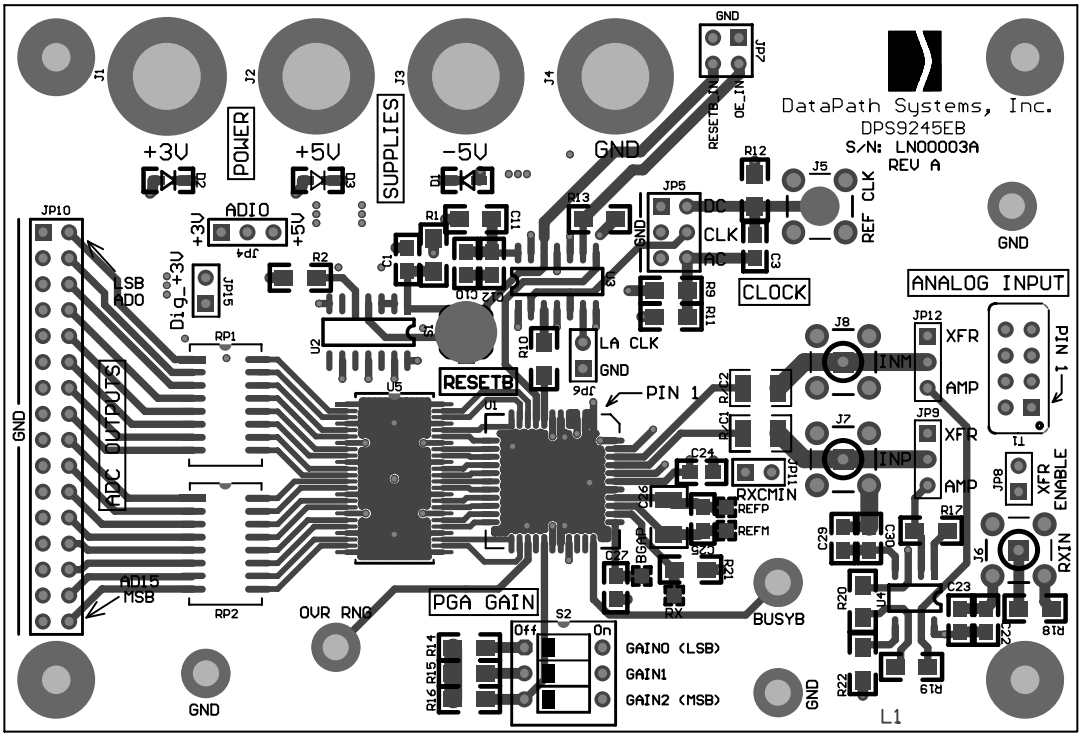


Figure 8 Plot of the Second Layer [Ground]

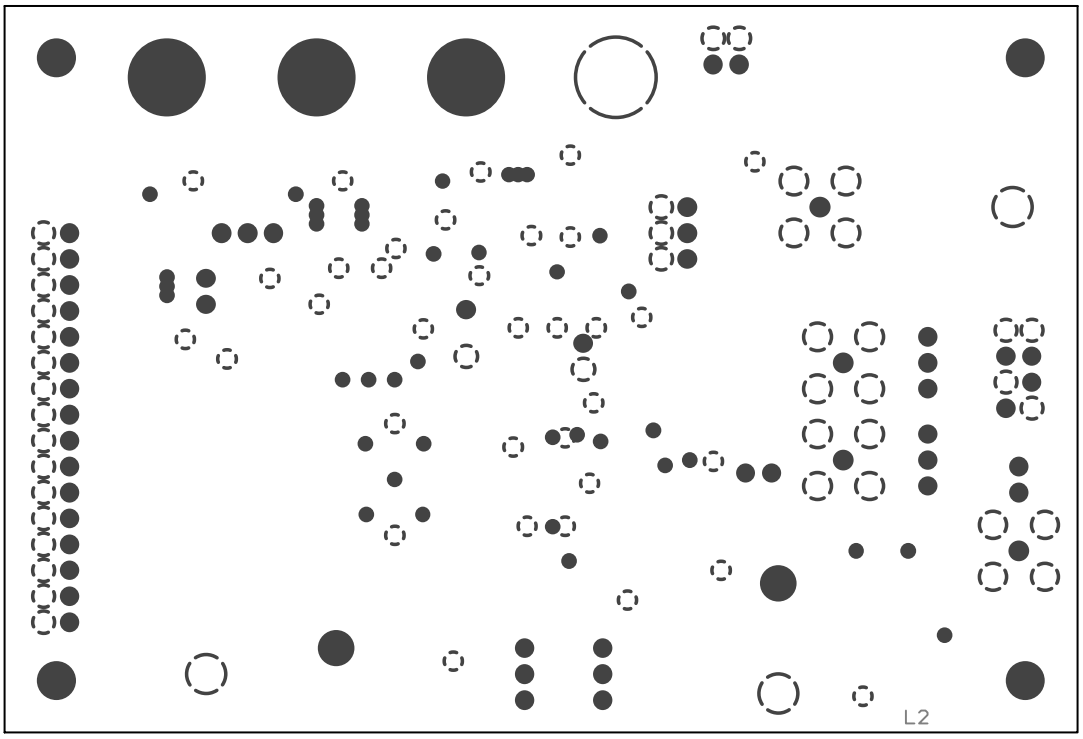


Figure 9 Plot of the Third Layer [Power]

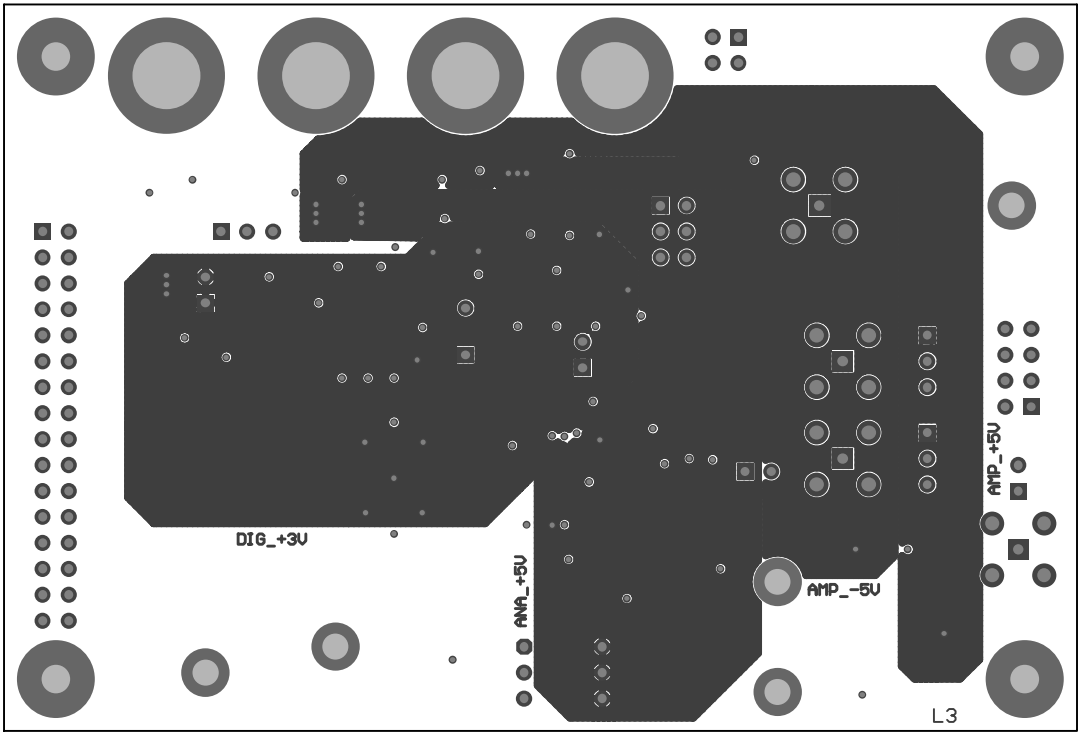


Figure 10 Plot of the Bottom Layer [Signal]

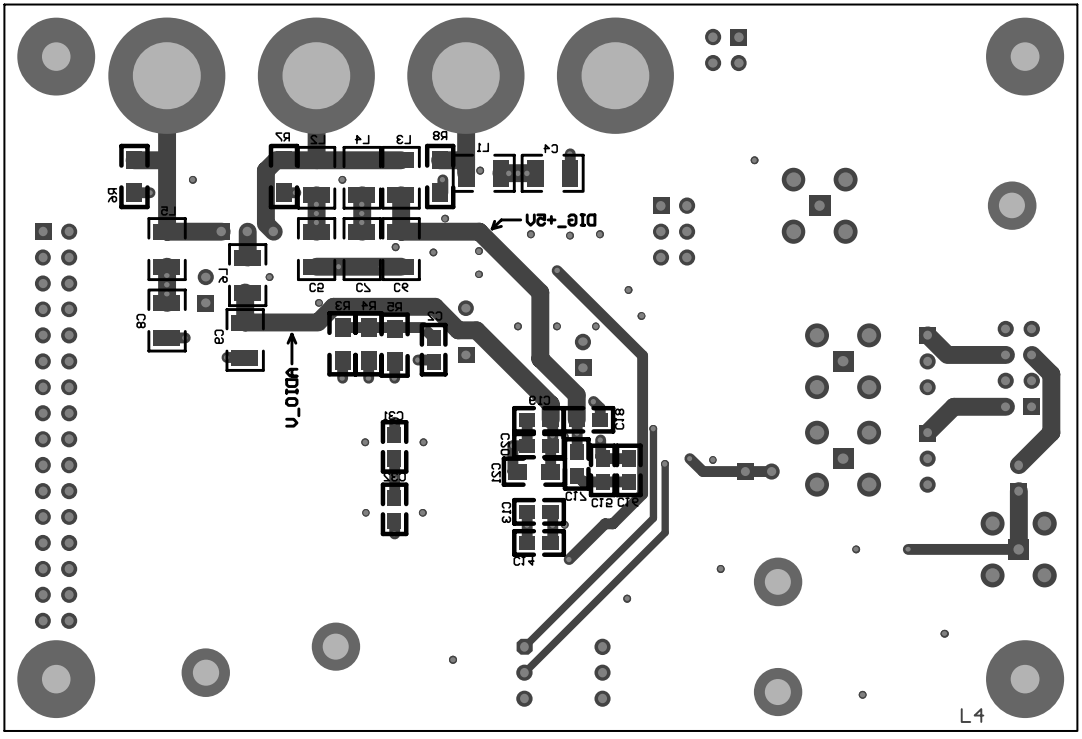
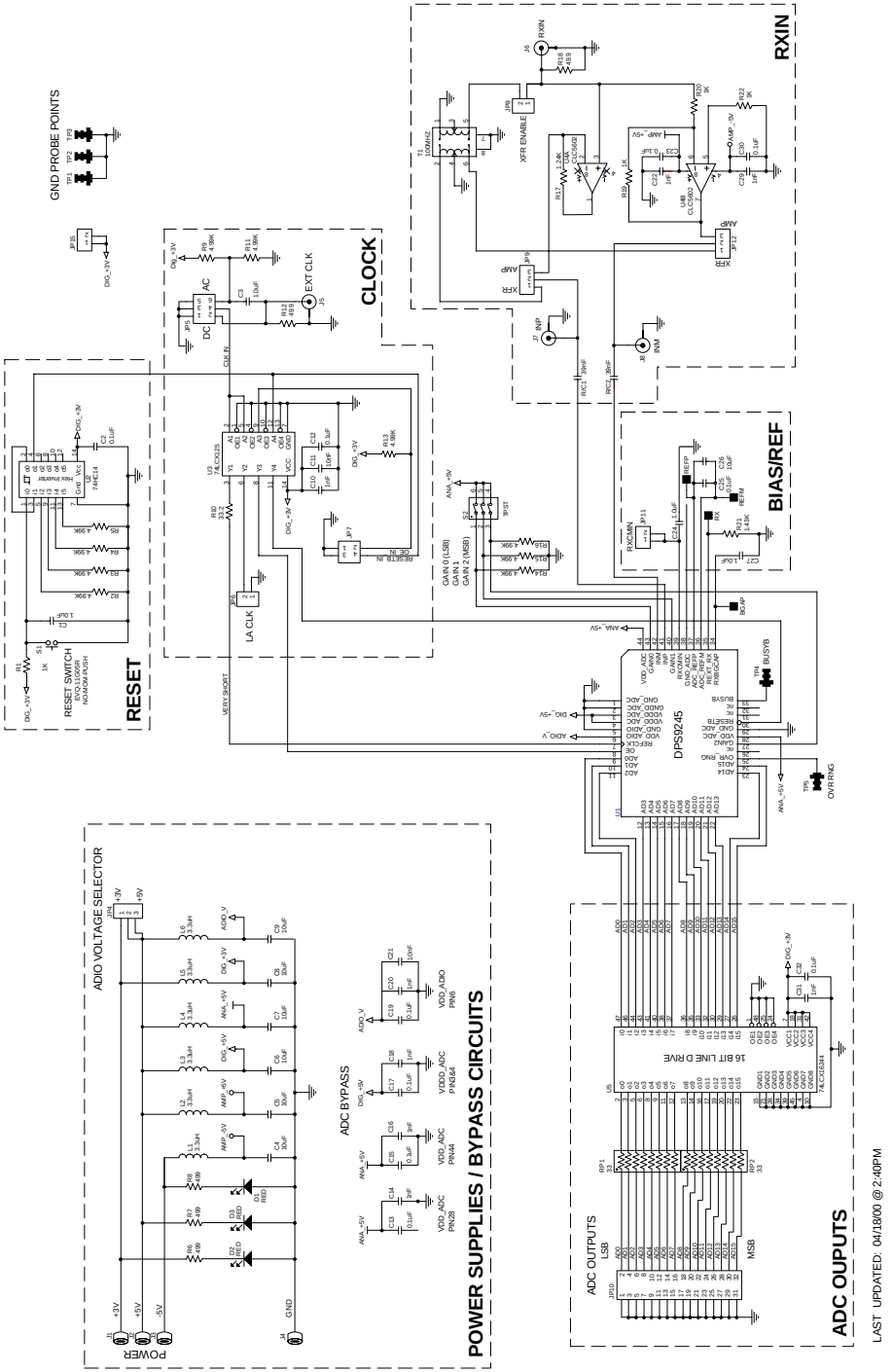


Figure 11 Top Level Schematic of the DPS9245E



Notes

Headquarters

LSI Logic Corporation
North American Headquarters
Milpitas CA
Tel: 408.433.8000
Fax: 408.433.8989

LSI Logic Europe Ltd
European Headquarters
Bracknell England
Tel: 44.1344.426544
Fax: 44.1344.481039

LSI Logic K.K.
Headquarters
Tokyo Japan
Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

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