

CYPRESS
SEMICONDUCTOR

CYM1622

64K x 16 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
— Access time of 25 ns
- Low active power
— 2.2W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Pinout compatible with CYM1611 and CYM1624
- Low profile
— Max. height of .50 in
- Small PCB footprint
— 0.5 sq. in. (ceramic)
— 0.68 sq. in. (FR4)

Functional Description

The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 64K x 4 static RAMs mounted onto a vertical substrate with pins. The pinout of this module is compatible with two other Cypress modules (CYM1611 and CYM1624) to maximize system flexibility.

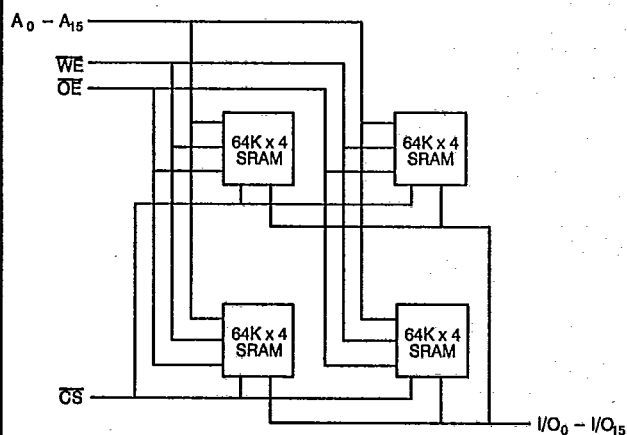
Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into

the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

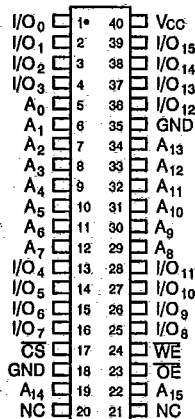
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1622-1

Pin Configuration

VDIP
Top View

1622-2

Selection Guide

	1622-25	1622-30	1622-35	1622-45
Maximum Access Time (ns)	25	30	35	45
Maximum Operating Current (mA)	400	400	400	400
Maximum Standby Current (mA)	140	140	140	140



T-46-23-14

CYM1622

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature	-65°C to +125°C
Ambient Temperature with Power Applied	-10°C to +80°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
Output Current into Outputs (LOW)	20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

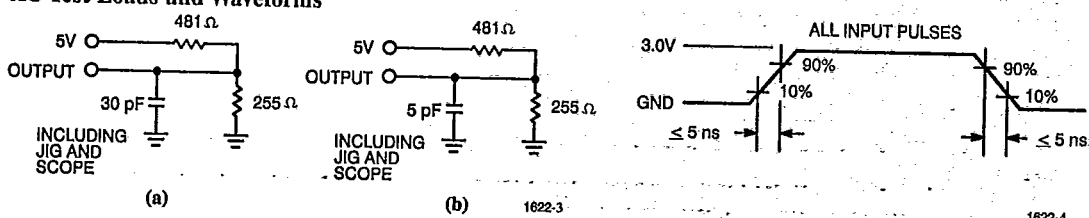
Parameters	Description	Test Conditions	CYM1622		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		400	mA
I _{SB1}	Automatic CS Power-Down Current	V _{CC} = Max.; CS ≥ V _{IH} , Min. Duty Cycle = 100%		140	mA
I _{SB2}	Automatic CS Power-Down Current	V _{CC} = Max.; CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		80	mA

Capacitance^[2]

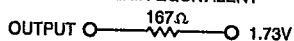
Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	35	pF
C _{OUT}	Output Capacitance		15	pF

Notes:1. V_{IL(MN)} = -3.0V for pulse widths less than 20 ns.

2. Tested on a sample basis.

AC Test Loads and Waveforms

Equivalent to: THEVENIN EQUIVALENT





T-46-23-14

CYM1622

Switching Characteristics Over the Operating Range^[3]

Parameters		Description	1622-25		1622-30		1622-35		1622-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
t _{RC}	Read Cycle Time	25		30		35		45		ns	
t _{AA}	Address to Data Valid	25		30		35		45		ns	
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns	
t _{ACS}	$\overline{CS}$ LOW to Data Valid	25		30		35		45		ns	
t _{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns	
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns	
t _{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20		20	ns	
t _{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		3		ns	
t _{HZCS}	$\overline{CS}$ HIGH to High Z ^[4]		15		20		20		20	ns	
t _{PU}	$\overline{CS}$ LOW to Power-Up	0	25	0	30	0	35	0	45	ns	
t _{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45	ns	
WRITE CYCLE ^[5]											
t _{WC}	Write Cycle Time	25		30		35		45		ns	
t _{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns	
t _{AW}	Address Set-Up to Write End	20		25		30		40		ns	
t _{HA}	Address Hold from Write End	3		3		3		3		ns	
t _{SA}	Address Set-Up to Write Start	2		2		2		2		ns	
t _{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns	
t _{SD}	Data Set-Up to Write End	15		20		20		25		ns	
t _{HD}	Data Hold from Write End	2		2		2		2		ns	
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns	
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[4]	0	15	0	15	0	15	0	20	ns	

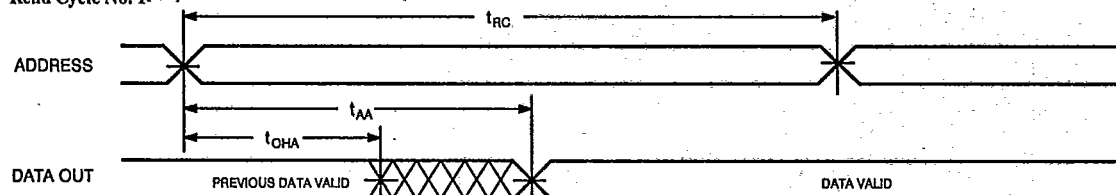
Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input

set-up and hold timing should be reference to the rising edge of the signal that terminates the write.

- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{CS} = V_{IL}$.
- Address valid prior to or coincident with $\overline{CS}$ transition LOW.
- If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

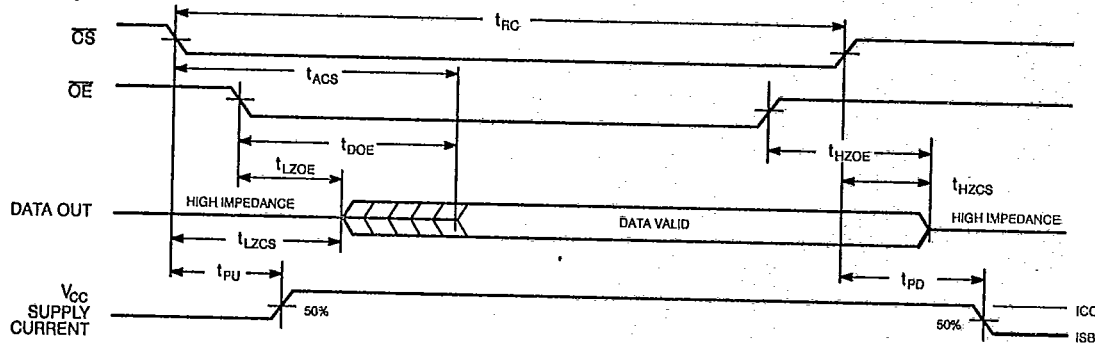
Read Cycle No. 1^[6, 7]

1622-5



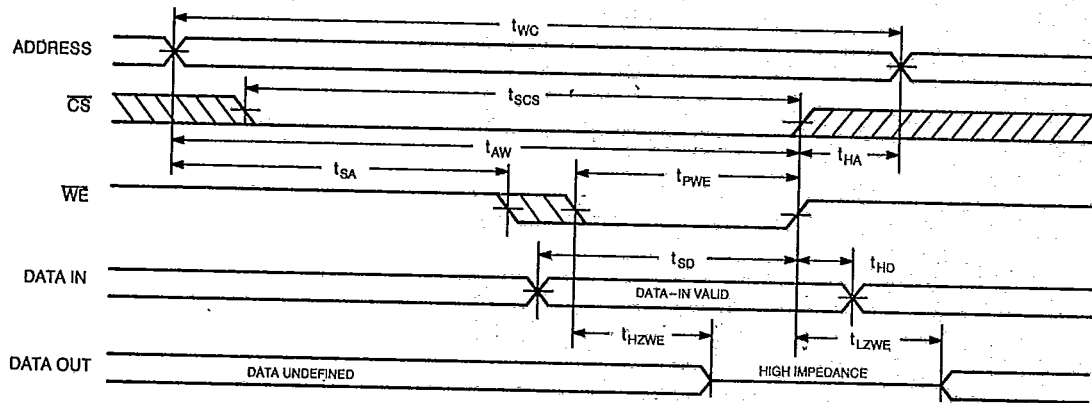
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



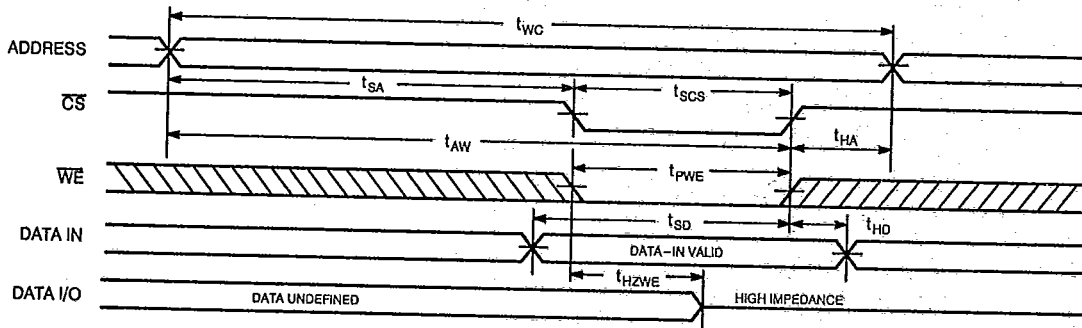
1622-6

Write Cycle No. 1 (WE Controlled)[5]



1622-7

Write Cycle No. 2 (CS Controlled)[5, 9]



1622-8

MODULES



T-46-23-14

CYM1622

Truth Table

CS	OE	WE	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power--Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CYM1622HV-25C	HV03	Commercial
	CYM1622PV-25C	PV04	
30	CYM1622HV-30C	HV03	Commercial
	CYM1622PV-30C	PV04	
35	CYM1622HV-35C	HV03	Commercial
	CYM1622PV-35C	PV04	
45	CYM1622HV-45C	HV03	Commercial
	CYM1622PV-45C	PV04	

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