CPL16V8

CMOS PROGRAMMABLE LOGIC ARRAY WITH OUTPUT MACROCELLS (20-PIN)

Advance Information

FEATURES/BENEFITS

- **Equivalent to industry standard 16V8 architecture, superset of CPL20 family**
- **Three speed grades:**
  t_{PD} = 20ns Max, t_{PD} = 25ns Max, t_{PD} = 30ns Max
- **Two power grades: 45mA Max, 70mA Max**
- **CMOS, UV-erasable EPROM cell allows reprogrammability in windowed packages**
- **8 input/output macrocells for maximum flexibility**
  - **Up to 16 inputs and 8 outputs**
  - **Programmable output polarity**
  - **Registered or combinatorial output selection**
- **Test array and preloadable output registers for improved testability**
- **100% functional, AC and programming tests improve reliability and programming yields**
- **>2000V ESD input protection**
- **Programmable security bit to prevent CPL pattern duplication**

DESCRIPTION

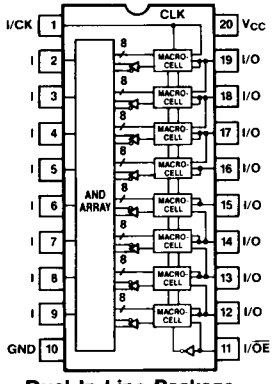
The CPL16V8 is a high-speed CMOS electrically programmable, UV-erasable device with an advanced architecture. The device is manufactured using a 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the device allows for 100% programming, functional, and AC testing, resulting in a highly reliable end product and 100% programming yields.

The CPL16V8 uses the standard programmable AND/Fixed OR logic array structure familiar to most programmable logic users to implement complex logic functions. The array is made up of 8 sets of product terms, each connected to a programmable macrocell via an OR gate. Eight product terms comprise each set, where they can be connected to 16 inputs, true or complement. Every output from the array feeds a programmable macrocell enabling it to be programmed as a combinatorial or registered, active high or low output.

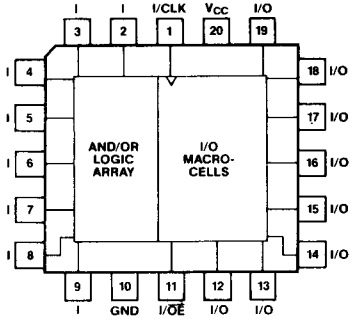
The 16V8 device can be housed in a 20-pin plastic DIP, 20-pin PLCC, or a windowed 20-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The CPL device in a plastic package is One-Time-Programmable (OTP) and may not be erased.

3

PIN CONFIGURATIONS

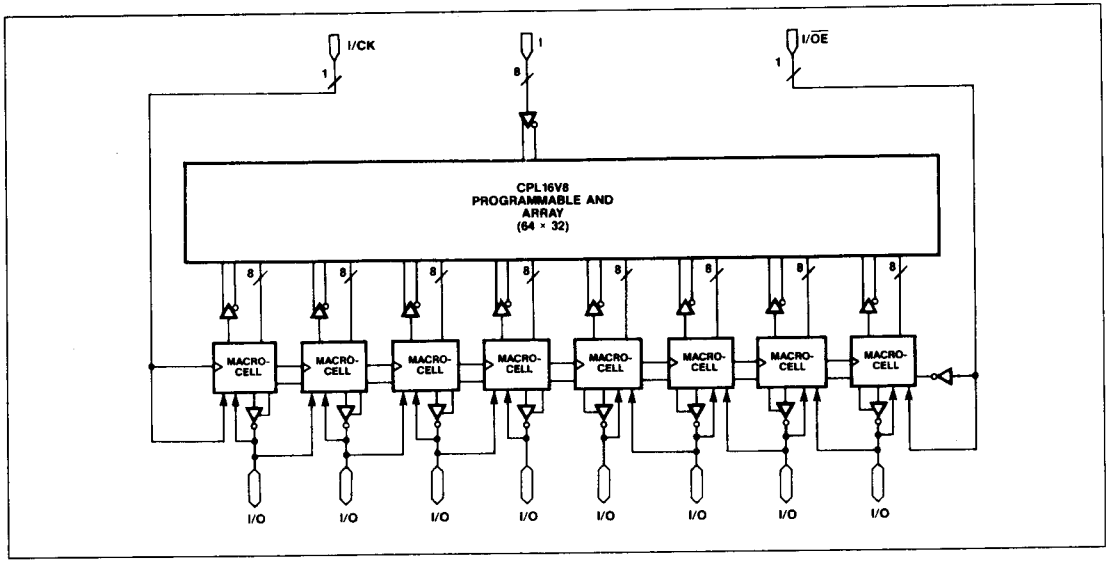


Dual In-Line Package



Plastic Leaded Chip Carrier

Figure 1. Block Diagram



The block diagram of the CPL16V8 device is shown in Figure 1. There are 10 dedicated inputs and 8 programmable macrocell outputs, which may also serve as inputs. In addition, pin 1 can act as a clock for the D-type registers and pin 11 can act as a common output enable. Each input and its complement is connected to a programmable AND array which contains a total of 64 product terms. Each set of 8 product terms drives an output macrocell.

CONFIGURABLE OUTPUT MACROCELLS

One of the CPL16V8's unique features is its 8 user-configurable output macrocells, shown in Figure 2a. By programming these macrocells, the device is not only capable of emulating all common 20-pin PAL device architectures, but also other architectures which have not previously been available.

There are three main PAL-like architectures that the CPL16V8 will emulate: programmed in Modes 0, 1, and 2:

Mode 0 — PAL architecture with Macrocells configured as Dedicated Inputs and/or Dedicated Combinatorial Outputs without Feedback.

Mode 1 — PAL architecture with all 8 Macrocells configured as Combinatorial Outputs, 6 with Feedback.

Mode 2 — PAL architecture with at least 1 Macrocell configured as a Registered Output. All Macrocells configured with Feedback.

These three modes are obtained by the programming of certain architectural control bits: SYN, AC0, AC1(n), and POL(n), which configure each macrocell in the CPL16V8. They are specified in the design file created during the design process and are completely transparent to the user.

A truth table in Figure 2b summarizes the output macrocell configurations that result when the architectural control bits are programmed.

REGISTERED OUTPUT CAPABILITY

Registered output capability is controlled by the SYN bit. If SYN is programmed HIGH (modes 0 and 1), the device outputs will be non-registered (asynchronous) and pins 1 and 11 stay as data inputs. If SYN is programmed LOW (mode 2), at least one output will be registered (synchronous) and pin 1 becomes the clock input while pin 11 becomes the common output enable for the registered output(s).

FUSE MAP COMPATIBILITY

The SYN bit is also used to maintain full JEDEC compatibility with standard 20-pin PAL device architectures. In mode 1, the SYN bit is inverted and replaces AC0 of the Input Feedback Multiplexer in the two outermost macrocells (pins 12, 19).

Figure 2a. Output Macrocell w/ Configuration Bits

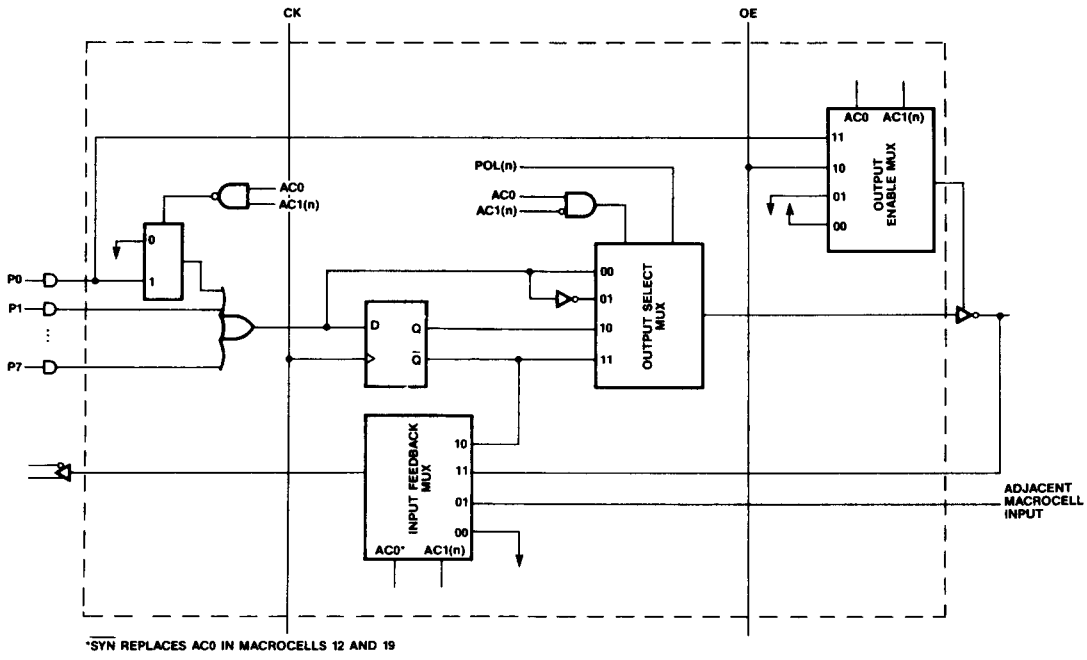


Figure 2b. Truth Table for Configuration Bits

Mode	SYN	AC0	AC1(n)	Output Macrocell Configuration	Notes
0	1	0	1	I/O Configured as Input, Output is Disabled.	Pins 1, 11 are data inputs. No feedback. Pins 15, 16 can only be outputs.
			0	I/O Configured as Dedicated Combinatorial Output, Output Always Enabled.	
1	1	1	1	All Outputs are Combinatorial — 16L8, 16H8, or 16P8 Configuration Only	Pins 1, 11 are data inputs. Pins 12, 19 can only be outputs.
2	0	1	1	I/O is Configured as Combinatorial Output in Registered Device	Pin 1 = $\overline{CK}$, Pin 11 = $\overline{OE}$
			0	I/O is Configured as Registered Output	

POL(n)	Output Polarity
0	Active Low
1	Active High

I/O AND OUTPUT ENABLE CONTROL

Input/Output control is selected via the AC0 control bit. If AC0 is programmed LOW (mode 0), each I/O is configured either as a dedicated input with the output always disabled, or as a dedicated combinatorial output with no feedback. If AC0 is programmed HIGH (modes 1 and 2), array feedback is allowed with the resultant outputs being combinatorial or registered.

Together with the AC0 bit, eight AC1(n) control bits individually determine the final configuration of each macrocell, except for the output's polarity. With AC0 LOW (mode 0), an AC1 bit programmed LOW will direct an I/O to be a dedicated input by disabling the macrocell's three-state output buffer, and an AC1 bit programmed HIGH will direct an I/O to be a dedicated output by permanently enabling the output buffer. With AC0 HIGH (modes 1 and 2), an AC1 bit programmed LOW will direct an output to be registered and have common output enable control, whereas an AC1 bit programmed HIGH will direct an output to be combinatorial and have the output enable controlled separately from a product term.

PROGRAMMABLE POLARITY

Finally, the polarity of each output macrocell is individually determined by the POL(n) bit. If POL(n) is programmed LOW, the macrocell output will be active LOW and if POL(n) is programmed HIGH, the output will be active HIGH.

EXAMPLE MACROCELL CONFIGURATIONS

Examples of the resultant CPL16V8 macrocell configurations for modes 0, 1, and 2 are illustrated in Figures 3, 4, and 5, respectively. Note that these three modes provide four main output configurations: combinatorial active low, combinatorial active high, registered active low, and registered active high.

When a registered output is chosen, the signal is shifted out on the positive clock transition to the I/O pin and also fed back into the array, providing current status information to the programmable array. This is important for state machine applications. When a combinatorial output is chosen or when the output is disabled and the signal is on the I/O pin, the signal is also fed back into the array, (except for pins 12 and 19 in mode 1).

Figure 3. Mode 0 Macrocell Configuration Example (Four I/O Cells)

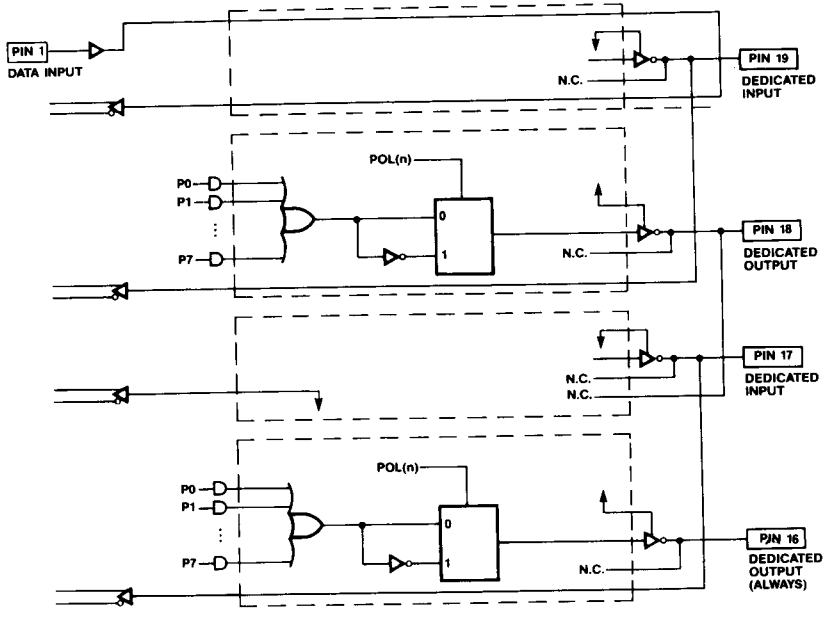


Figure 4. Mode 1 Macrocell Configuration Example (Two I/O Cells)

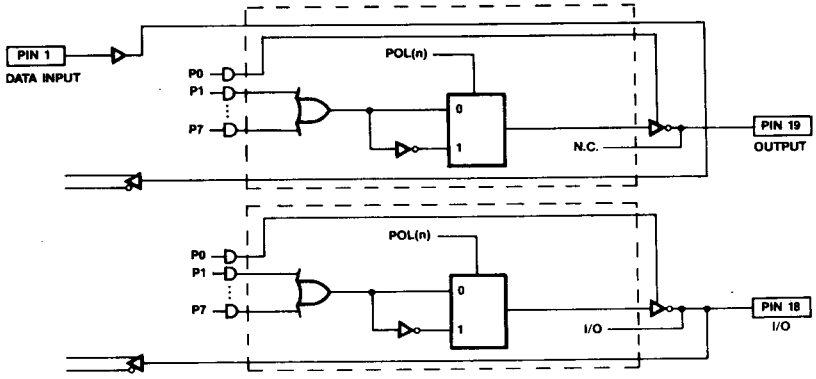
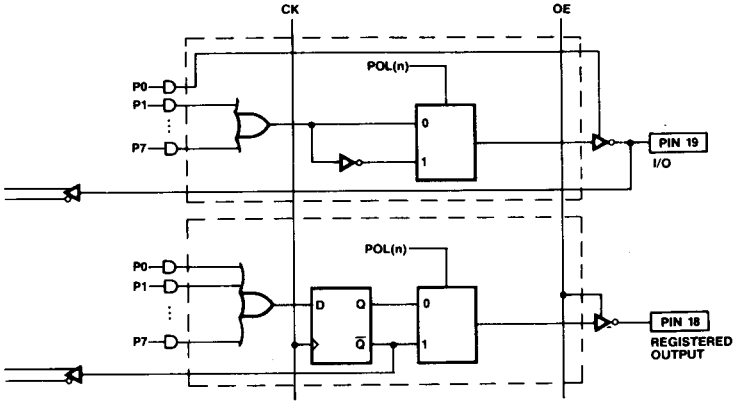


Figure 5. Mode 2 Macrocell Configuration Example (Two I/O Cells)



POWER-UP RESET

During system power-up, each register in the CPL16V8 will be reset to a logic low, to ensure predictable system initialization. Actual output states, however, will be low or high, depending on the polarity chosen at each output. For reliable resets, the V_{CC} rise must be monotonic and the clock input must not change for 1μs.

SECURITY BIT

To prevent a proprietary CPL16V8 design from being copied without authorization, a security bit has been provided. This security bit is programmed via the designer's logic programmer. Once this is done, the read, verify, and preload operations are disabled, which completely secures the device.

TEST FEATURES

Register Preload

To ease functional testing, the CPL16V8 device is equipped with a register preload feature that allows an arbitrary state value to be loaded into any or all of its registers from the output pins. This makes it possible to check and verify any logical state transition, without having to run through an entire test vector sequence. Also, by using register preload, all possible states can be tested to guarantee proper in-system operation.

Test Array

Another feature of the CPL16V8 is the on-chip test array which increases the device reliability by allowing each product term to be tested. The test array is programmed by Samsung to verify final functional and AC yields of the packaged device before shipping. When using the test array to test the device (even if the security bit has been programmed), only the input terms in the shaded portion of the functional block diagram are accessed. During normal operation, the test arrays are not accessed. As a result, the test array facilitates simple and shortened testing.

Input Term Testing

Finally, the CPL16V8 has additional product terms, one on output 12 and one on output 19, which are controlled by the device's input terms. These product terms allow testing of all input structures and are programmed for functional and AC testing of the packaged device, before shipping. The additional product terms are not accessed as part of the normal operation. Having both input term testing and test arrays allows Samsung to provide a packaged device of the highest quality.

ERASURE (windowed-CERDIP only)

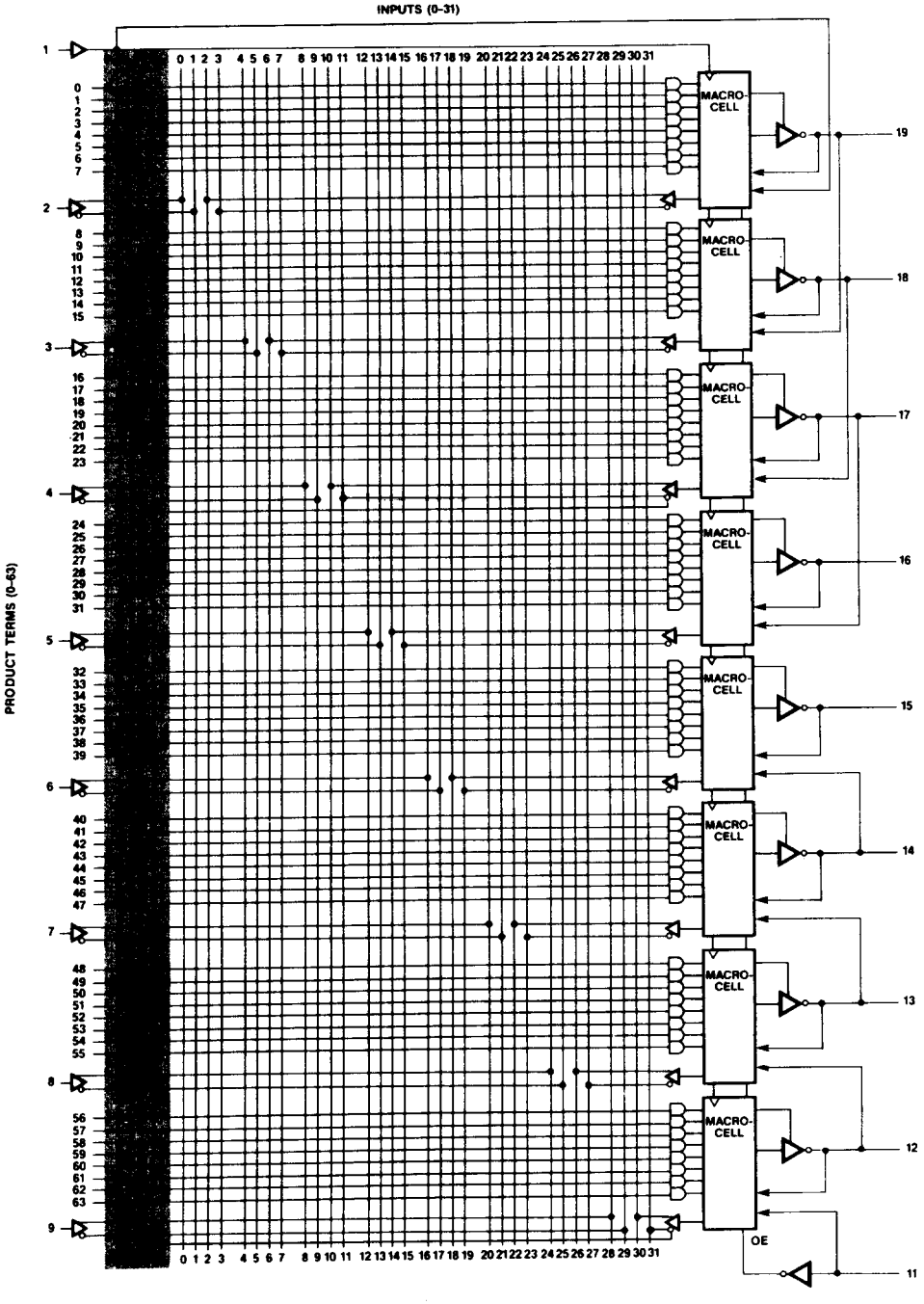
The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose — 25 Wsec/cm^2)

If an ultraviolet lamp with a 12 mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL16V8 FUNCTIONAL LOGIC DIAGRAM



CPL16V8 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)				0.8	V
High Level Input Voltage	V_{IH}	(Note 4)			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$			-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA			0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.2mA		2.4		V
Off-State Output Leakage Current	I_{OZ}	V_{CC} = Max	$V_{SS} \leq V_O \leq V_{CC}$			±10	μA
Power Supply Current	I_{CC}	V_{IN} = GND, I_{OUT} = 0mA	V_{CC} = MAX	"L" STD		45 70	mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Capacitance

Parameter	Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz		8	

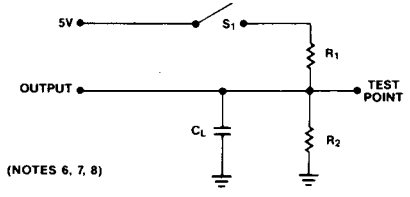
AC Electrical Characteristics

Over Recommended Operating Conditions (Note 5)

Parameter		Symbol	CPL16V8-20 COM/IND		CPL16V8-25 CPL16V8L-25 COM/IND		CPL16V8L-30 COM/IND		Unit
			Min	Max	Min	Max	Min	Max	
Input or Feedback to Non-Registered Output		t_{PD} (Note 8)		20		25		30	ns
Clock to Registered Output or Feedback		t_{CO}		15		15		20	ns
Pin 11 to Output Enabled		t_{PZX11}		18		20		25	ns
Pin 11 to Output Disabled		t_{PXZ11}		18		20		25	ns
Input to Output Enabled		t_{PZX}		20		25		30	ns
Input to Output Disabled		t_{PXZ}		20		25		30	ns
Setup Time from Input or Feedback to Clock		t_{SU}	15		20		25		ns
Hold Time		t_H	0		0		0		ns
Clock Width (High or Low)		t_W	12		15		15		ns
Clock Period		t_P	30		35		45		ns
Maximum Frequency	Feedback	f_{MAX}	33.3		28.5		22.2		MHz
	No Feedback		41.6		33.3		33.3		

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$

AC Test Circuit



Resistor Values (Ω)

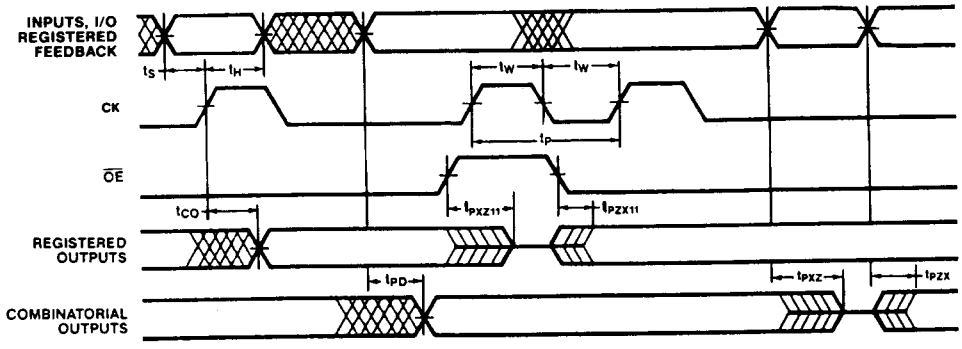
R1	R2
200	390

Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

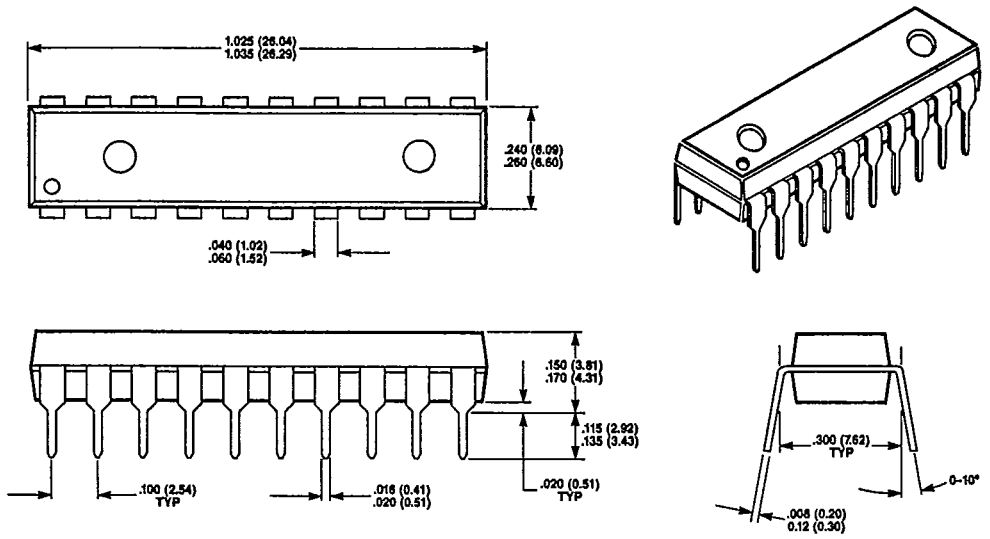
Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

Switching Waveforms



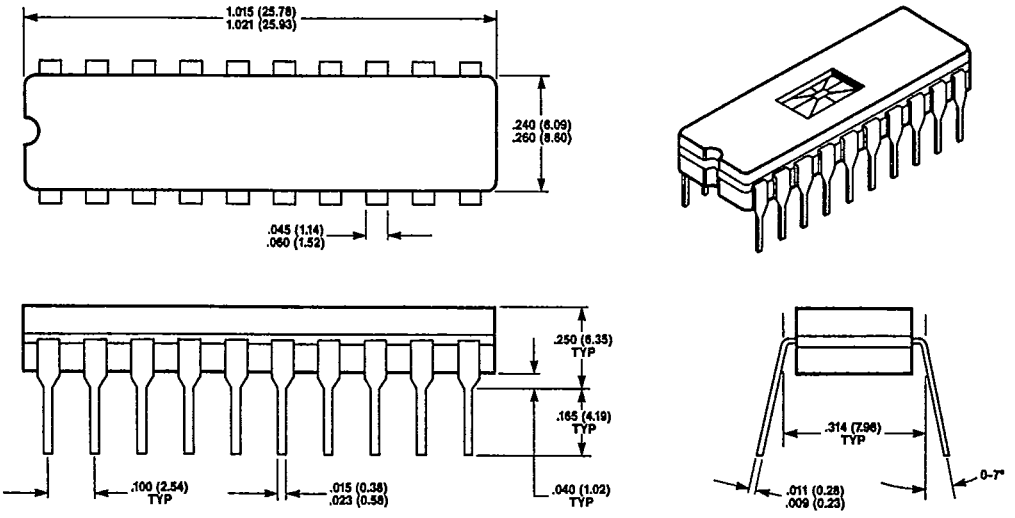
T-90-20

20 PIN PLASTIC DIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

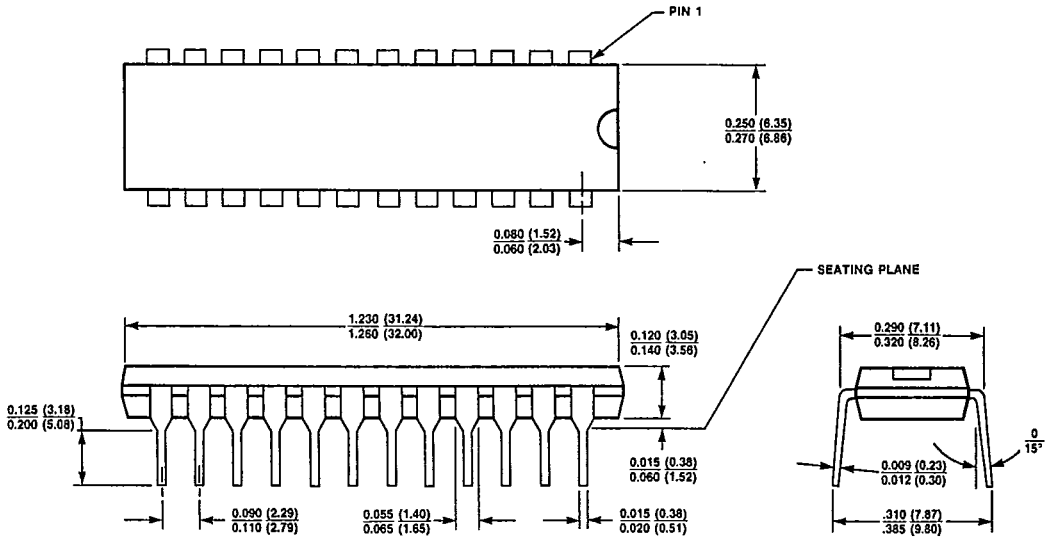
20 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

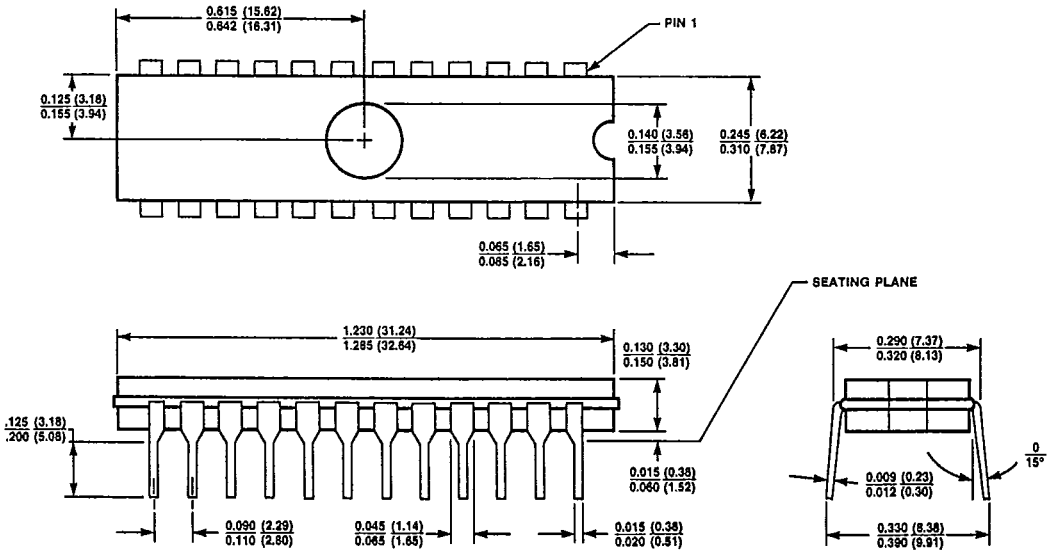
7

24 PIN PLASTIC DIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

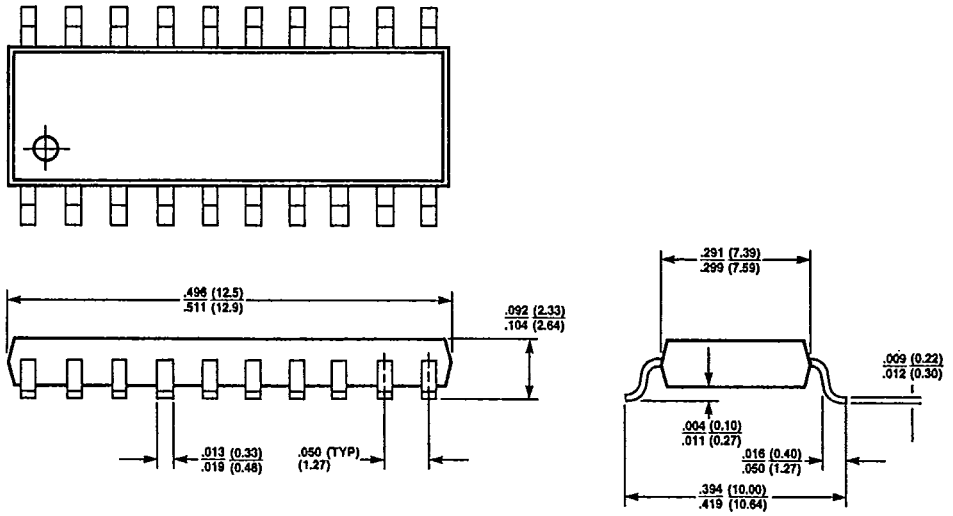
24 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

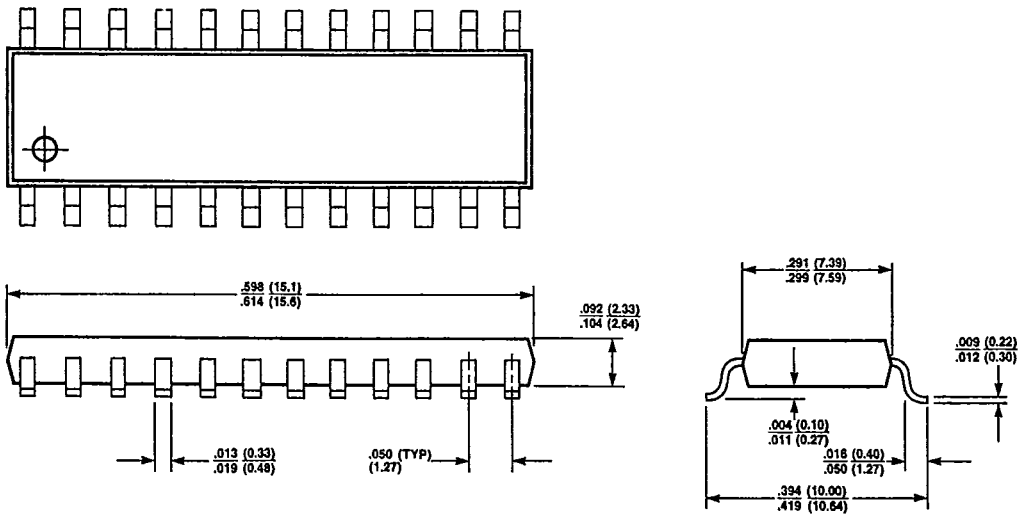
T-90-20

20 PIN SOIC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN SOIC

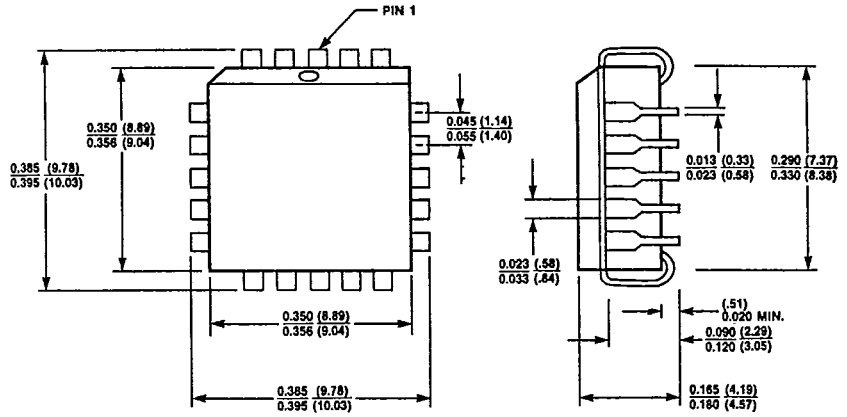


DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

7

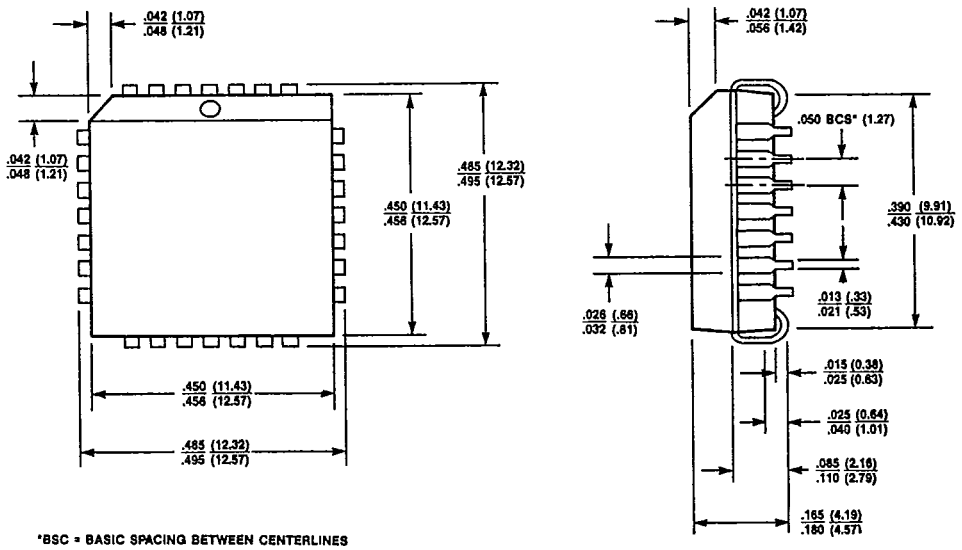
T-90-20

20 PIN PLCC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

28 PIN PLCC



*BSC = BASIC SPACING BETWEEN CENTERLINES

DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.