

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Added device type 04. -sld	99-04-02	K. A. Cottongim

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C											
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Steve L. Duncan	DEFENSE SUPPLY CENTER COLUMBUS																	
STANDARD MICROCIRCUIT DRAWING  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS  AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY Michael Jones	P. O. BOX 3990 COLUMBUS, OHIO 43216-5000																	
	APPROVED BY Kendall A. Cottongim	MICROCIRCUIT, HYBRID, MEMORY, STATIC RANDOM ACCESS MEMORY (SRAM) 256K x 16 BIT																	
	DRAWING APPROVAL DATE 97-12-23	SIZE A	CAGE CODE 67268	5962-96902															
	REVISION LEVEL C	SHEET 1 OF 23																	

DSCC FORM 2233  
APR 97

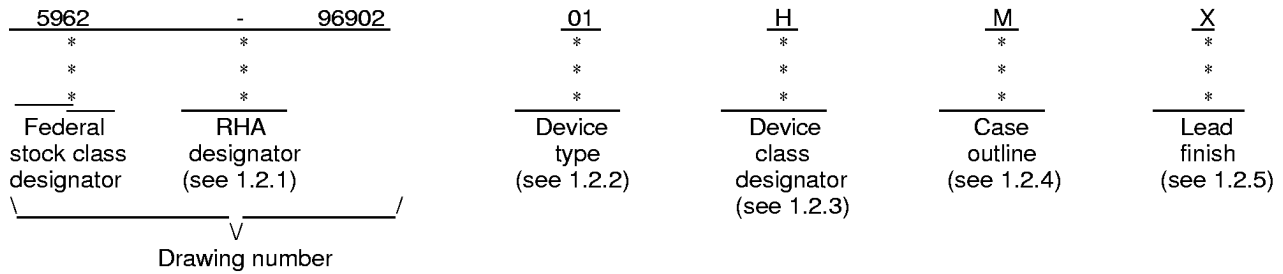
5962-E195-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, Class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access time</u>
01	WMS256K16-35DL	SRAM, 256K x 16-bit	35 ns
02	WMS256K16-25DL	SRAM, 256K x 16-bit	25 ns
03	WMS256K16-20DL	SRAM, 256K x 16-bit	20 ns
04	WMS256K16-17DL	SRAM, 256K x 16-bit	17 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device performance documentation</u>
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
M	See figure 1	44	Ceramic SOJ
N	See figure 1	44	Ceramic flat pack
T	See figure 1	44	Ceramic flat pack, lead formed

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

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DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL <b>C</b>	SHEET <b>2</b>

1.3 Absolute maximum ratings. <sup>1/</sup>

Supply voltage range (V <sub>CC</sub> ) .....	-0.5 V to +7.0 V
Input voltage range .....	-0.5 V to +7.0 V
Power Dissipation(P <sub>D</sub> ) .....	1.6 W
Storage temperature range .....	-65° C to +150° C
Lead temperature (soldering, 10 seconds).....	+300°C
Supply voltage range (V <sub>CC</sub> ) .....	-0.5 V to +7.0 V
Data retention.....	10 Years minimum
Endurance.....	10,000 cycles minimum

1.4 Recommended operating conditions.

Supply voltage range (V <sub>CC</sub> ) .....	+4.5 V dc to +5.5 V dc
Input low voltage range (V <sub>IL</sub> ) .....	-0.3 V dc to +0.8 V dc
Input high voltage range(V <sub>IH</sub> ).....	+2.2 V dc to V <sub>CC</sub> + 0.5 V dc
Output voltage, high minimum (V <sub>OH</sub> ).....	+2.4 V dc
Output voltage, low maximum (V <sub>OL</sub> ).....	-0.5 V to +7.0 V
Case operating temperature range (T <sub>C</sub> ).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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### 3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Output load circuit. The output load circuit shall be as specified in figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc, V <sub>SS</sub> = 0 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
DC Parameters							
Operating supply current	I <sub>CC</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH},$ f = 5 MHz, V <sub>CC</sub> = 5.5 V dc	1, 2, 3	All		275	mA
Standby current	I <sub>SB</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH},$ f = 5 MHz, V <sub>CC</sub> = 5.5 V dc	1, 2, 3	All		17	mA
Input leakage current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5 V dc, V <sub>IN</sub> = GND to V <sub>CC</sub>	1, 2, 3	All		10	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH},$ V <sub>OUT</sub> = GND to V <sub>CC</sub>	1, 2, 3	All		10	μA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = 4.5 V	1, 2, 3	All		0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA, V <sub>CC</sub> = 4.5 V	1, 2, 3	All	2.4		V
Dynamic characteristics							
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	4	All		20	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V, f = 1.0 MHz	4	All		20	pF
Data retention characteristics							
Data retention supply voltage	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2 V$	1, 2, 3	All	2.0	5.5	V
Data retention current	ICCDR1	V <sub>CC</sub> = 3.0 V	1, 2, 3	All		8.0	mA
See footnotes at end of table.							
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc, V <sub>SS</sub> = 0 V Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional testing							
Functional tests		See 4.3.1c	7, 8A, 8B	All			
Read cycle AC timing characteristics							
Read cycle time	t <sub>RC</sub>	See figure 4	9, 10, 11	01 02 03 04	35 25 20 17		ns
Address access time	t <sub>AA</sub>	See figure 4	9, 10, 11	01 02 03 04		35 25 20 17	ns
Output hold from address change	t <sub>OH</sub>	See figure 4	9, 10, 11	All	0		ns
Chip select access time	t <sub>ACS</sub>	See figure 4	9, 10, 11	01 02 03 04		35 25 20 17	ns
Output enable to output valid	t <sub>OE</sub>	See figure 4	9, 10, 11	01 02 03 04		20 15 12 10	ns
Chip select to output enable in low Z <u>2/</u>	t <sub>CLZ</sub>	See figure 4	9, 10, 11	01,02,03 04	5 2		ns
Output enable to output in low Z <u>2/</u>	t <sub>OLZ</sub>	See figure 4	9, 10, 11	All	0		ns
See footnotes at end of table.							
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc, V <sub>SS</sub> = 0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics – Continued.							
Chip enable to output in high Z <u>2/</u>	t <sub>CHZ</sub>	See figure 4	9, 10, 11	01 02 03 04		15 12 10 9	ns
Output enable to output in high Z <u>2/</u>	t <sub>OHZ</sub>	See figure 4	9, 10, 11	01 02 03 04		15 12 10 9	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ , access time	t <sub>BA</sub>	See figure 4	9, 10, 11	01 02 03 04		17 14 12 10	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ , enable to low Z output <u>2/</u>	t <sub>BLZ</sub>	See figure 4	9, 10, 11	All	0		ns
$\overline{\text{LB}}, \overline{\text{UB}}$ , disable to high Z output <u>2/</u>	t <sub>BHZ</sub>	See figure 4	9, 10, 11	01 02 03 04		15 12 10 9	ns
Write cycle AC timing characteristics							
Write cycle time	t <sub>WC</sub>	See figure 5	9, 10, 11	01 02 03 04	35 25 20 17		ns
Chip select to end of write	t <sub>CW</sub>	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns
See footnotes at end of table.							
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V dc ≤ V <sub>CC</sub> ≤ 5.5 V dc, V <sub>SS</sub> = 0 V Unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Address valid to end of write	t <sub>AW</sub>	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns
Data valid to end of write	t <sub>DW</sub>	See figure 5	9, 10, 11	01 02 03 04	20 15 12 10		ns
Write pulse width	t <sub>WP</sub>	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns
Address setup time	t <sub>AS</sub>	See figure 5	9, 10, 11	All	0		ns
Address hold time	t <sub>AH</sub>	See figure 5	9, 10, 11	All	2		ns
Output active from end of write	t <sub>OW</sub>	See figure 5	9, 10, 11	All	0		ns
Write enable to output in high Z <sup>2/</sup>	t <sub>WHZ</sub>	See figure 5	9, 10, 11	01 02 03 04		15 10 10 9	ns
Data hold time	t <sub>DH</sub>	See figure 5	9, 10, 11	All	0		ns
$\overline{LB}$ , $\overline{UB}$ , valid to end of write	t <sub>BW</sub>	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns

<sup>1/</sup> Unless otherwise specified, the DC test conditions are as follows:  
 Input pulse levels; V<sub>IH</sub> = V<sub>CC</sub> - 0.3 V and V<sub>IL</sub> = 0.3 V.  
 Unless otherwise specified, the AC test conditions are as follows:  
 Input pulse levels; V<sub>IH</sub> = 3.0 V and V<sub>IL</sub> = 0.0 V.  
 Input rise and fall times; 5 ns.  
 Input to output timing reference levels; 1.5 V.

<sup>2/</sup> Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

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Case outline M.

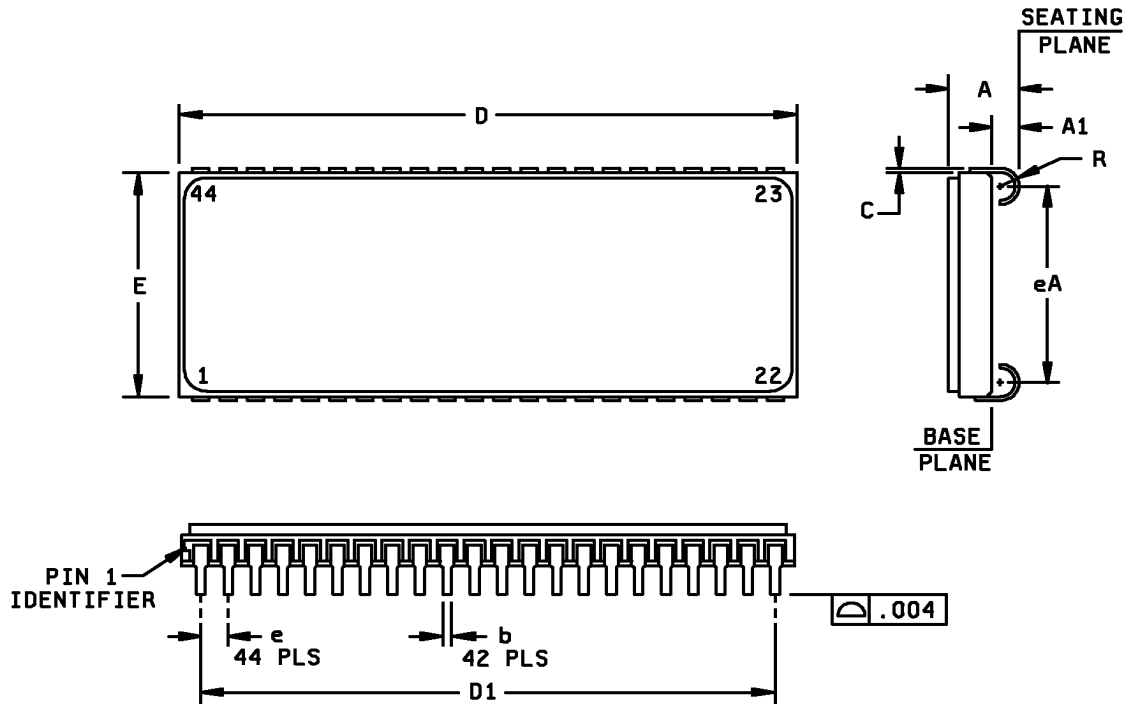


FIGURE 1. Case outline(s).

<p>STANDARD MICROCIRCUIT DRAWING</p>	<p>SIZE <b>A</b></p>		<p>5962-96902</p>
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Case outline M - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.69	3.96	.106	.156
A1	1.01	1.52	.040	.060
b	0.38	0.48	.015	.019
C	0.15	0.25	.006	.010
D	28.44	28.95	1.120	1.140
D1	26.54	26.79	1.045	1.055
E	10.79	11.04	.425	.435
e	1.27 TYP		.050 TYP	
eA	9.29	9.80	.366	.386
R	0.88 TYP		.035 TYP	

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Case outline N.

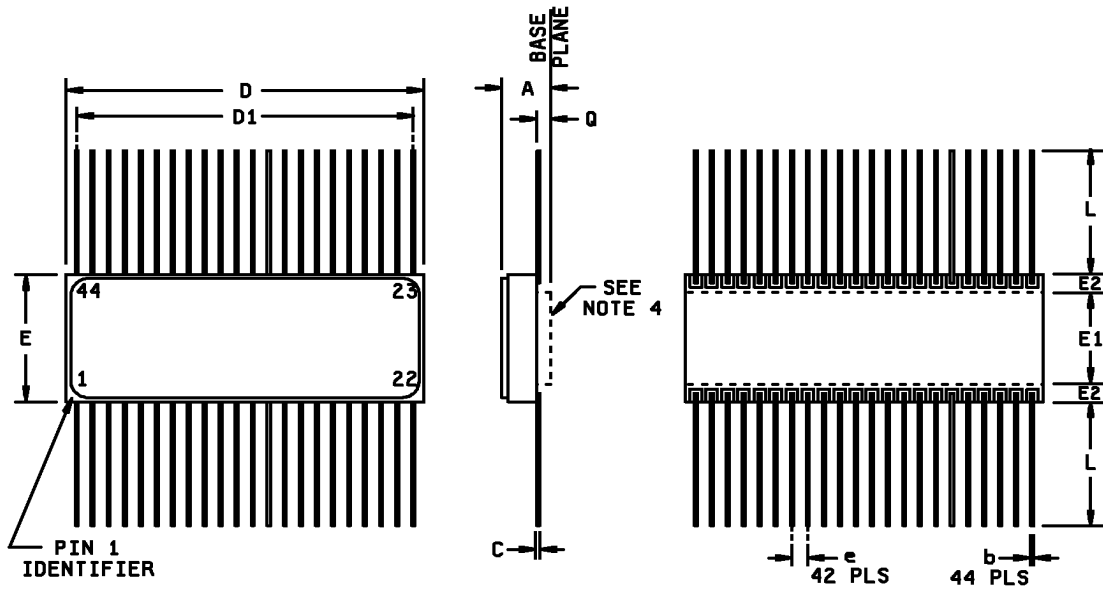


FIGURE 1. Case outline(s) - Continued.

<p>STANDARD MICROCIRCUIT DRAWING</p>	<p>SIZE <b>A</b></p>		<p>5962-96902</p>
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Case outline N - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.31	3.18	.091	.125
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
D	28.19	28.70	1.110	1.130
D1	26.54	26.80	1.045	1.055
E	12.83	13.80	.505	.515
E1	9.78	10.03	.385	.395
E2	1.52 TYP		.060 TYP	
e	1.27 TYP		.050 TYP	
L	9.65	10.67	.380	.420
Q	0.56	0.71	.022	.028

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline N is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline N.

FIGURE 1. Case outline(s) - Continued.

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Case outline T.

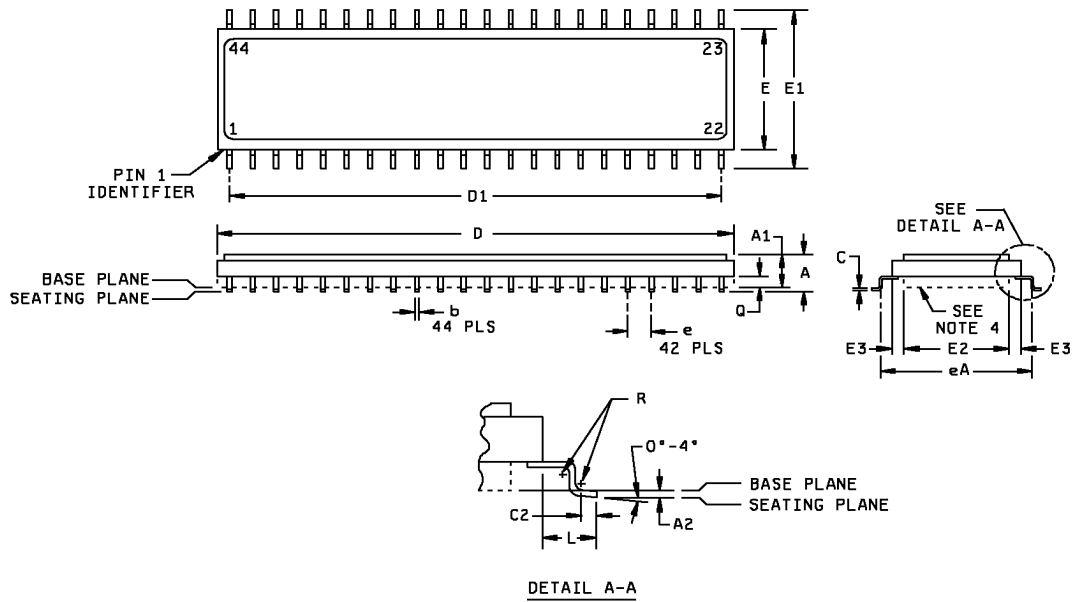


FIGURE 1. Case outline(s) - Continued.

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Case outline T - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.57	3.81	.101	.150
A1	2.31	3.18	.091	.125
A2	0.25	0.64	.010	.025
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
C2	0.76 TYP		.030 TYP	
D	28.19	28.70	1.110	1.130
D1	26.67 TYP		1.050 TYP	
E	12.83	13.08	.505	.515
E1	16.64	16.89	.655	.665
E2	9.78	10.03	.385	.395
E3	1.52 TYP		.060 TYP	
eA	11.07 TYP		.436 TYP	
e	1.27 TYP		.050 TYP	
L	1.91 TYP		.075 TYP	
Q	0.38	0.64	.015	.025
R	0.18 TYP		.007 TYP	

NOTES:

1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline T is available in either a pedestal or non-pedestal package. The Q dimension only applies to the Pedestal version of case outline T.

FIGURE 1. Case outline(s) - Continued.

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Device types	All	Device types	All
Case outlines	M, N, T	Case outlines	M, N, T
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	23	A10
2	A1	24	A11
3	A2	25	A12
4	A3	26	A13
5	A4	27	A14
6	$\overline{CS}$	28	NC
7	I/O1	29	I/O9
8	I/O2	30	I/O10
9	I/O3	31	I/O11
10	I/O4	32	I/O12
11	V <sub>CC</sub>	33	V <sub>CC</sub>
12	V <sub>SS</sub>	34	V <sub>SS</sub>
13	I/O5	35	I/O13
14	I/O6	36	I/O14
15	I/O7	37	I/O15
16	I/O8	38	I/O16
17	$\overline{WE}$	39	$\overline{LB}$
18	A5	40	$\overline{UB}$
19	A6	41	$\overline{OE}$
20	A7	42	A15
21	A8	43	A16
22	A9	44	A17

FIGURE 2. Terminal Connections.

STANDARD MICROCIRCUIT DRAWING  DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE <b>A</b>		5962-96902
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$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	Data I/O		Power
						I/O 1-8	I/O 9-16	
H	X	X	X	X	Not select	High Z	High Z	Standby
L	H	H	X	X	Output disable	High Z	High Z	Active
L	X	X	H	H	Output disable	High Z	High Z	Active
L	H	L	L	H	Read	Data out	High Z	Active
L	H	L	H	L		High Z	Data out	
L	H	L	L	L		Data out	Data out	
L	L	X	L	H	Write	Data in	High Z	Active
L	L	X	H	L		High Z	Data in	
L	L	X	L	L		Data in	Data in	

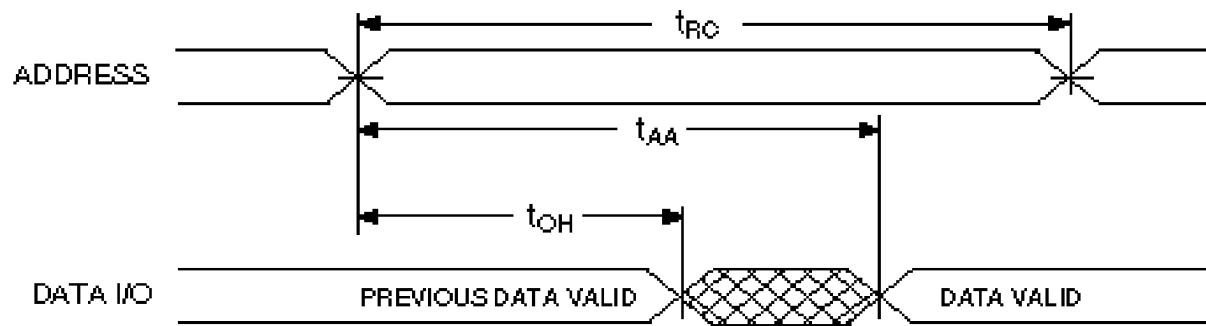
NOTES:

1. H =  $V_{IH}$  = High logic state.
2. L =  $V_{IL}$  = Low logic level.
3. X = Don't care (either high or low).
4. High Z = High impedance state.

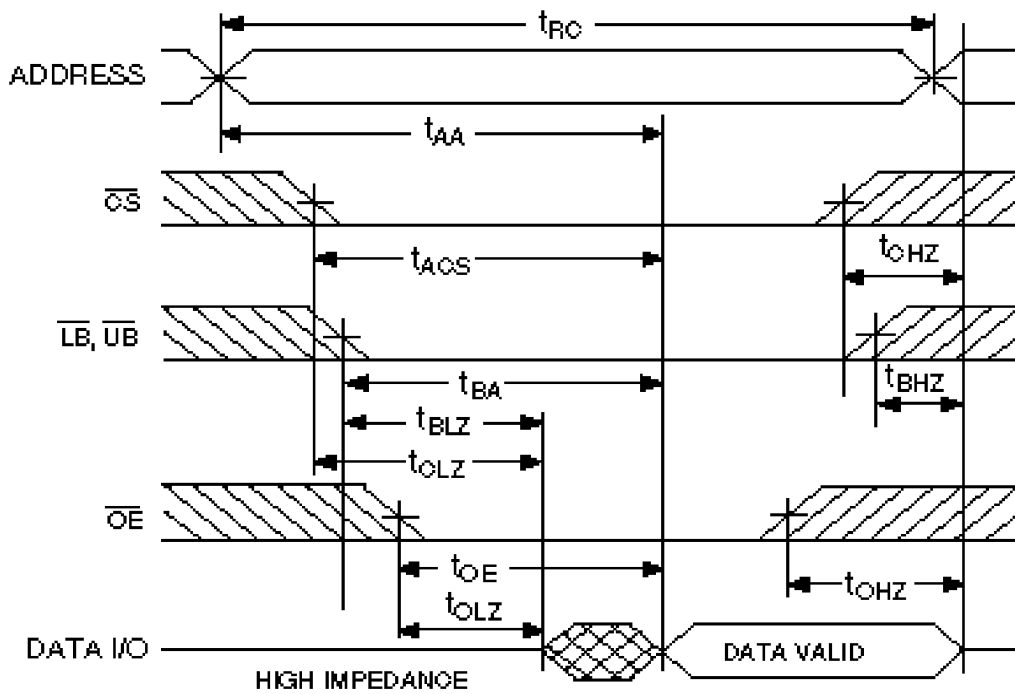
FIGURE 3. Truth table.

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READ CYCLE 1 ( $\overline{CS} = \overline{OE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



READ CYCLE 2 ( $\overline{WE} = V_{IH}$ )

FIGURE 4. Read cycle timing diagram.

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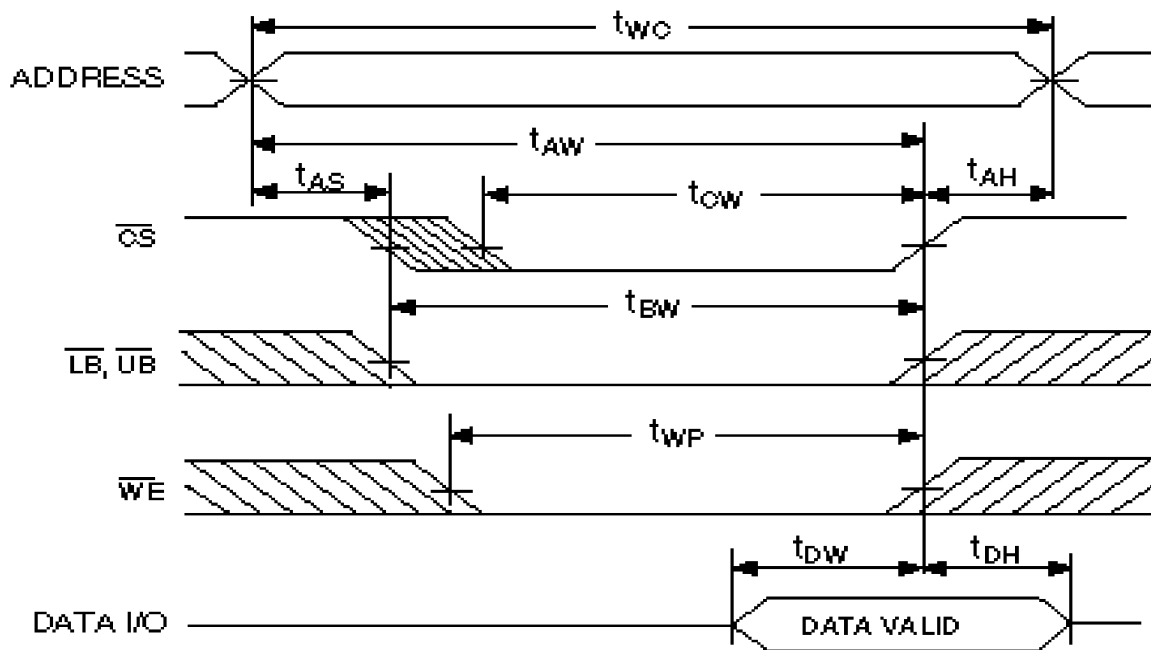
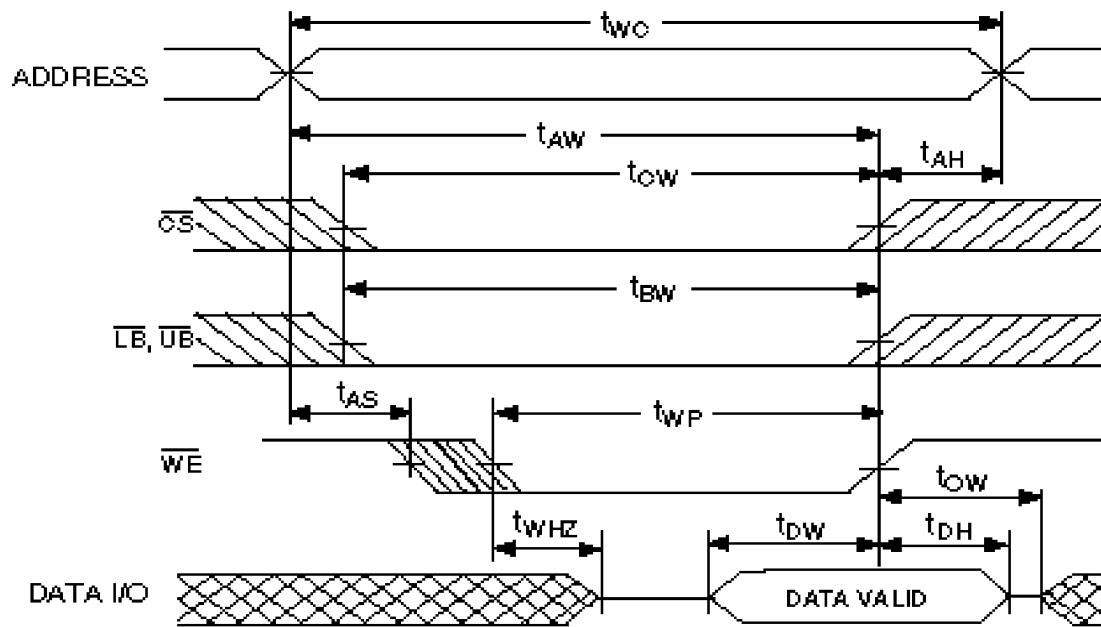
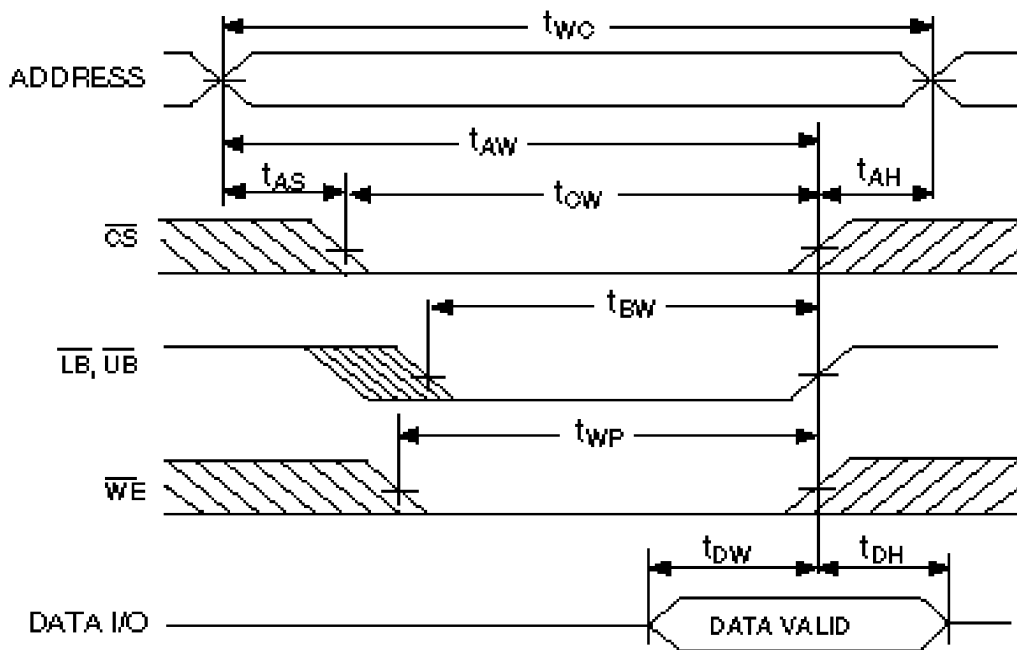


FIGURE 5. Write cycle timing diagram.

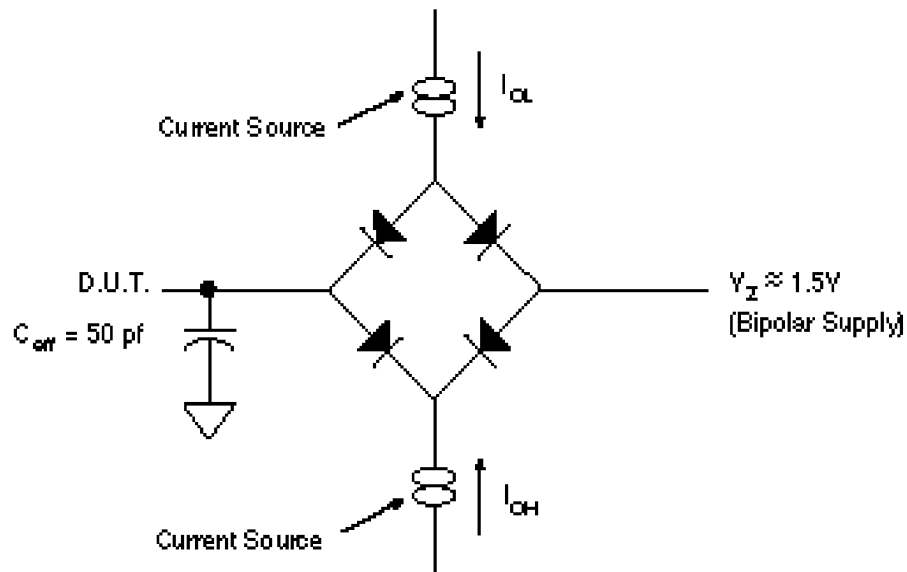
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WRITE CYCLE 3,  $\overline{LB}$ ,  $\overline{UB}$  CONTROLLED

FIGURE 5. Write cycle timing diagram - Continued.

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Parameter	Typical	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:

1.  $V_Z$  is programmable from -2 V to +7 V.
2.  $I_{OL}$  and  $I_{OH}$  programmable from 0 to 16 mA.
3. Tester impedance  $Z_0 = 75 \Omega$ .
4.  $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
5.  $I_{OL}$  and  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 6. Output load circuit

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1*,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical Parameters	1*,2,3,4,7,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

\* PDA applies to subgroup 1.

\*\* When applicable to this standard microcircuit drawing,  
the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

- (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- (2) T<sub>A</sub> as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 shall be omitted.
- c. Subgroups 7, 8A, and 8B shall include verification of the truth table of figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

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4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A$  as specified in accordance with table I of method 1005 of MIL-STD-883.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table II herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.
- d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5$  percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

<p style="text-align: center;">STANDARD MICROCIRCUIT DRAWING</p>	<p style="text-align: center;">SIZE A</p>		<p style="text-align: right;">5962-96902</p>
<p style="text-align: center;">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</p>		<p style="text-align: center;">REVISION LEVEL C</p>	<p style="text-align: right;">SHEET 23</p>

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-04-02

Approved sources of supply for SMD 5962-96902 are listed below for immediate acquisition information only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE Number	Vendor Similar PIN <u>2/</u>
5962-9690201HMA	54230	WMS256K16-35DLQ
5962-9690201HMC	54230	WMS256K16-35DLQ
5962-9690201HNA	54230	WMS256K16-35FLQ
5962-9690201HNC	54230	WMS256K16-35FLQ
5962-9690201HTA	54230	WMS256K16-35FGQ
5962-9690201HTC	54230	WMS256K16-35FGQ
5962-9690202HMA	54230	WMS256K16-25DLQ
5962-9690202HMC	54230	WMS256K16-25DLQ
5962-9690202HNA	54230	WMS256K16-25FLQ
5962-9690202HNC	54230	WMS256K16-25FLQ
5962-9690202HTA	54230	WMS256K16-25FGQ
5962-9690202HTC	54230	WMS256K16-25FGQ
5962-9690203HMA	54230	WMS256K16-20DLQ
5962-9690203HMC	54230	WMS256K16-20DLQ
5962-9690203HNA	54230	WMS256K16-20FLQ
5962-9690203HNC	54230	WMS256K16-20FLQ
5962-9690203HTA	54230	WMS256K16-20FGQ
5962-9690203HTC	54230	WMS256K16-20FGQ
5962-9690204HMA	54230	WMS256K16-17DLQ
5962-9690204HMC	54230	WMS256K16-17DLQ
5962-9690204HNA	54230	WMS256K16-17FLQ
5962-9690204HNC	54230	WMS256K16-17FLQ
5962-9690204HTA	54230	WMS256K16-17FGQ
5962-9690204HTC	54230	WMS256K16-17FGQ

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the manufacturer to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.



STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN - CONTINUED

DATE: 99-04-02

Approved sources of supply for SMD 5962-96902 are listed below for immediate acquisition information only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Vendor CAGE  
number

54230

Vendor name  
and address

White Electronic Designs Corporation  
3601 East University Drive  
Phoenix, AZ 85034

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.