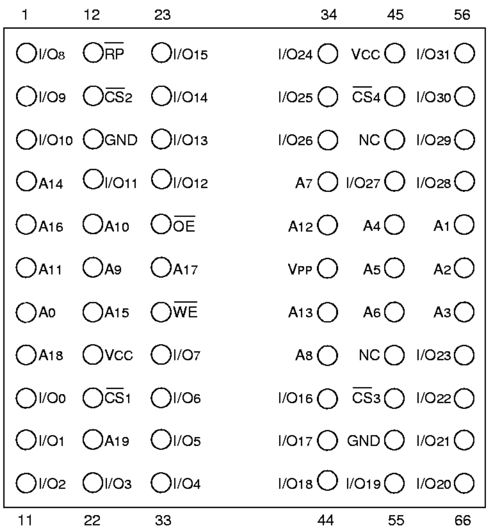
1Mx32 12V FLASH MODULE, SMD 5962-94613

FEATURES

- Access Times of 100, 150ns
- Packaging:
  - 66-pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402)
  - 68 lead, 40mm Low Profile CQFP, 3.5mm (0.140"), (Package 502)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Sector Architecture
  - 16 equal size sectors of 64KBytes per each 1024Kx8 chip
  - Two step sequence of erase ensures that memory contents are not accidently erased.
- 100,000 Erase/Program Cycles Minimum (0°C to 70°C)
- Organized as 1Mx32, user configurable as 2Mx16 or 4Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 12 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS, 3mA Standby Typical
- Automated Byte Write and Block Erase
  - Command User Interface
  - Status Register
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Microsoft Flash File System (FFS)
- Weight
  WF1M32-XG2X - 8 grams typical
  WF1M32-XH2X - 13 grams typical
  WF1M32-XG4TX - 20 grams typical

FIG. 1 PIN CONFIGURATION FOR WF1M32-XH2X, SMD 5962-94613

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RP}$	Reset/Powerdown
Vcc	Power Supply
VPP	Program/Erase Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

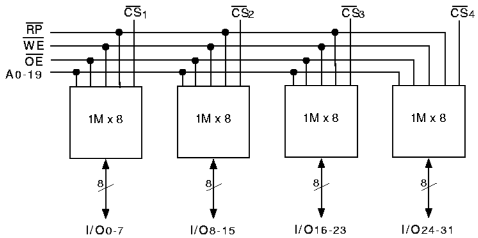
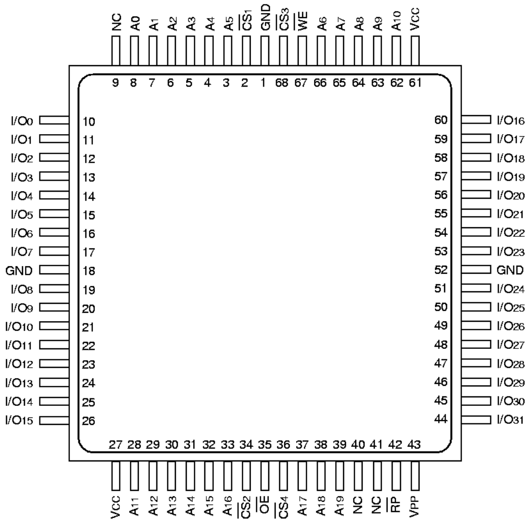


FIG. 2 PIN CONFIGURATION FOR WF1M32C-XG4TX, SMD 5962-94613

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE	Write Enable
CS1-4	Chip Selects
OE	Output Enable
RP	Reset/Powerdown
Vcc	Power Supply
GND	Ground
VPP	Program/Erase Supply
NC	Not Connected

BLOCK DIAGRAM

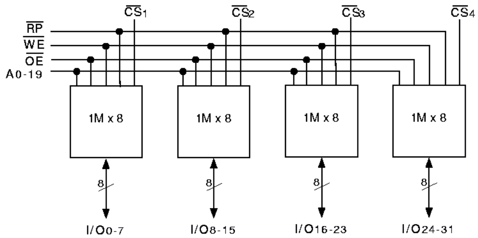
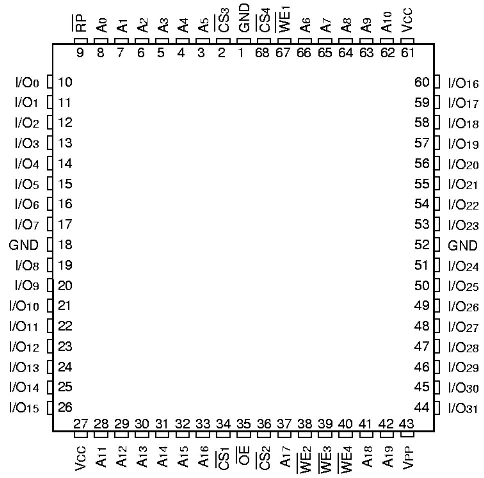
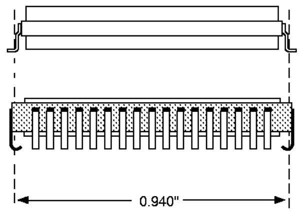


FIG. 3 **PIN CONFIGURATION FOR WF1M32-XG2X, Package Under Development**

TOP VIEW



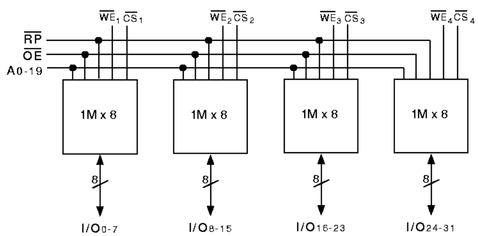


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-19	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
RP	Reset/Powerdown
Vcc	Power Supply
VPP	Program/Erase Supply
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on Anny Pin with Respect to GND (except Vcc and VPP)	-2.0 to +7.0	V
VPP Program Voltage with Respect to GND during Block Erase/Byte Write	-2.0 to +14.0	V
Vcc Supply Voltage with Respect to GND	-2.0 to +7.0	V
Output Short Circuit Current	100	mA

NOTES:

1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is Vcc + 0.5V which, during transitions, may overshoot to Vcc + 2.0V for periods <20 ns.
2. Maximum DC voltage on VPP may overshoot to +14.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a Stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

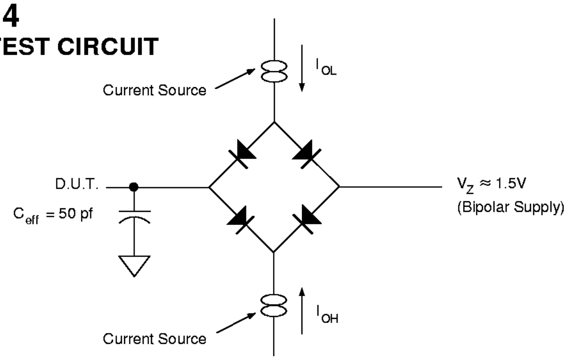
CAPACITANCE

(T_A = +25° C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			50	
CQFP G4			50	
CQFP G2			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = V_{CC} to GND			10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{OUT} = V_{CC} to GND			10	µA
V_{CC} Standby Current (4)	I_{CCS}	V_{CC} = 5.5, $\overline{CS}$ = $\overline{RP}$ = V_{IH}, f = 5MHz		3.0	10.0	mA
V_{CC} Read Current	I_{CCR}	V_{CC} = 5.5, $\overline{CS}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0mA		80	180	mA
V_{CC} Byte Write Current	I_{CCW}	Byte Write in Progress, V_{PP} = V_{PPH} = 12.6V		30	160	mA
V_{CC} Block Erase Current	I_{CCE}	Block Erase in Progress, V_{PP} = V_{PPH} = 12.6V		30	160	mA
V_{CC} Powerdown Current (4)	I_{CCD}	$\overline{RP}$ = GND I_{OUT}		8.0	200	µA
V_{PP} Standby Current	I_{PPS}	V_{PP} < V_{CC}		4	100	µA
V_{PP} Deep Powerdown Current (4)	I_{PPD}	$\overline{RP}$ = GND		8	200	µA
V_{PP} Write Current	I_{PPW}	V_{PP} = V_{PPH} = 12.6V, Byte Write in Progress		40	200	mA
V_{PP} Block Erase Current	I_{PPE}	V_{PP} = V_{PPH} = 12.6V, Block Erase in Progress		40	200	mA
Output Low Voltage (4)	V_{OL}	V_{CC} = 4.5, I_{OL} = 5.8 mA			0.45	V
Output High Voltage (4)	V_{OH}	V_{CC} = 4.5, I_{OH} = -2.5 mA	2.4			V
V_{PP} during Normal Operations (3)	V_{PPL}		0.0		6.5	V
V_{PP} during Erase/Write Operations	V_{PPH}		11.4	12.0	12.6	V
V_{CC} Erase/Write Lock Voltage	V_{LKO}		2.0			V

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. Valid for all speeds.
2. I_{CCES} is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block Erases/Byte Writes are inhibited when V_{PP} = V_{PPL} and not guaranteed in the range between V_{PPH} and V_{PPL}.
4. $\overline{RP}$ is not available in WF1M32E-XHX.
5. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-100 Min	-100 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	100		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	10		10		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	40		40		ns
V_{PP} Setup Time (1)	t_{VPWH}	t_{VPS}	100		100		ns
Address Setup Time	t_{AVWH}	t_{AS}	40		40		ns
Data Setup Time	t_{DVWH}	t_{DS}	40		40		ns
Data Hold Time	t_{WHDX}	t_{DH}	5		5		ns
Address Hold Time	t_{WHAX}	t_{AH}	5		5		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	10		10		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		ns
Duration of Byte Write Operation (1,2,3)	t_{WHQV1}		6		6		µs
Duration of Block Erase Operation (1,2,3)	t_{WHQV2}		0.3		0.3		sec
Write Recovery before Read	t_{WHGL}		0		0		µs
$\overline{RP}$ High Recovery Time (4)	t_{PHWL}	t_{PS}	1.0		1.0		µs

NOTES:
1. Guaranteed by design, not tested.
2. The on-chip Write State Machine incorporates all byte write and block erase functions and overhead of the flash memory, this includes byte program and verify, block precondition and veify, erase and verify.
3. Byte write and block erase durations are measured to completion (SR. 7 = 1). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).
4. $\overline{RP}$ is not available in WF1M32E-XHX.

AC CHARACTERISTICS – WRITE OPERATION - $\overline{CS}$ CONTROLLED [1]

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-100 Min	-100 Max	-150 Min	-150 Max	Unit
Write Enable Cycle Time	t_{AVAV}	t_{WC}	100		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	60		60		ns
V_{PP} Setup Time (1)	t_{VPEH}	t_{VPS}	100		100		ns
Address Setup Time	t_{AVEH}	t_{AS}	40		40		ns
Data Setup Time	t_{DVEH}	t_{DS}	40		40		ns
Data Hold Time	t_{EHDX}	t_{DH}	5		5		ns
Address Hold Time	t_{EHAX}	t_{AH}	5		5		ns
Write Enable Hold Time	t_{EHWH}	t_{WH}	0		0		ns
Chip Select Pulse Width High	t_{EHEL}	t_{EPH}	30		30		ns
Duration of Byte Write Operation (3)	t_{EHQV1}		6		6		µs
Duration of Block Erase Operation (3)	t_{EHQV2}		0.3		0.3		sec
Write Recovery before Read	t_{EHGL}		0		0		µs
$\overline{RP}$ High Recovery to $\overline{CS}$ Low (4)	t_{PHEL}	t_{PS}	1		1		µs

NOTES:
1. Chip-Select Controlled Writes: Write operations are driven by the valid combination of $\overline{CS}$ and $\overline{WE}$. In systems where $\overline{CS}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CS}$ waveform.
2. Guaranteed by design, not tested.
3. Byte write and block erase durations are measured to completion (SR7 = 1, V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR3/4/5 = 0).
4. $\overline{RP}$ available in WF1M32C-XG4X only.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-100 Min	-100 Max	-150 Min	-150 Max	Unit
Read Cycle Time	t_{AVAV}	t_{RC}	100		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		150	ns
Chip Select to Output Valid (1)	t_{ELQV}	t_{CE}		100		150	ns
Output Enable to Output Valid (1)	t_{GLQV}	t_{OE}		50		70	ns
Chip Select to Output Low Z (2)	t_{ELQX}	t_{LZ}	0		0		ns
Chip Select High to Output High Z (2)	t_{EHQZ}	t_{HZ}		65		65	ns
Output Enable to Output Low Z (2)	t_{GLQX}	t_{OLZ}	0		0		ns
Reset to Output Valid (3)	t_{PHQV}	t_{PWH}		400		400	ns
Output EnableHigh to Output High Z (2)	t_{GHQZ}	t_{DF}		50		50	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, Whichever is First[2]		t_{OH}	0		0		ns

NOTES:
1. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{CE}.
2. Guaranteed by design, not tested.
3. $\overline{RP}$ is not available in WF1M32E-XHX.

FIG. 5 AC WAVEFORMS FOR WRITE-ERASE-PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

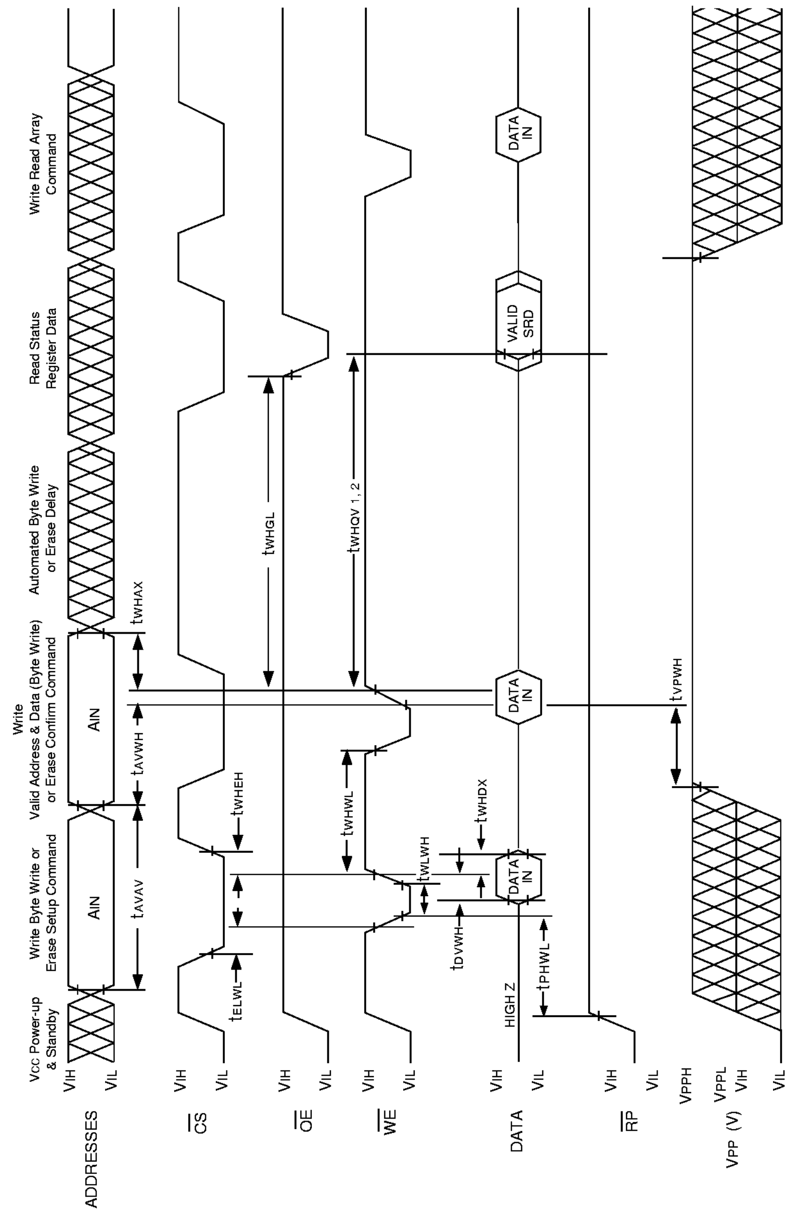


FIG. 6 ALTERNATE AC WAVEFORM FOR WRITE OPERATIONS - $\overline{CS}$ CONTROLLED

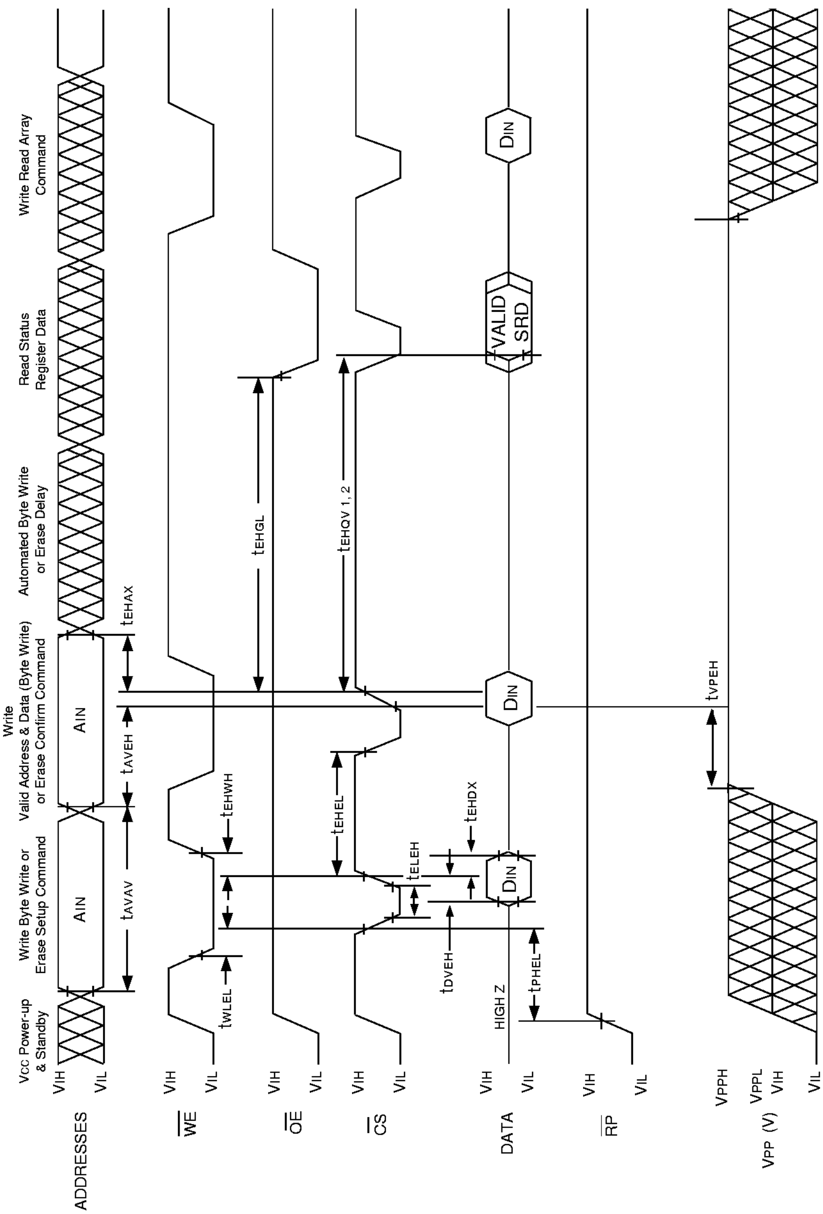
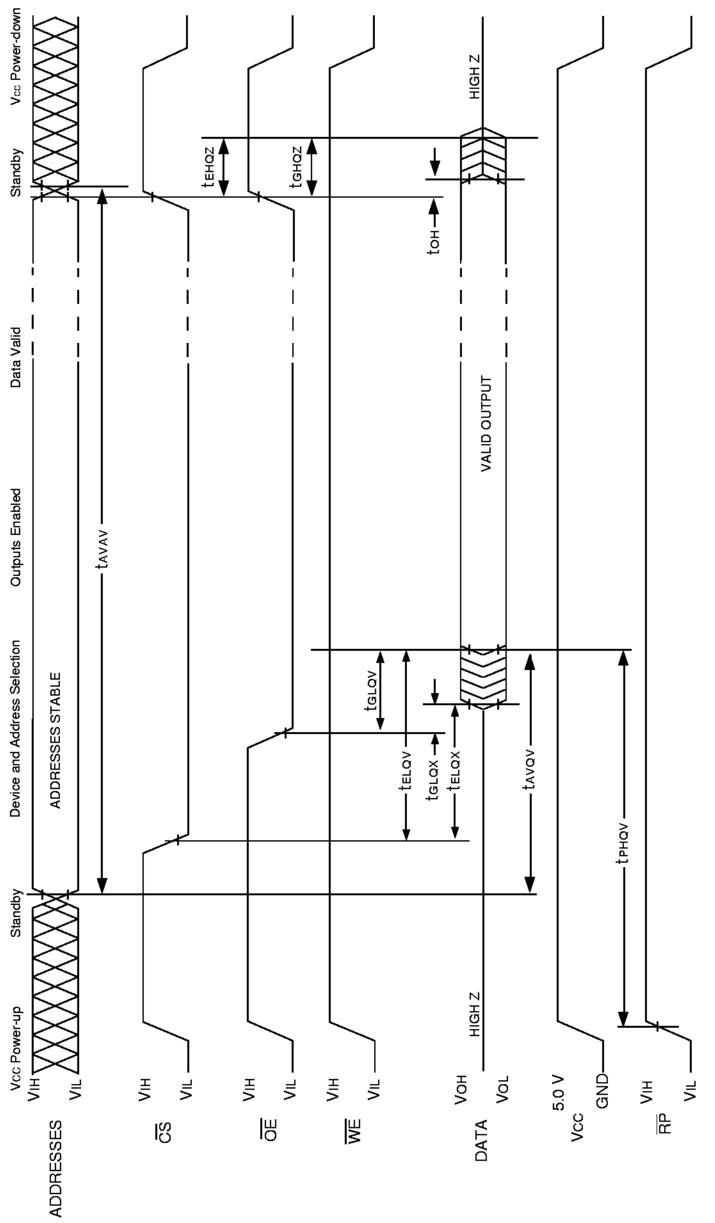


FIG. 7 AC WAVEFORM FOR READ OPERATIONS



PRINCIPLES OF OPERATION

The following Principles of Operation of the WF1M32-XXX MCM is applicable to each of the four memory chips inside the MCM. Chip 1 is distinguished by $\overline{CS_1}$ and I/O0-7, Chip 2 by $\overline{CS_2}$ and I/O8-15, Chip 3 by $\overline{CS_3}$ and I/O16-23, and Chip 4 by $\overline{CS_4}$ and I/O24-31.

The WF1M32-XXX includes write automation to manage write and erase functions. The Write State Machine allows for 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with RAM-like interface timings.

After initial device powerup the WF1M32-XXX functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. The status register can also be accessed through the command user interface when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables successful block erasure and byte writing of the device. Functions associated with altering memory contents—byte write, block erase—are accessed via the command user interface and verified thru the status register.

Commands are written using standard microprocessor write timings. Command user interface contents serve as input to the write status machine, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the device are again possible via the read array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

COMMAND USER INTERFACE AND WRITE AUTOMATION

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the Status Register on each of the four memory chips in the MCM. Byte write is similarly controlled, after destination address and expected data are supplied.

DATA PROTECTION

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. Additionally, all functions are disabled whenever V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The two-step byte write/block erase command user interface write sequence provides additional software write protection.

BUS OPERATION

Flash memory reads, erase and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

The WF1M32-XXX can be read from any of its blocks, and information can be read from the status register of each chip selected. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate read mode command to the command user interface. The device automatically resets to read array mode upon initial device powerup or after exit from deep powerdown. Chip select $\overline{CS}$ is the device selection control, and when active enables the selected memory device. Output Enable ($\overline{OE}$) is the data input/output (I/O0-I/O31) direction control, and when active drives data from the select memory onto the I/O bus. $\overline{RP}$ and $\overline{WE}$ must also be at V_{IH}. Figure 7 illustrates read bus cycle waveforms.

OUTPUT DISABLE

With $\overline{OE}$ at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (I/O0-31) are placed in a high-impedance state.

STANDBY

$\overline{CS}$ at a logic-high level (V_{IH}) places the device in a standby mode. Standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (I/O0-31) are placed in a high-impedance state independent of the status of $\overline{OE}$. If the device is deselected during block erase or byte write, it will continue functioning and consuming normal active power until the operation is completed.

WRITE

Writes to the command user interface enable reading of device data. They also control inspection and cleaning of the status register. Additionally, when $V_{PP} = V_{PPH}$, the command user interface controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.

The command user interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase setup and erase confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The command user interface is written by bringing $\overline{WE}$ to a logic-low level (V_{IL}) while $\overline{CS}$ is low. Address and data are latched on the rising edge of $\overline{WE}$. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operation, Figures 5 and 6, for specific timing parameters.

COMMAND DEFINITIONS

When V_{PPL} is applied to the V_{PP} pin of the chip selected, read operations from the status register, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the command user interface of the chip selected. Table 2 defines the WF1M32-XXX commands.

READ ARRAY COMMAND

Upon initial device powerup the device defaults to Read Array mode. This operation is also initiated by writing FFH into the command user interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command user interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

TABLE 1 - BUS OPERATIONS

Mode	$\overline{RP}$	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	VPP	I/O0-31
Read (1,2,4)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Output Disable (4)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High Z
Standby (4)	V_{IH}	V_{IH}	X	X	X	High Z
Deep Powerdown	V_{IL}	X	X	X	X	High Z
Write (3,4)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. X can be V_{IL} or V_{IH} for control pins and V_{PPL} or V_{PPH} for V_{PP}. See DC Characteristics for V_{PPL} and V_{PPH} voltages.
3. Command writes involving block erase or byte write are only successfully executed when $V_{PP} = V_{PPH}$.
4. $\overline{RP}$ is not available in WF1M32E-XHX.

TABLE 2 - COMMAND DEFINITIONS

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array/Reset	1	Write	X	FFH			
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H			
Erase Setup/Erase Confirm	2	Write	BA[1]	20H	Write	BA[1]	D0H
Erase Suspend/Erase Resume	2	Write	X	B0H	Write	X	D0H
Byte Write Setup/Write	2	Write	WA[1]	40H[3]	Write	WA[1]	WD[2]
Alternate Byte Write Setup/Write	2	Write	WA[1]	10H[3]	Write	WA[1]	WD[2]

NOTES:
1. BA = Address within the block being erased. WA = Address of memory location to be written.
2. SRD = Data read from status register. See Table 3 for a description of the status register bits. WD = Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$.
3. Either 40H or 10H are recognized by the WSM as the Byte Write Setup command.

TABLE 3
STATUS REGISTER DEFINITIONS

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy
SR.6 = ERASE SUSPENDED STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed
SR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase
SR.4 = BYTE WRITE STATUS
1 = Error in Byte Write
0 = Successful Byte Write
SR.3 = VPP STATUS
1 = VPP Low Detect; Operation Abort
0 = VPP OK
SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use and should be masked out when polling the status register.

NOTES:

The Write State Machine Status bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success.

If the Byte Write and Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.

If V_{PP} low status is detected, the status register must be cleared before another byte write or block erase operation is attempted.

The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

READ STATUS REGISTER COMMAND

Each chip of the WF1M32-XXX contains a status register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the read status register command (70H) to the command user interface. After writing this command, all subsequent read operations output data from the status register, until another valid command is written to the command user interface. The contents of the status register are latched on the falling edge of CE or CS, whichever occurs last in the read cycle. CE or CS must be toggled to V_{IH} before further reads to update the status register latch. The read status register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

CLEAR STATUS REGISTER COMMAND

The erase status and byte write status bits are set to "1"s by the Write State Machine on each chip and can only be reset by the clear status register command. These bits indicate various failure conditions (see Table 3). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The status register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

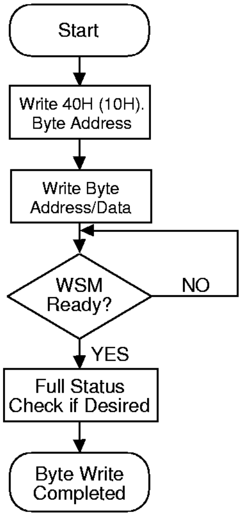
Additionally, the V_{PP} Status bit (SR3) of the chip selected MUST be reset by system software before further byte writes or block erases are attempted. To clear the status register, the clear status register command (50H) is written to the command user interface. The clear status register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

ERASE SETUP/ERASE CONFIRM COMMANDS

Erase is executed one block at a time, initiated by a two-cycle command sequence. An erase setup command (20H) is first written to the command user interface, followed by the Erase Confirm command (D0H). These commands require both appropriate sequencing and address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two command erase sequence is written to it, the WF1M32-XXX automatically outputs status register data when read (see Figure 9; Block Erase Algorithm). The CPU can detect the completion of the erase event by analyzing the output of the WSM Status bit of the status register.

FIG. 8

AUTOMATED BYTE WRITE ALGORITHM



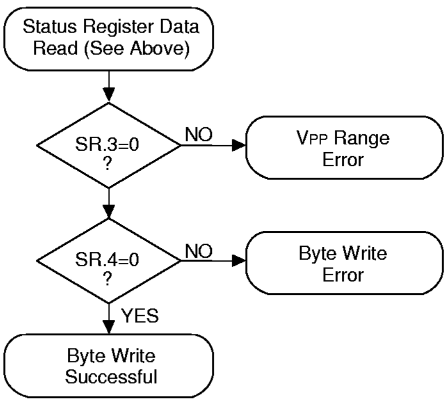
Bus Operation	Command	Comments
Write	Byte Write Setup	Data = 40H (10H) Address = Byte to be Written
Write	Byte Write	Data to be written Address = Byte to be Written
Standby/Read		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CS}$ to update Status Register

Repeat for subsequent bytes

Full status check can be done after each byte or after a sequence of bytes

Write FFH after the last byte write operation to reset the device to Ready Array Mode

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 Both 1 = Byte Write Error

SR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the clear status register command, in cases where multiple bytes are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

When erase is completed, the Erase Status bit should be checked. If erase error is detected, the status register should be cleared. The command user interface remains in read status register mode until further commands are issued to it.

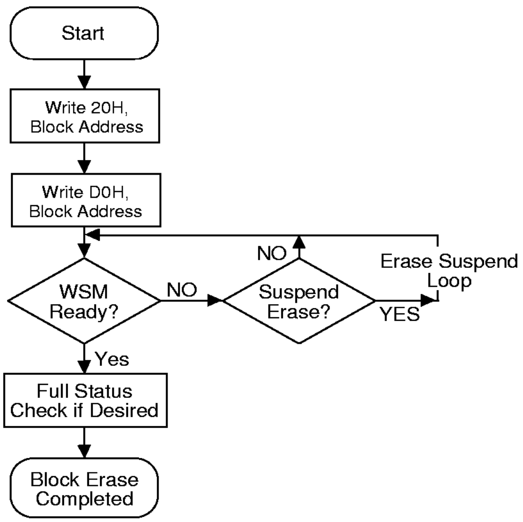
This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, reliable block ensure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

BYTE WRITE SETUP/WRITE COMMANDS

Byte write is executed by a two-command sequence. The byte write setup command (40H) is written to the command user interface of the chip selected, followed by a second write specifying the address and data (latched on the rising edge of $\overline{WE}$) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two-command byte write sequence is written to it, the device automatically outputs status register data when read (see Figure 8; Byte Write Algorithm). The CPU can detect the completion of the byte write event by analyzing the output of the WSM Status bit of the status register. Only the read status register command is valid while byte write is active.

When byte write is complete, the byte write status bit should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The command user interface remains in read status register mode until further commands are issued to it. If byte write is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Byte write attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

FIG. 9
AUTOMATED BLOCK ERASE ALGORITHM



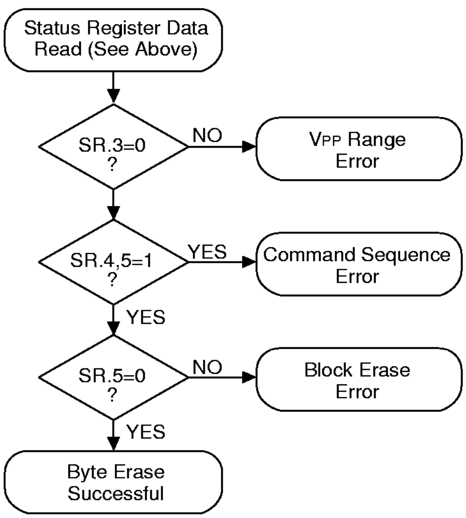
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Address = Within block to be erased
Write	Erase	Data = D0H Address = Within block to be erased
Standby/Read		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CS}$ to update Status Register

Repeat for subsequent bytes

Full status check can be done after each byte or after a sequence of bytes

Write FFH after the last byte write operation to reset the device to Ready Array Mode

FULL STATUS CHECK PROCEDURE



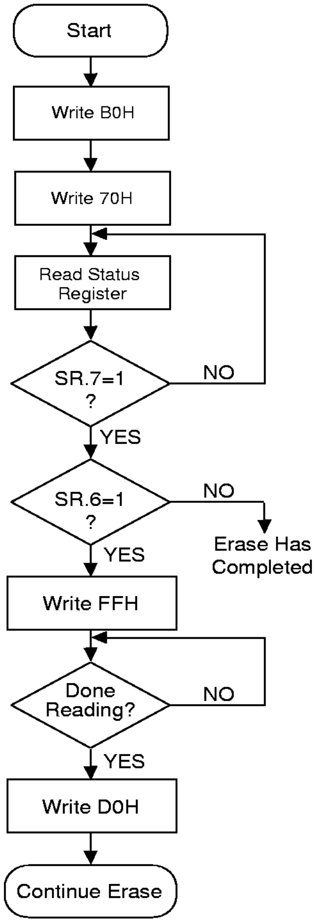
Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the clear status register command, in cases where multiple bytes are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

FIG. 10
ERASE SUSPEND/RESUME ALGORITHM



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H
Write	Read Status Register	Data=70H
Standby/Read		Check Read Status Register
		Check SR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CS}$ to update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

ERASE SUSPEND/ERASE RESUME COMMANDS

The erase suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the erase suspend command (B0H) to the command user interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The WF1M32-XXX continues to output status register data when read, after the erase suspend command is written to it. Polling the WSM status and erase suspend status bits will determine when the erase operation has been suspended (both will be set to "1").

At this point, a read array command can be written to the command user interface to read data from blocks other than that which is suspended. The only other valid commands at this time are read status register (70H) and erase resume (D0H), at which time the WSM will continue with the erase process. The erase suspend status and WSM status bits of the status register will be automatically cleared. After the erase resume command is written to it, the device automatically outputs status register data when read (see Figure 10). V_{PP} must remain at V_{PPH} while in erase suspend.

V_{CC}, V_{PP}, $\overline{RP}$ TRANSITIONS AND THE COMMAND/STATUS REGISTERS

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} Status bit of the Status Register (SR3) is set to "1", a Clear Status Register command MUST be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (SR4) or Erase (SR5) Status bits of the Status Register will be set to "1"s if error is detected. $\overline{RP}$ transitions to V_{IL} during byte write and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device poweroff, or $\overline{RP}$ transitions to V_{IL}, clear the Status Register to initial value 10000 for the upper 5 bits.

The Command User Interface latches commands as issued by system software and is not altered by V_{PP} or $\overline{CS}$ transitions or WSM actions. Its state upon powerup, after exit from deep powerdown or after V_{CC} transitions below V_{LKO}, is Read Array Mode.

After byte write or block erase is complete, even after V_{PP} transitions down to V_{PPL}, the Command User interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

NOTE: $\overline{RP}$ is not available in WF1M32E-XHX.

POWER UP/DOWN PROTECTION

The WF1M32-XXX is designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the device ensures that the Command User interface is reset to the Read Array mode on power up.

POWERDOWN AND RESET

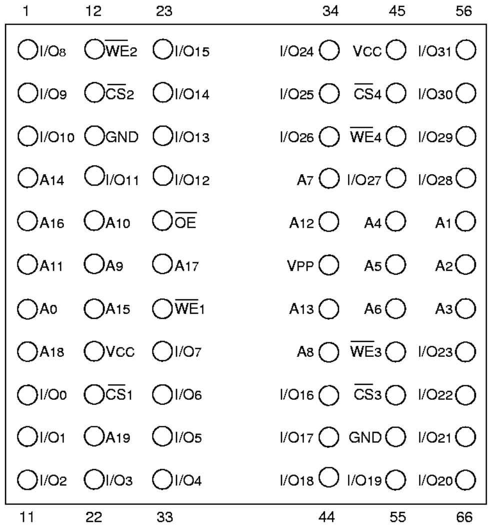
The WF1M32-XG4X offers a deep power-down feature, entered when $\overline{RP}$ is a V_{IL}. During read modes, $\overline{RP}$-low deselects the memory, places output drivers in a high-impedence state and turns off all internal circuits. The device requires time t_{PWH} (see AC Characeristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command User Interface is reset to Read Array, and the upper 5 bits of the Status Register are cleared to value 10000, upon return to normal operation.

During block erase or bytewrite modes. $\overline{RP}$ low will abort either operaton. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time t_{PS} after $\overline{RP}$ goes to logic-high (V_{IH}) is required before another command can be written.

This use of $\overline{RP}$ during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during write/erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur beause the flash memory would be providing the status information instead of array data. These flash memories allow proper CPU initialization following a system reset through the use of the $\overline{RP}$ input. In this application $\overline{RP}$ is controlled by the same $\overline{RESET}$ signal that resets the system CPU.

FIG. 10 PIN CONFIGURATION FOR WF1M32E-XH2X

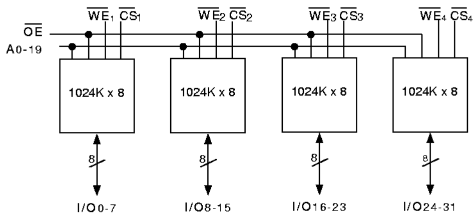
TOP VIEW



PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-19}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Program/Erase Supply
GND	Ground

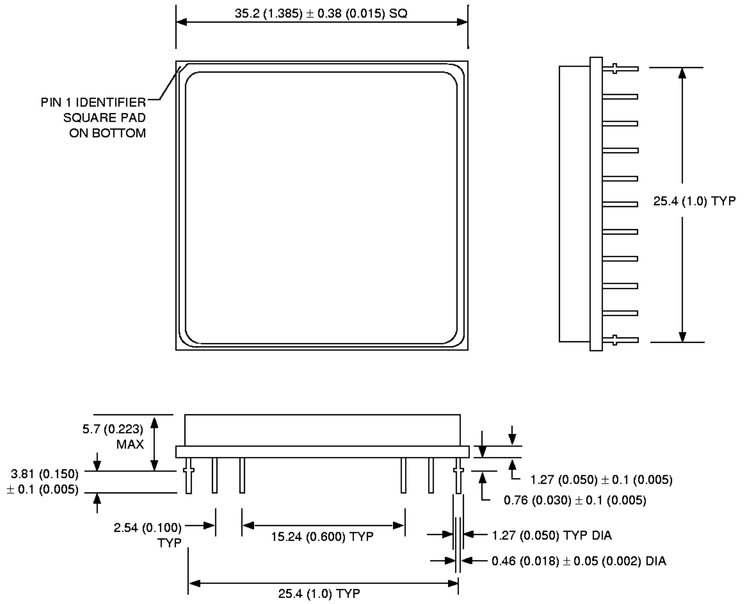
BLOCK DIAGRAM



PIN CONFIGURATION OPTIONS

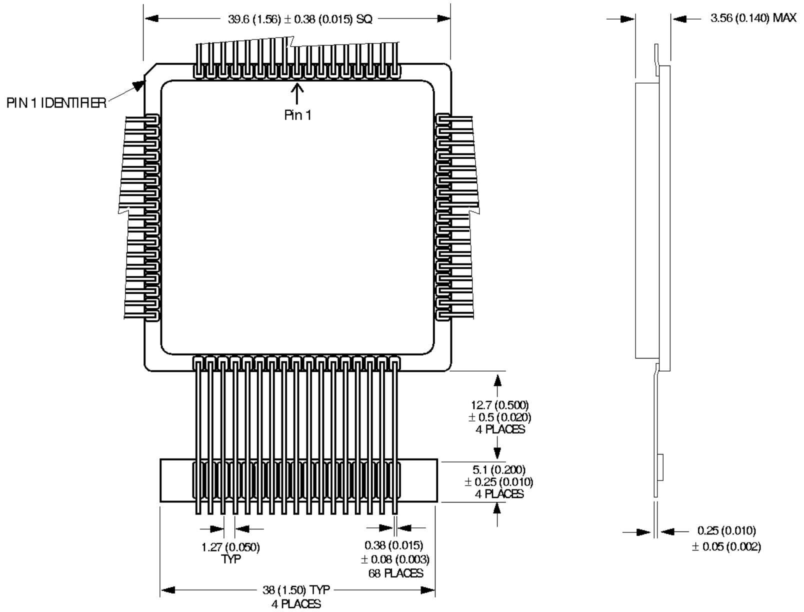
Package	Pin Configuration Option(s)	WM Part Number
HIP (PGA)	4 $\overline{CS}$, 1 $\overline{WE}$, $\overline{RP}$ (FIG. 1)	WF1M32-XH2X
	4 $\overline{CS}$, 4 $\overline{WE}$ (FIG. 10)	WF1M32E-XH2X
CQFP (G4)	4 $\overline{CS}$, 1 $\overline{WE}$, $\overline{RP}$ (FIG. 2)	WF1M32C-XG4X
Low Profile CQFP (G4T)	Upgradable to 2M x 32 and 4M x 32 in the same footprint	WF1M32C-XG4TX
CQFP (G2)	4 $\overline{CS}$, 4 $\overline{WE}$, $\overline{RP}$ (FIG. 3)	WF1M32-XG2X

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



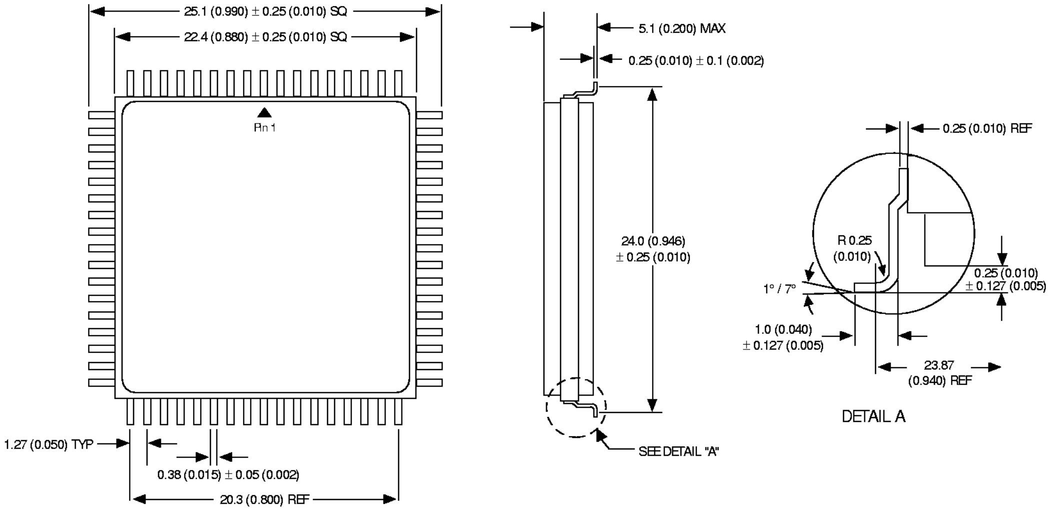
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

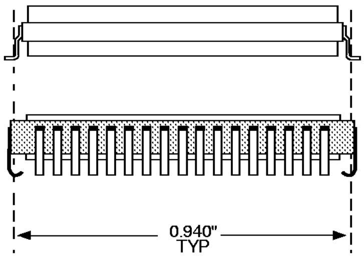
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)





The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 1M32 X - XXX X X X X

- **LEAD FINISH:**
  - Blank = Gold plated leads
  - A = Solder dip leads
- **V_{PP} PROGRAMMING VOLTAGE**
  - Blank = 12V
- **DEVICE GRADE:**
  - M = Military Screened -55°C to +125°C
  - I = Industrial -40°C to +85°C
  - C = Commercial 0 to +70°C
- **PACKAGE TYPE:**
  - H2 = Ceramic Hex In line Package, HIP (Package 402)
  - G2 = 22mm Ceramic Quad Flat Pack, CQFP (Package 500)
  - G4T = 40mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 502)
- **ACCESS TIME (ns)**
- **IMPROVEMENT MARK**
  - E = 4 Chip Selects and 4 Write Enables in HIP
  - C = 4 Chip Selects and 1 Write Enable in CQFP
- **ORGANIZATION, 1M x 32**
  - User configurable as 2M x 16 or 4M x 8
- **Flash PROM**
- **WHITE MICROELECTRONICS**

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
1M x 32 Flash	150ns	66 pin HIP (H2)	5962-94613 01HXX
1M x 32 Flash	100ns	66 pin HIP (H2)	5962-94613 02HXX
1M x 32 Flash	150ns	68 lead CQFP, Low Profile (G4T)	5962-94613 01HZX
1M x 32 Flash	100ns	68 lead CQFP, Low Profile (G4T)	5962-94613 02HZX