NEC

NEC Electronics Inc.

μPD41221
224,000-BIT
SERIAL-ACCESS NMOS RAM

December 1987

Description

The μPD41221 is a 224,000-bit, serial-access memory that uses the same technology as standard N-channel MOS dynamic RAMs. The dynamic circuit technology based on the one-transistor memory cell is combined with the double-polysilicon NMOS process technology.

The μPD41221 is well-suited for use as a field memory for television systems. The memory array, organized as 320 rows by 700 columns, is a size that can satisfy almost all requirements for NTSC and PAL. Memory operation is based on one horizontal scanning period (1H). A serial read or write operation is executed on a row within 1H.

The operation sequence within 1H is as follows.

(1) The row location is specified by $\overline{RCR}$ (reset to row 0), $\overline{INC}$ (+1 increment), or $\overline{DEC}$ (−1 decrement).

(2) A data transfer cycle (from the row to the data register) is selected by $\overline{RAS}$ active with $\overline{WE}$ high.

(3) SC causes a serial write or read operation between the data input/output and the data register from column 0 to any column location up to 699.

(4) $\overline{REF}$ (refresh control) executes internal automatic refresh asynchronously with serial operation.

(5) A data restore cycle (from the data register to the row selected) is selected by $\overline{RAS}$ active with $\overline{WE}$ low.

Address pins are eliminated because serial address functions are built into the chip. SYN, an open-drain output, is in the low-impedance state from the 605th $\overline{SC}$ cycle to the beginning of the data restore cycle, allowing system designers to generate a horizontal sync signal.

The μPD41221 data register stores memory data on one word line. A fast serial read or write is executed between the data input/output and the data register. During the serial operation, data refresh cycles for the memory array can be performed asynchronously.

Features

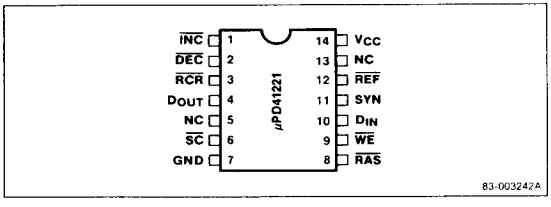
- ☐ 224,000 x 1-bit serial-access memory
- ☐ Screen size memory array suitable for NTSC and PAL
- ☐ +5-volt ±10% single power supply
- ☐ On-chip substrate bias generator
- ☐ Two key functional blocks
  - — 320-row by 700-column memory array
  - — 700-bit data register
- ☐ Full serial operation with line pointer control
- ☐ Variable serial cycle numbers up to column bit size
- ☐ Input data appears on data output in serial write cycle
- ☐ Dual (refresh/serial) operation
- ☐ Refresh cycle: 320 cycles/2 ms
- ☐ Power dissipation
  - — Active: 385 mW (max)
  - — Standby: 82.5 mW (max)
- ☐ All inputs TTL-compatible
- ☐ Three-state HCMOS-compatible output
- ☐ Output data caused by negative $\overline{SC}$ transition is maintained up to next $\overline{SC}$ or $\overline{RAS}$ negative transition

Ordering Information

Part Number	$\overline{SC}$ Cycle Time (min)	Read Access Time (max)	Package
μPD41221C-70	70 ns	55 ns	14-pin plastic DIP
C-90	90 ns	75 ns	

Pin Configuration

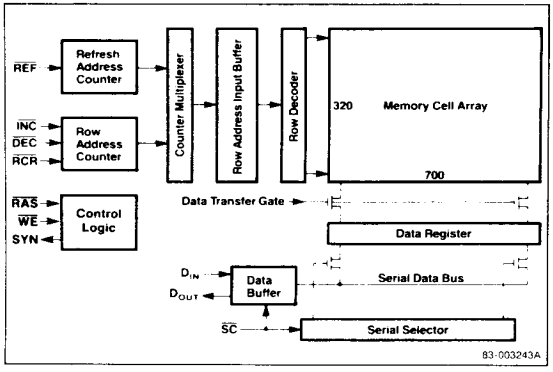
14-Pin Plastic DIP



Pin Identification

Symbol	Function
D_{IN}	Data in
D_{OUT}	Data out
$\overline{INC}$	Row counter increment
$\overline{DEC}$	Row counter decrement
$\overline{RCR}$	Row counter reset
SC	Serial control
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
SYN	Sync acknowledge
$\overline{REF}$	Refresh control
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Supply voltage on V_{CC} relative to GND, V_{CC}	−1.0 to +7.0 V
Supply voltage on inputs relative to GND, V_I	−1.0 to +7.0 V
Supply voltage on outputs relative to GND, V_O	−1.0 to +7.0 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; $V_{CC} = 5.0$ V; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance ($\overline{RAS}$, $\overline{REF}$, $\overline{SC}$, $\overline{WE}$, D_{IN}, $\overline{RCR}$, $\overline{INC}$, $\overline{DEC}$)	C_I			10	pF	GND = 0 V
Output capacitance (D_{OUT}, SYN)	C_O			10	pF	GND = 0 V

DC Characteristics

$T_A = -10$ to +55°C; $V_{CC} = 5.0$ V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Input voltage, high	V_{IH}	2.4		5.5	V	
Output voltage, low	V_{OL}	0		0.2 V_{CC}	V	$I_{OL} = 20\ \mu A$
Output voltage, high	V_{OH}	0.7 V_{CC}		V_{CC}	V	$I_{OH} = -20\ \mu A$
Input leakage current	I_I	−10		10	μA	$V_{IN} = 0$ V to 5.5 V; all other pins = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; $V_{OUT} = 0$ V to 5.5 V
Standby current	I_{CC1}			15	mA	$I_O = 0$ mA (D_{OUT}, SYN); $\overline{RAS}$, $\overline{SC}$, $\overline{REF}$, $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR} = V_{IH}$

Power Supply Current Characteristics

T_A = −10 to +55°C; V_{CC} = 5.0 V ±10%; GND = 0 V

		Limits							
		μPD41221-70			μPD41221-90				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Data transfer cycle current	I_{CC2}			45			45	mA	$t_{RC} = t_{RC}$ min
Data restore cycle current	I_{CC3}			40			40	mA	$t_{RC} = t_{RC}$ min
$\overline{REF}$ refresh cycle current	I_{CC4}			40			40	mA	$t_{FC} = t_{FC}$ min
Serial read cycle current	I_{CC5}			55			45	mA	$t_{SC} = t_{SC}$ min
Serial write cycle current	I_{CC6}			55			45	mA	$t_{SC} = t_{SC}$ min
Row counter reset cycle current	I_{CC7}			20			20	mA	Minimum timing
Row counter increment cycle current	I_{CC8}			20			20	mA	Minimum timing
Row counter decrement cycle current	I_{CC9}			20			20	mA	Minimum timing

Notes:
(1) An initial pause of 2 ms is required after power-up, followed by any eight cycles of $\overline{RAS}$ or $\overline{REF}$ before achieving proper device operation.

AC Characteristics

T_A = −10 to +55°C; V_{CC} = 5.0 V ±10%; GND = 0 V

		Limits					
		μPD41221-70		μPD41221-90			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RAS}$ cycle time	t_{RC}	710		710		ns	
$\overline{RAS}$ pulse width	t_{RAS}	500	2000	500	2000	ns	
$\overline{RAS}$ precharge time	t_{RP}	200		200		ns	
$\overline{RAS}$ to $\overline{REF}$ delay time	t_{RFD}	200		200		ns	
$\overline{RAS}$ to $\overline{SC}$ delay time	t_{RSD}	300		300		ns	
Read setup time before $\overline{RAS}$ low	t_{RRS}	0		0		ns	
Read hold time after $\overline{RAS}$ high	t_{RRH}	20		20		ns	
$\overline{REF}$ precharge time before $\overline{RAS}$ low	t_{FRP}	200		200		ns	
$\overline{SC}$ precharge time before $\overline{RAS}$ low	t_{SRP}	200		200		ns	
$\overline{WE}$ setup time before $\overline{RAS}$ low	t_{WRS}	0		0		ns	
$\overline{WE}$ hold time after $\overline{RAS}$ low	t_{WRH}	50		50		ns	
Output disable time from $\overline{RAS}$ low	t_{RSZ}	0	400	0	400	ns	(Note 1)
$\overline{REF}$ cycle time	t_{FC}	710		710		ns	
$\overline{REF}$ pulse width	t_{REF}	500		500		ns	
$\overline{REF}$ precharge time	t_{FP}	200		200		ns	
$\overline{SC}$ cycle time	t_{SC}	70		90		ns	
$\overline{SC}$ pulse width	t_{SA}	25	2000	35	2000	ns	
$\overline{SC}$ precharge time	t_{SP}	25	2000	35	2000	ns	
$\overline{WE}$ setup time before $\overline{SC}$ low	t_{WSS}	0		0		ns	
$\overline{WE}$ hold time after $\overline{SC}$ low	t_{WSH}	25		35		ns	
Read setup time before $\overline{SC}$ low	t_{RSS}	0		0		ns	
Read hold time after $\overline{SC}$ high	t_{RSH}	20		30		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits μPD41221-70 Min	Limits μPD41221-70 Max	Limits μPD41221-90 Min	Limits μPD41221-90 Max	Unit	Test Conditions
Data input setup time before $\overline{SC}$ low	t_{DSS}	0		0		ns	
Data input hold time after $\overline{SC}$ low	t_{DSH}	25		35		ns	
Access time from $\overline{SC}$	t_{SAC}		55		75	ns	
Output disable time from $\overline{SC}$ low	t_{SCZ}	5	40	5	60	ns	(Note 1)
$\overline{RAS}$ to $\overline{RCR}$ delay time	t_{RRD}	200		200		ns	
$\overline{RAS}$ to $\overline{INC}$ delay time	t_{RID}	200		200		ns	
$\overline{RAS}$ to $\overline{DEC}$ delay time	t_{RDD}	200		200		ns	
$\overline{RCR}$ pulse width	t_{RCR}	100	2000	100	2000	ns	
$\overline{INC}$ pulse width	t_{INC}	100	2000	100	2000	ns	
$\overline{DEC}$ pulse width	t_{DEC}	100	2000	100	2000	ns	
Time between $\overline{RCR}$ and $\overline{INC}$	t_{RIP}	100		100		ns	
Time between $\overline{INC}$ and $\overline{DEC}$	t_{IDP}	100		100		ns	
Time between $\overline{RCR}$ and $\overline{DEC}$	t_{RDP}	100		100		ns	
$\overline{RCR}$ precharge time before $\overline{RAS}$ low	t_{RRP}	100		100		ns	
$\overline{INC}$ precharge time before $\overline{RAS}$ low	t_{IRP}	100		100		ns	
$\overline{DEC}$ precharge time before $\overline{RAS}$ low	t_{DRP}	100		100		ns	
SYN response time after 605th $\overline{SC}$	t_{SYA}		200		200	ns	
SYN recovery time after $\overline{RAS}$ low	t_{SYR}	0	1400	0	1400	ns	
Refresh interval	t_{REF}		2		2	ms	
$\overline{RAS}$ precharge (serial operation)	t_{RPS}		2		2	ms	
Serial data output valid	t_{SOV}		2		2	ms	
Transition time	t_T	3	35	3	35	ns	

Notes:

(1) t_{SCZ} and t_{RSZ} define the times at which the output achieves the open-circuit condition and are not referenced to output voltage levels. The duration of the output voltage level depends on the time constant of the load. See input and output timing waveforms and figures 1 and 2.

(2) Timing measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals and t_T.

Figure 1. Loading Conditions Test Circuit for SYN

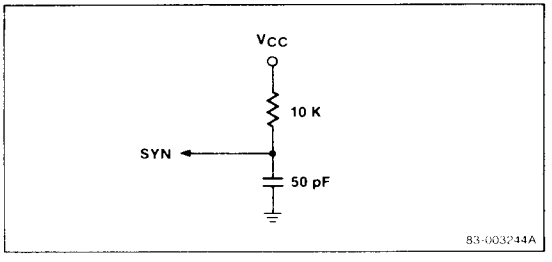
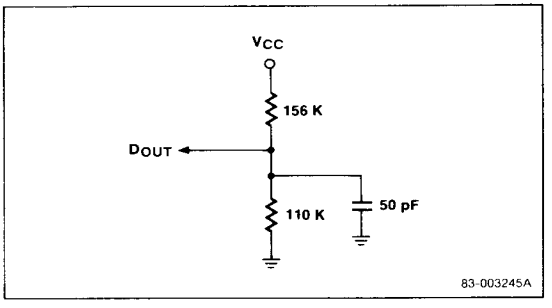


Figure 2. Loading Conditions Test Circuit for D_{OUT}

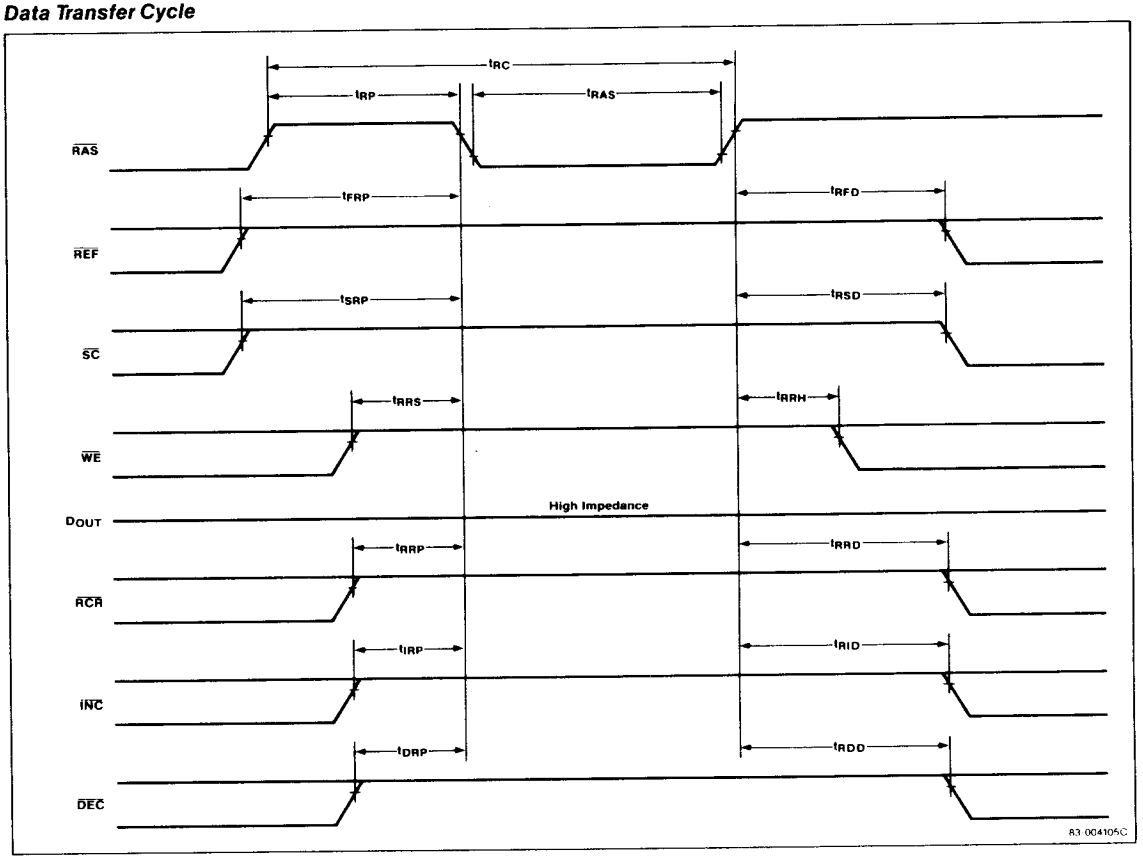


Timing Waveforms

Input Timing

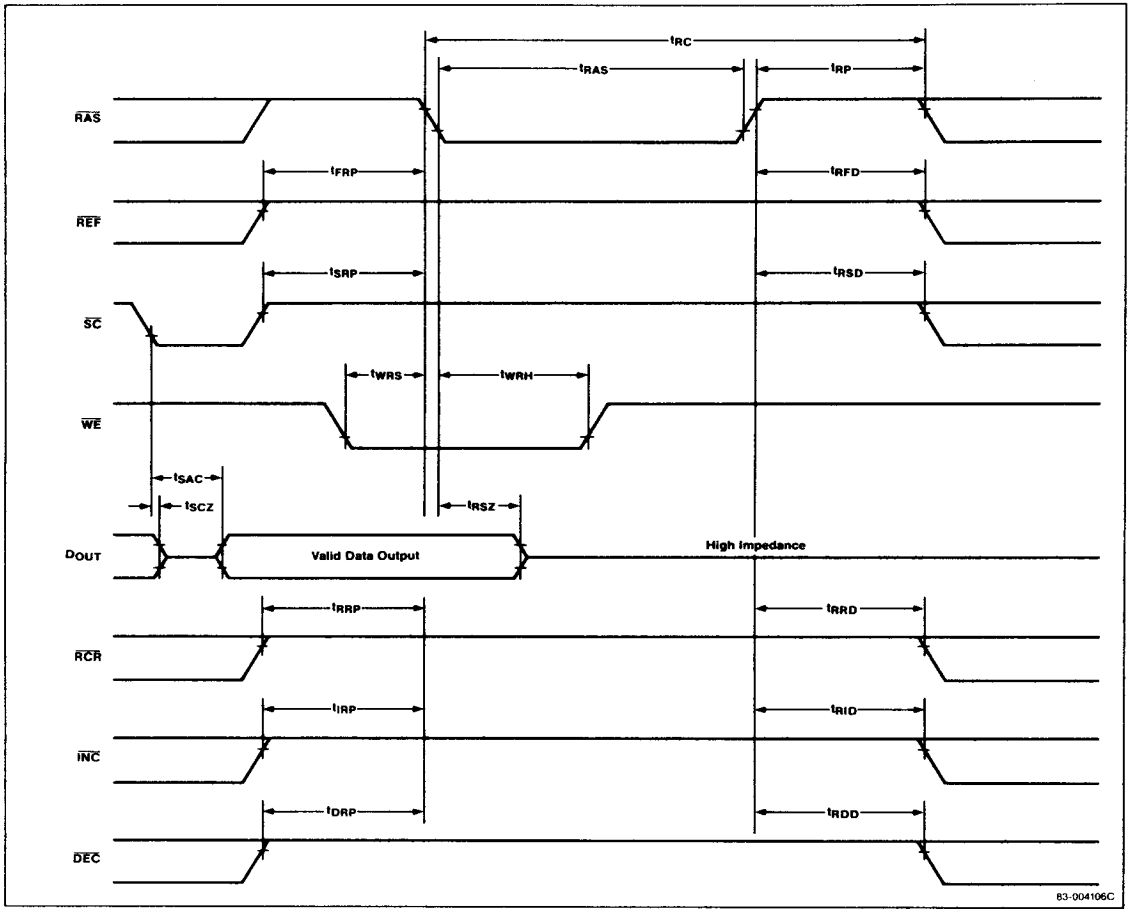
Output Timing

Data Transfer Cycle



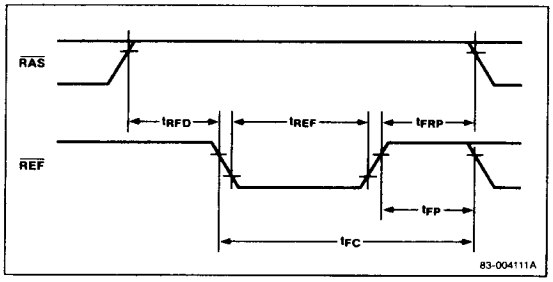
Timing Waveforms (cont)

Data Restore Cycle

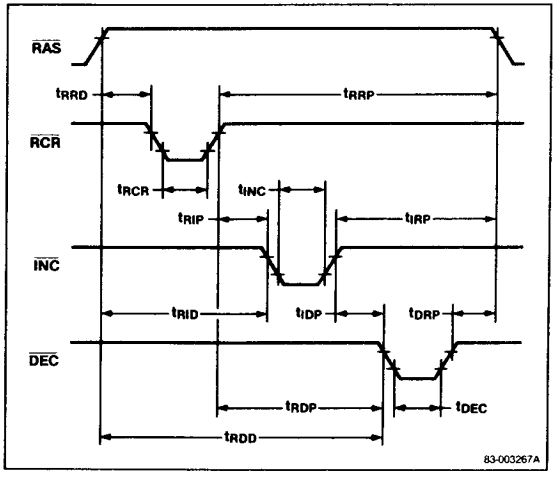


Timing Waveforms (cont)

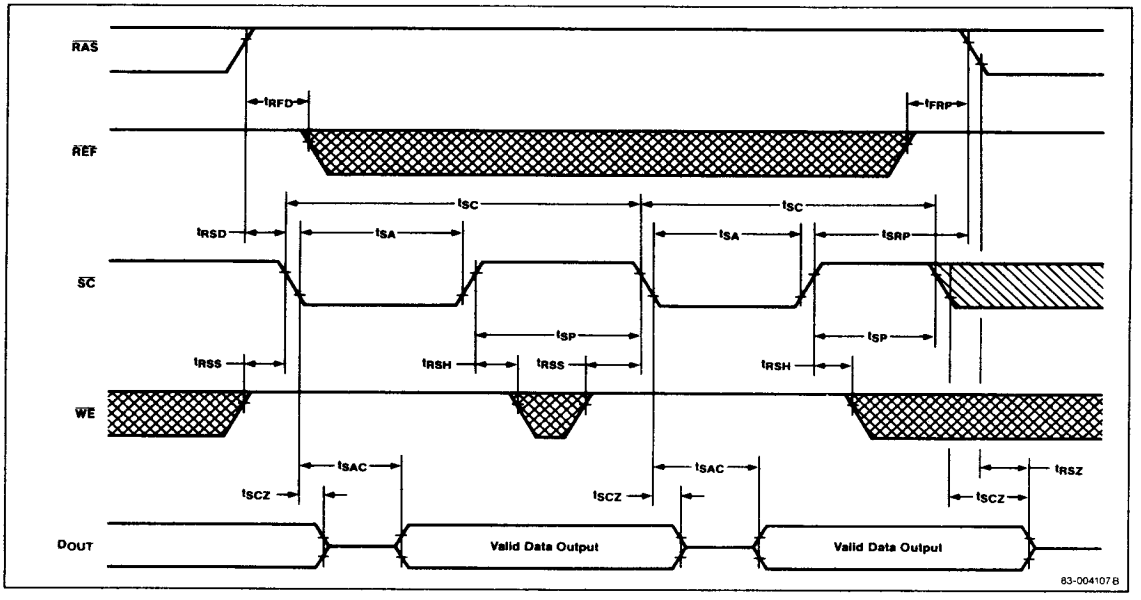
$\overline{REF}$ Refresh Cycle



Row Counter Cycle

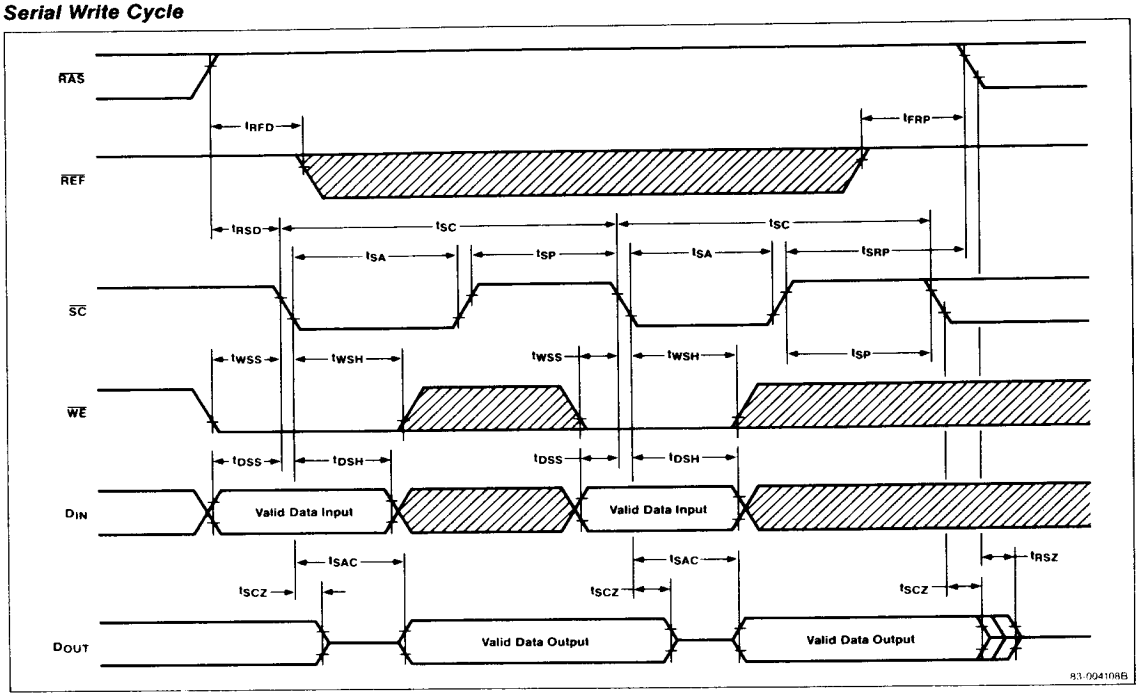


Serial Read Cycle

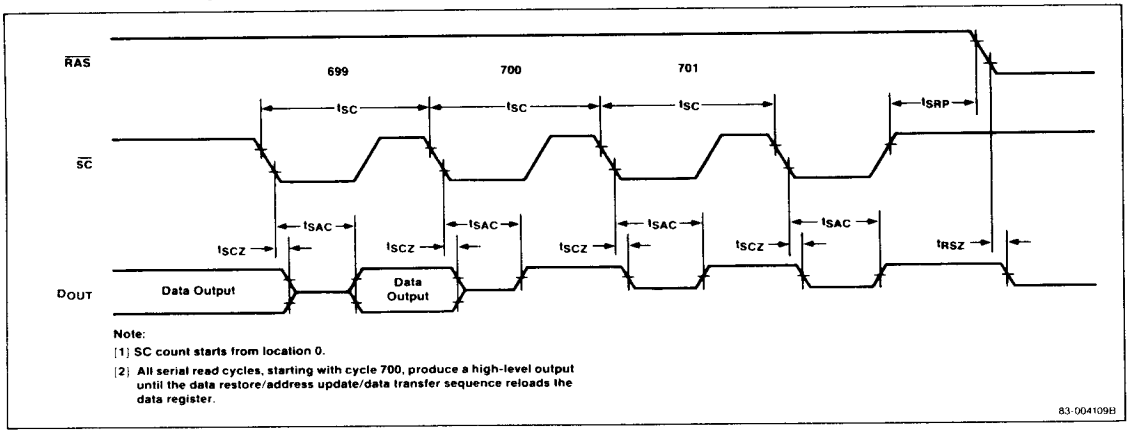


Timing Waveforms (cont)

Serial Write Cycle

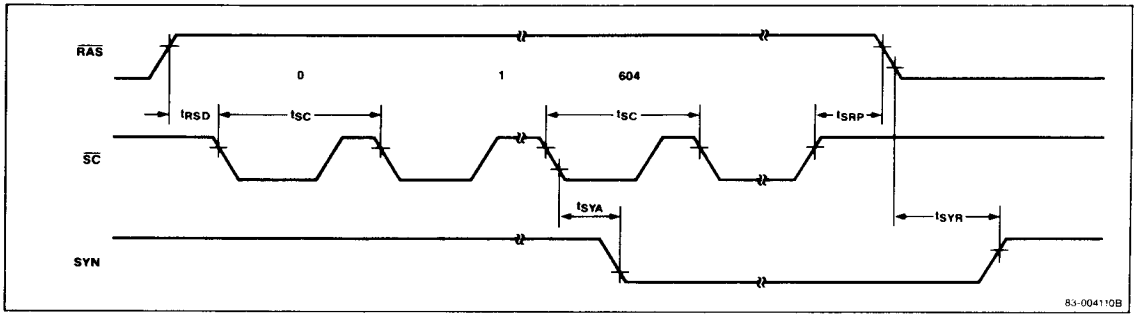


Serial Read Data Output Control



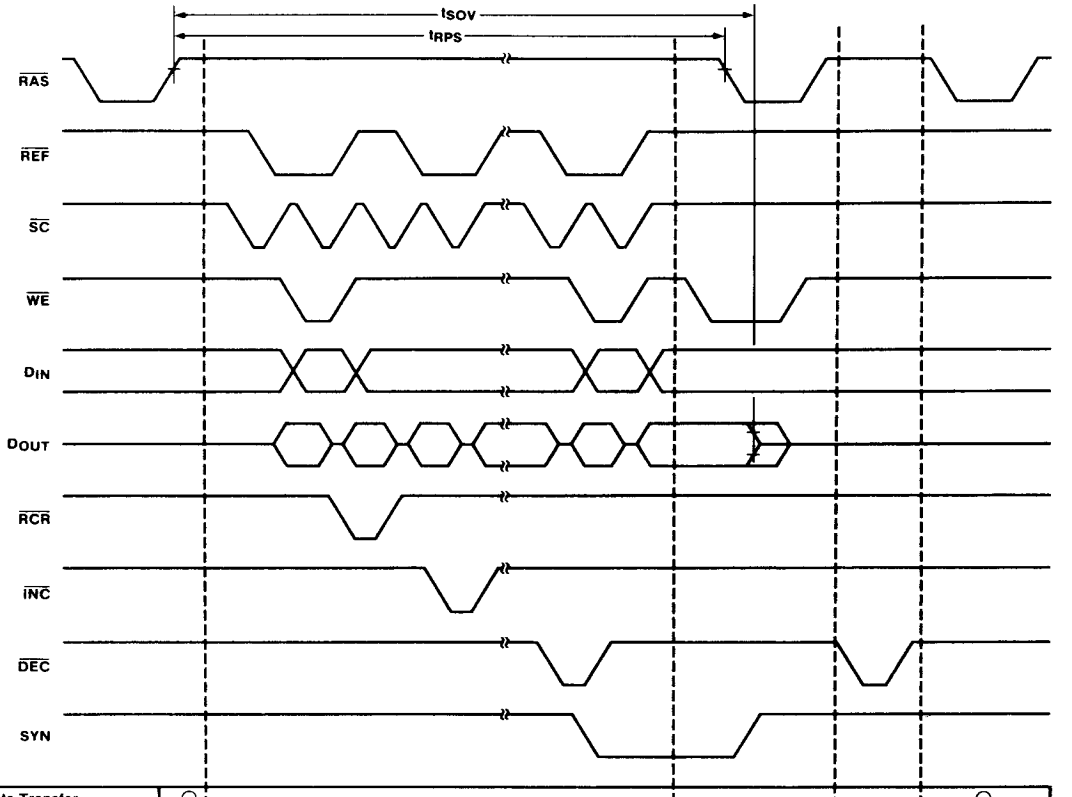
Timing Waveforms (cont)

Sync Acknowledge



Timing Waveforms (cont)

Total Timing Scheme



Data Transfer	○					○
Data Restore			○			
REF Refresh		○			○	
Serial Write		○				
Serial Read		○				
Row Counter Reset		○		○	○	
Row Counter Increment		○		○	○	
Row Counter Decrement		○		○	○	

Note:

[1] In this table a "O" indicates that the operation is available using the timing shown above.

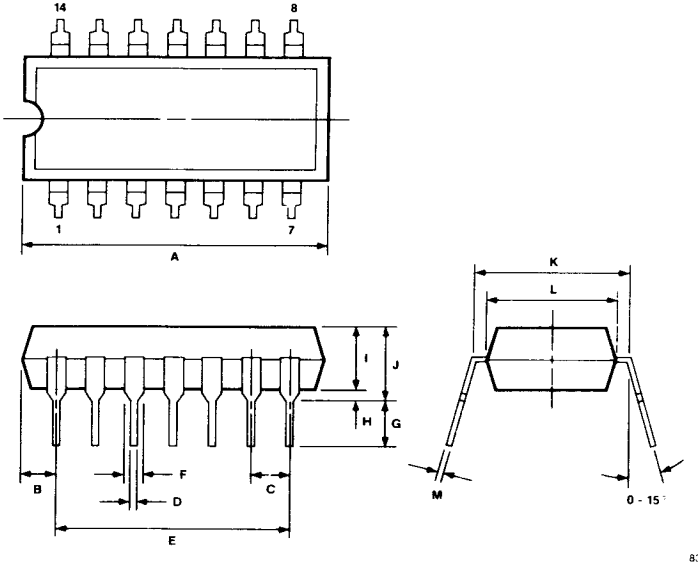
83-003270C

Package Drawings

14-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	15.24	.600
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



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