DATA SHEET

SKY77500 iPAC™ FEM for Quad-Band GSM / GPRS

Applications

- Quad-band cellular handsets comprised of
  - Class 4 GSM850/900
  - Class 1 DCS1800 PCS1900
  - Class 12 GPRS multi-slot operation

Features

- High efficiency
  - GSM850 43%
  - GSM900 43%
  - DCS 40%
  - PCS 40%
- Internal ICC sense-resistor for iPAC
- Closed loop iPAC or open loop operation with external PAC circuit
- Input/Output matching 50 ohms internal (with DC blocking)
- TX-VCO-to-antenna and antenna-to-RX-SAW filter RF interface
- TX harmonics below –33 dBm·
- PHEMT RF switches afford high linearity, low insertion loss and less than 20 µA supply current in receive modes
- Small outline
  - 8 mm x 10 mm
- Low profile
  - 1.2 mm maximum
- Low APC current:
  - 20 µA
- Gold plated, lead free contacts
- High impedance control inputs, 15 µA, typical

Description

The SKY77500 is a transmit and receive Front End Module (FEM) designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation—a complete transmit VCO-to-Antenna and Antenna-to-receive SAW filter solution. The FEM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of separate GSM850/900 and DCS1800/PCS1900 PA blocks, internal circuitry for matching to 50 Ω input and output impedances, TX harmonics filtering, high linearity and low insertion loss PHEMT RF switches, diplexer, and an integrated power amplifier control (iPAC™) function that utilizes an internal current-sense resistor. A custom silicon integrated circuit contains decoder circuitry to control the RF switches while providing a low current external control interface.

Two Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated onto a single Gallium Arsenide (GaAs) die; one supports the GSM850/900 bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. The output of each PA block and the outputs to the four receive pins are connected to the antenna pin through PHEMT RF switches and a diplexer. The GaAs die, PHEMT dies, Silicon (Si) die, and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

Band selection and control of transmit and receive RF signal flows are performed by use of three external control pins. See Figure 1 shown below. Two band select pins select GSM, DCS or PCS modes of operation and the TX_RX pin selects the receive or transmit mode of the respective RF switch (TX = logic 1). Proper timing of the logic on this pin, PAC Enable, and Analog Power Control (APC) allow for high isolation between the antenna and TX-VCO while the VCO is being tuned prior to the transmit burst. The PAC Enable input allows initial turn-on of the PAC circuitry to minimize battery drain.

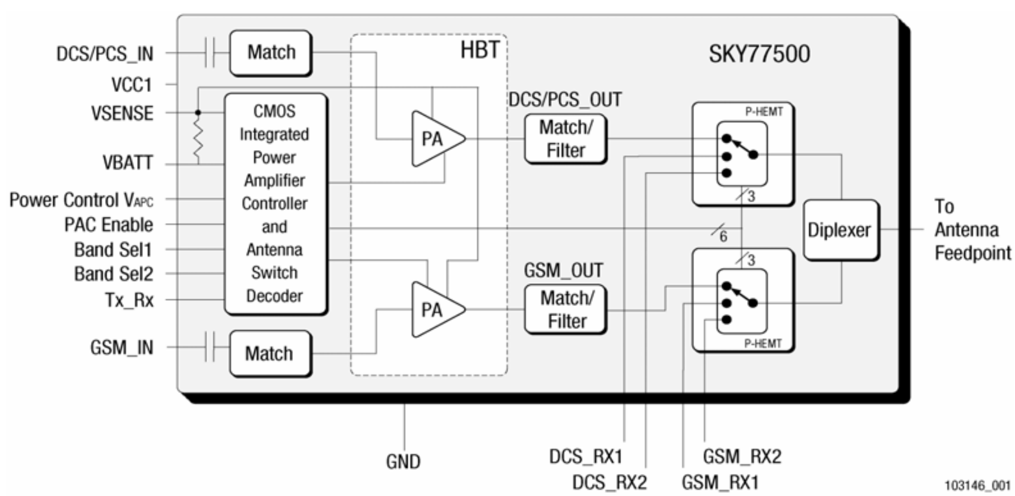


Figure 1. Functional Block Diagram

Electrical Specifications

This section contains the following tables for the electrical characteristics of the SKY77500 Power Amplifier Module.

The absolute maximum ratings and recommended operating conditions for the SKY77500 are listed in Table 1 and Table 2, respectively. Table 3 specifies the mode control logic and Table 4 contains the electrical characteristics of the SKY77500 for the modes, GSM850, GSM900, DCS1800, and PCS1900. Figure 2 is a diagram of a typical SKY77500 application.

The SKY77500 is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields. Detailed information on device dimensions, pin descriptions, packaging and handling can be found in later sections of this data sheet.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Power (P_{IN})	—	15	dBm
Supply Voltage (V_{CC}), Standby, $V_{APC} \leq$ 0.3 V, PAC ENABLE $\leq$ 0.2 V	—	7	V
Control Voltage (V_{APC})	–0.5	V_{CC_MAX} – 0.2 (See Table 4)	V
Storage Temperature	–55	+150	°C

Table 2. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V_{CC})	2.9	3.5	4.8V (1)	V
Supply Current (I_{CC})	0	—	2.5 (1)	A
Operating Case Temperature (T_{CASE}) –Bottom Surface of Package				°C
1–Slot (12.5% duty cycle)	–20	—	+100	°C
2–Slot (25.0% duty cycle)	–20	—	+100	°C
3–Slot (37.5% duty cycle)	–20	—	+85	°C
4–Slot (50.0% duty cycle)	–20	—	+85	°C

(1) In open loop operation: For charging conditions with V_{CC} > 4.8 V, derate I_{CC} linearly down to 0.5 A, maximum, at V_{CC} = 5.5 V.

Table 3. Mode Control Logic

Mode	Input Control Bits		
	TX_RX	BS1	BS2
GSM_RX1/STANDBY	0	0	0
GSM_RX2	0	0	1
DCS_RX1	0	1	0
DCS_RX2	0	1	1
GSM_TX	1	0	X (1)
DCS_TX	1	1	X (1)

(1) X = don't care

Table 4. SKY77500 Electrical Specifications (1) *(1 of 9)*

General							
Parameter		**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Supply voltage		V_{CC}	—	2.9	3.5	4.8	V
Power control impedance		Z_{APC}	—	85	100	115	kΩ
PAC ENABLE control voltage	Low	V_{PE}	—	–0.1	—	0.5	V
	High	V_{PE}	—	2.0	—	V_{CC}	V
PAC ENABLE current (6)		I_{PE}	$V_{PE} \leq 3.0$ V	—	—	30	µA
Band Select control voltage	Low	V_{BS1}, V_{BS2}	—	–0.1	—	0.5	V
	High	V_{BS1}, V_{BS2}	—	2.0	—	V_{CC}	V
Band Select current (6)		I_{BS1}, I_{BS2}	$V_{BS1} \leq 3.0$ V, $V_{BS2} \leq 3.0$ V	—	—	30	µA
TX_RX control voltage	Low	V_{TX_RX}	—	–0.1	—	0.5	V
	High	V_{TX_RX}	—	2.0	—	V_{CC}	V
TX_RX current (6)		I_{TX_RX}	—	—	—	30	µA
Leakage current	Standby Mode	I_{QS}	$V_{CC} = 3.5$ V $V_{APC} \leq 0.3$ V PAC ENABLE ≤ 0.2 V $T_{CASE} = +25$ °C $P_{IN} \leq -60$ dBm	—	10	30	µA
	Receive Mode	I_{QRX}		—	15	—	
Closed Loop V_{APC} Input Filter Bandwidth		$V_{APC\ FBW}$	—	95	135	170	kHz
Closed Loop V_{APC} Threshold		$V_{APC\ THCL}$	—	400	420	460	mV
Open Loop (4) V_{APC} Enable Threshold		$V_{APC\ THOL}$	—	200	—	800	mV

Table 4. SKY77500 Electrical Specifications [1] *(2 of 9)*

GSM850 Mode (f = 824 to 849 MHz and P_{IN} = 0 to 6 dBm)						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Frequency range	f	—	824	—	849	MHz
Input power	P_{IN}	—	0	—	6	dBm
Analog power control voltage	V_{APC}	—	0.4	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 33 dBm PAC ENABLE > 2.0 V pulse width 577 μs duty cycle 1:8 T_{CASE} = +25 °C	39	43	—	%
2nd to 13th harmonics	$2f_0$ to $13f_0$	BW = 3 MHz 5 dBm ≤ P_{OUT} ≤ 33 dBm	—	–45	–33	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	33.0	34.0	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	30.5	32.0	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.8 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	30.5	36.5	—	
Input VSWR	Γ_{IN}	P_{OUT} = 5 to 33 dBm, controlled by V_{APC}	—	1.5:1	2:1	—
Forward isolation [5]	$P_{OUT\ ENABLED\_RX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≤ 0.5 V Mode = GSM_RX (See Table 3)	—	–40	–20	dBm
	$P_{OUT\ STANDBY}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≤ 0.2 V TX_RX ≤ 0.2 V Mode = GSM_RX (See Table 3)	—	–60	–39	
	$P_{OUT\ ENABLED\_TX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0V TX_RX ≥ 2.0 V Mode = GSM_TX (See Table 3)	—	–25	0	
Coupling of GSM850 TX output (f_0) to GSM_RX output pins [5]	$CG_{LOTX\text{-}RX\_F0}$	5 dBm ≤ P_{OUT} ≤ +33 dBm Mode = GSM_TX (See Table 3)	—	5	+11	dBm
Coupling of GSM850 TX output ($2f_0$, $3f_0$) to DCS_RX output pins	$CG_{LOTX\text{-}DCSRX}$	5 dBm ≤ P_{OUT} ≤ +33 dBm Mode = GSM_TX (See Table 3)	—	–80	–70	dBc

Table 4. SKY77500 Electrical Specifications (1) *(3 of 9)*

GSM850 Mode (f = 824 to 849 MHz and P_{IN} = 0 to 6 dBm) *[continued]*						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Open Loop (4) Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +5 dBm	—	1.2	4.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +20.0 dBm	—	1.0	2.5	
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +33 dBm	—	1.4	3.0	
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled (2) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 12:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled (2) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 20:1, all phase angles	No module damage or permanent degradation			
RX Band Spurious	R_{X_SPUR}	At f_O + 20 MHz (869 to 894 MHz) RBW = 100 kHz V_{CC} = 3.5 V T_{CASE} = +25 °C 5 dBm ≤ P_{OUT} ≤ 33 dBm	—	–86	–83	dBm
		At 1930 to 1990 MHz RBW = 100 kHz V_{CC} = 3.5 V T_{CASE} = +25 °C 5 dBm ≤ P_{OUT} ≤ 33 dBm	—	—	–84	
Power control dynamic range	P_{CDR}	—	30	50		dB
Power control variation: Control level 7–15 (3.2 V ≤ V_{CC} ≤ 4.5 V)	P_{CV}	P_{OUT} +13 to +33 dBm, +25 °C P_{OUT} +13 to +33 dBm	–1.0 –1.5	— —	+1.0 +1.5	dB
Power control variation: Control level 16–19		P_{OUT} +5 to +11 dBm, +25 °C P_{OUT} +5 to +11 dBm	–1.7 –2.0	— —	+1.7 +2.0	
Power control slope	P_{CS}	5 to 33 dBm	—	—	300	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	700	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	50	65	—	deg.
GSM850 RECEIVE (f = 869 TO 894 MHz) Mode = GSM_RX						
Frequency range	f	—	869	—	894	MHz
Insertion Loss, ANT-to-GSM_RX (5)	IL GSM_RX	T_{CASE} = +25 °C	—	1.1	1.3	dB
VSWR ANT, GSM_RX (5)	Γ_{IN}, Γ_{OUT}	—	—	1.3:1	1.5:1	

Table 4. SKY77500 Electrical Specifications [(1)] *(4 of 9)*

GSM900 Mode (f = 880 to 915 MHz and P_{IN} = 0 to 6 dBm)						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Frequency range	F	—	880	—	915	MHz
Input power	P_{IN}	—	0	—	6	dBm
Analog power control voltage	V_{APC}	—	0.4	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 33 dBm PAC ENABLE > 2.0 V pulse width 577 μs duty cycle 1:8 T_{CASE} = +25 °C	39	43	—	%
2nd to 13th harmonics	$2f_0$ TO $13f_0$	BW = 3 MHz 5 dBm ≤ P_{OUT} ≤ 33 dBm	—	–45	–33	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	33.0	33.7	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	30.5	32.0	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.8 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	30.5	36.0	—	
Input VSWR	Γ_{IN}	P_{OUT} = 5 to 33 dBm controlled by V_{APC}	—	1.5:1	2:1	—
Forward isolation [(5)]	$P_{OUT\ ENABLED\_RX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≤ 0.5 V Mode = GSM_RX (See Table 3)	—	–45	–20	dBm
	$P_{OUT\ STANDBY}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≤ 0.2 V TX_RX ≤ 0.2 V Mode = GSM_RX (See Table 3)	—	–65	–39	
	$P_{OUT\ ENABLED\_TX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≥ 2.0 V Mode = GSM_TX (See Table 3)	—	–25	0	
Coupling of GSM900 TX output (f_0) to GSM_RX output pins [(5)]	$CG_{HITX\_RX\_FO}$	5 dBm ≤ P_{OUT} ≤ +33 dBm Mode = GSM_TX (See Table 3)	—	6	+11	dBm
Coupling of GSM900 TX output ($2f_0$, $3f_0$) to DCS_RX output pins	$CG_{HITX\text{-}DCSRX}$	5 dBm ≤ P_{OUT} ≤ +33 dBm Mode = GSM_TX (See Table 3)	—	–80	–70	dBc
Open Loop [(4)] Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +5 dBm	—	1.2	4.0	μs
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +20.0 dBm	—	1.0	2.5	
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +33 dBm	—	1.4	3.0	

Table 4. SKY77500 Electrical Specifications [1] *(5 of 9)*

GSM900 Mode (f = 880 to 915 MHz and P_{IN} = 0 to 6 dBm) *[continued]*							
Parameter		**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Spurious		Spur	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 12:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch		Load	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 20:1, all phase angles	No module damage or permanent degradation			
RX Band Spurious		R_{X_SPUR}	At f_0 + 20 MHz (935 to 960 MHz) RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 33 dBm T_{CASE} = +25 °C	—	–88	–84	dBm
			At f_0 + 10 MHz (925 TO 935 MHz) RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 33 dBm T_{CASE} = +25 °C	—	–86	–76	
			At 1805 to 1880 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 33 dBm T_{CASE} = +25 °C	—	—	–84	
Power control dynamic range		P_{CDR}	—	30	50	—	dB
Power control variation	Control level 5–15 (3.2 V ≤ V_{CC} ≤ 4.5 V)	P_{CV}	P_{OUT} +13 to +33 dBm, +25 °C P_{OUT} +13 to +33 dBm	–1.0 –1.5	— —	+1.0 +1.5	dB
	Control level 16–19		P_{OUT} +5 to +11 dBm, +25 °C P_{OUT} +5 to +11 dBm	–1.7 –2.0	— —	+1.76 +2.0	
Power control slope		P_{CS}	5 to 33 dBm	—	—	300	dB/V
Closed loop bandwidth		B_{CL}	V_{APC} = 1.0 V	—	700	—	kHz
Loop phase margin		P_M	V_{APC} = 1.0 V	50	65	—	deg.
GSM900 RECEIVE (f = 925 to 960 MHz) MODE = GSM_RX							
Frequency range		f	—	925	—	960	MHz
Insertion Loss, ANT-to-GSM_RX [5]		IL GSM_RX	T_{CASE} = +25 °C	—	1.1	1.3	dB
VSWR ANT, GSM_RX [5]		Γ_{IN}, Γ_{OUT}	—	—	1.2:1	1.5:1	

Table 4. SKY77500 Electrical Specifications [1] *(6 of 9)*

DCS1800 Mode (f = 1710 to 1785 MHz and P_{IN} = 0 to 6 dBm)						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Frequency range	f	—	1710	—	1785	MHz
Input power	P_{IN}	—	0	—	6	dBm
Analog power control voltage	V_{APC}	—	0.4	—	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 30 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	35	40	—	%
2nd to 7th harmonics	$2f_0$ to $7f_0$	BW = 3 MHz, 0 dBm ≤ P_{OUT} ≤ 30 dBm	—	–45	–33	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	30.0	31.0	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	27.5	29.5	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.8 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	27.5	33.5	—	
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 30 dBm controlled by V_{APC}	—	1.5:1	2:1	—
Forward isolation [5]	$P_{OUT\ ENABLED\_RX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≤ 0.5 V Mode = DCS_RX (See Table 3)	—	–60	–23	dBm
	$P_{OUT\ STANDBY}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≤ 0.2 V TX_RX ≤ 0.2 V Mode = DCS_RX (See Table 3)	—	–60	–50	
	$P_{OUT\ ENABLED\_TX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≥ 2.0 V Mode = DCS_TX (See Table 3)	—	–35	–5	
Coupling of DCS TX output to Receive RF output pins [5]	$CDCS_{TX-RX\_f0}$	Measured at all RX outputs 0 dBm ≤ P_{OUT} ≤ +30 dBm Mode = DCS_TX (See Table 3)	—	3	3	dBm
Open Loop [4] Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = 0 dBm	—	0.5	3.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +20.0 dBm	—	0.8	1.1	
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +30 dBm	—	1.2	1.5	

Table 4. SKY77500 Electrical Specifications (1) *(7 of 9)*

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
DCS1800 Mode (f = 1710 to 1785 MHz and P_{IN} = 0 to 6 dBm) *[continued]*						
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled (3) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 12:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled (3) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 20:1, all phase angles	No module damage or permanent degradation			
Rx Band Spurious	R_{X_SPUR}	At f_0 + 20 MHz (1805 to 1880 MHz) RBW = 100 kHz V_{CC} = 3.5 V 0 dBm ≤ P_{OUT} ≤ 30 dBm T_{CASE} = +25 °C	—	–90	–80	dBm
		At 925 to 960 MHz RBW = 100 kHz V_{CC} = 3.5 V 0 dBm ≤ P_{OUT} ≤ 30 dBm T_{CASE} = +25 °C	—	—	–87	
Power control dynamic range	P_{CDR}	—	35	50	—	dB
Power control variation: Control level 0–8 (3.2 V ≤ V_{CC} ≤ 4.5 V)	P_{CV}	P_{OUT} +14 to +30 dBm, +25 °C P_{OUT} +14 to +30 dBm	–1.0 –1.8	— —	+1.0 +1.8	dB
Power control variation: Control level 9–13		P_{OUT} +4 to +12 dBm, +25 °C P_{OUT} +4 to +12 dBm	–1.9 –3.3	— —	+1.9 +3.3	
Power control variation: Control level 14–15		P_{OUT} 0 to +2 dBm, +25 °C P_{OUT} 0 to +2 dBm	–3.0 –4.5	— —	+3.0 +4.5	
Power control slope	P_{CS}	0 to 30 dBm	—	—	500	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	500	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	75	—	—	deg.
DCS 1800 RECEIVE (f = 1805 to 1880 MHz) Mode = DCS_RX						
Frequency range	f	—	1805	—	1880	MHz
Insertion Loss, ANT-to-DCS_RX (5)	IL DCS_RX	T_{CASE} = +25 °C	—	1.3	1.5	dB
VSWR ANT, DCS_RX (5)	Γ_{IN}, Γ_{OUT}	—	—	1.2:1	1.5:1	

Table 4. SKY77500 Electrical Specifications (1) *(8 of 9)*

PCS1900 Mode (f = 1850 to 1910 MHz and P_{IN} = 0 to 6 dBm)						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Frequency range	f	—	1850		1910	MHz
Input power	P_{IN}	—	0		6	dBm
Analog power control voltage	V_{APC}	—	0.4		2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} = 30 dBm PAC ENABLE > 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	35	40	—	%
2nd to 7th harmonics	2fo to 7fo	BW = 3 MHz 0 dBm ≤ P_{OUT} ≤ 30 dBm	—	–40	–33	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V T_{CASE} = +25 °C	30.0	31.0	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	V_{CC} = 2.9 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	27.5	29.5	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	V_{CC} = 4.8 V PAC ENABLE > 2.0 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot.) P_{IN} = 0 dBm	27.5	33.5	—	
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 30 dBm controlled by V_{APC}	—	1.5:1	2.2:1	—
Forward isolation (5)	$P_{OUT\ ENABLED\_RX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≤ 0.5 V Mode = DCS_RX (See Table 3)	—	–65	–23	dBm
	$P_{OUT\ STANDBY}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≤ 0.2 V TX_RX ≤ 0.2 V Mode = DCS_RX (See Table 3)	—	–65	–50	
	$P_{OUT\ ENABLED\_TX}$	P_{IN} = 6 dBm V_{APC} ≤ 0.3 V PAC ENABLE ≥ 2.0 V TX_RX ≥ 2.0 V Mode = DCS_TX (See Table 3)	—	–35	–5	
Coupling of PCS TX output to Receive RF output pins (5)	$CPCS_{TX\text{-}RX\_f0}$	Measured at all RX outputs 0 dBm ≤ P_{OUT} ≤ +30 dBm Mode = DCS_TX (See Table 3)	—	3	3	dBm
Open Loop (4) Switching time	τ_{RISE}	Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = 0 dBm	—	0.5	3.0	µs
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +20 dBm	—	0.8	1.1	
		Time from P_{OUT} = –10 dBm to within 0.5 dB of P_{OUT} = +30 dBm	—	1.2	1.5	

Table 4. SKY77500 Electrical Specifications (1) *(9 of 9)*

PCS1900 Mode (f = 1850 to 1910 MHz and P_{IN} = 0 to 6 dBm) *[continued]*						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled (3) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 12:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled (3) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 20:1, all phase angles	No module damage or permanent degradation			
Rx Band Spurious	R_{X_SPUR}	At f_0 + 20 MHz (1930 to 1990 MHz) RBW = 100 kHz V_{CC} = 3.5 V 0 dBm ≤ P_{OUT} ≤ 30 dBm T_{CASE} = +25 °C	—	–89	–80	dBm
		At 869 to 894 MHz RBW = 100 kHz V_{CC} = 3.5 V 0 dBm ≤ P_{OUT} ≤ 30 dBm T_{CASE} = +25 °C	—	—	–87	
Power control dynamic range	P_{CDR}	V_{CC} = 3.5 V	35	50	—	dB
Power control variation: Control level 0–8 (3.2 V ≤ V_{CC} ≤ 4.5 V)	P_{CV}	P_{OUT} +14 to +30 dBm, +25 °C P_{OUT} +14 to +30 dBm	–1.0 –1.8	— —	+1.0 +1.8	dB
Power control variation: Control level 9–13		P_{OUT} +4 to +12 dBm, +25 °C P_{OUT} +4 to +12 dBm	–1.9 –3.3	— —	+1.9 +3.3	
Power control variation: Control level 14–15		P_{OUT} 0 to +2 dBm, +25 °C P_{OUT} 0 to +2 dBm	–3.0 –4.5	— —	+3.0 +4.5	
Power control slope	P_{CS}	0 to 30 dBm	—	—	550	dB/V
Closed loop bandwidth	B_{CL}	V_{APC} = 1.0 V	—	500	—	kHz
Loop phase margin	P_M	V_{APC} = 1.0 V	75	—	—	deg.
PCS 1900 RECEIVE (f = 1930 to 1990 MHz) Mode = DCS_RX						
Frequency range	f	—	1930	—	1990	MHz
Insertion Loss, ANT-to-DCS_RX (5)	IL DCS_RX	T_{CASE} = +25 °C	—	1.3	1.5	dB
VSWR ANT, DCS_RX (5)	Γ_{IN}, Γ_{OUT}	—	—	1.2:1	1.5:1	

(1) Unless specified otherwise:
T_{CASE} = –20 °C to max. operating temperature (see Table 2), RL = 50 Ω, pulsed operation with pulse width ≤ 1154 μs and duty cycle ≤ 2:8, V_{CC} = 2.9 V to 4.8 V.

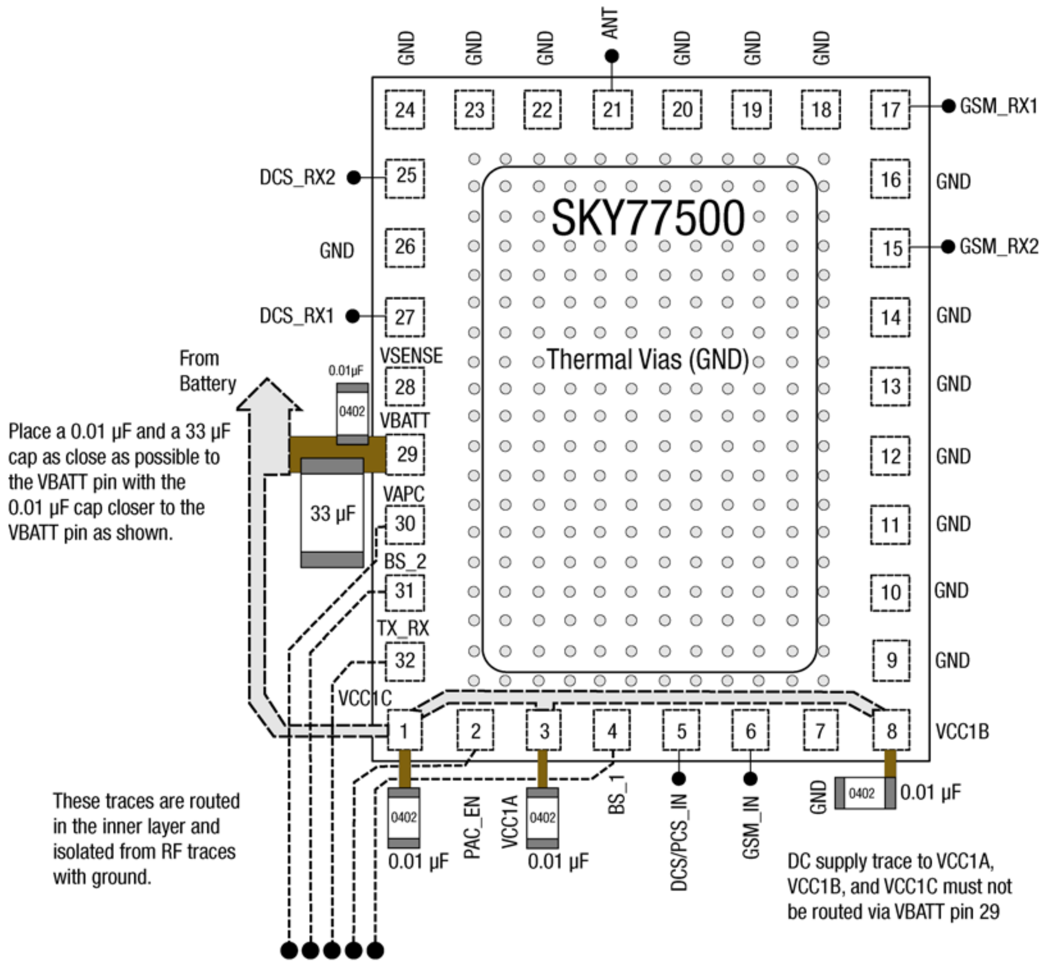
(2) I_{CC} = 0A to xA, where x = current at P_{OUT} = 33 dBm, 50 Ω load, and V_{CC} = 3.5 V.

(3) I_{CC} = 0A to xA, where x = current at P_{OUT} = 30 dBm, 50 Ω load, and V_{CC} = 3.5 V.

(4) This device has an Open Loop mode that allows bypassing the internal PAC circuitry. See the Technical Information section at end of this document for further information.

(5) Terminate all unused RF ports with 50 Ω load.

(6) BS_1, BS_2, TX_RX, and PAC_EN inputs have active 200 kΩ pulldowns to ground.



NOTES:

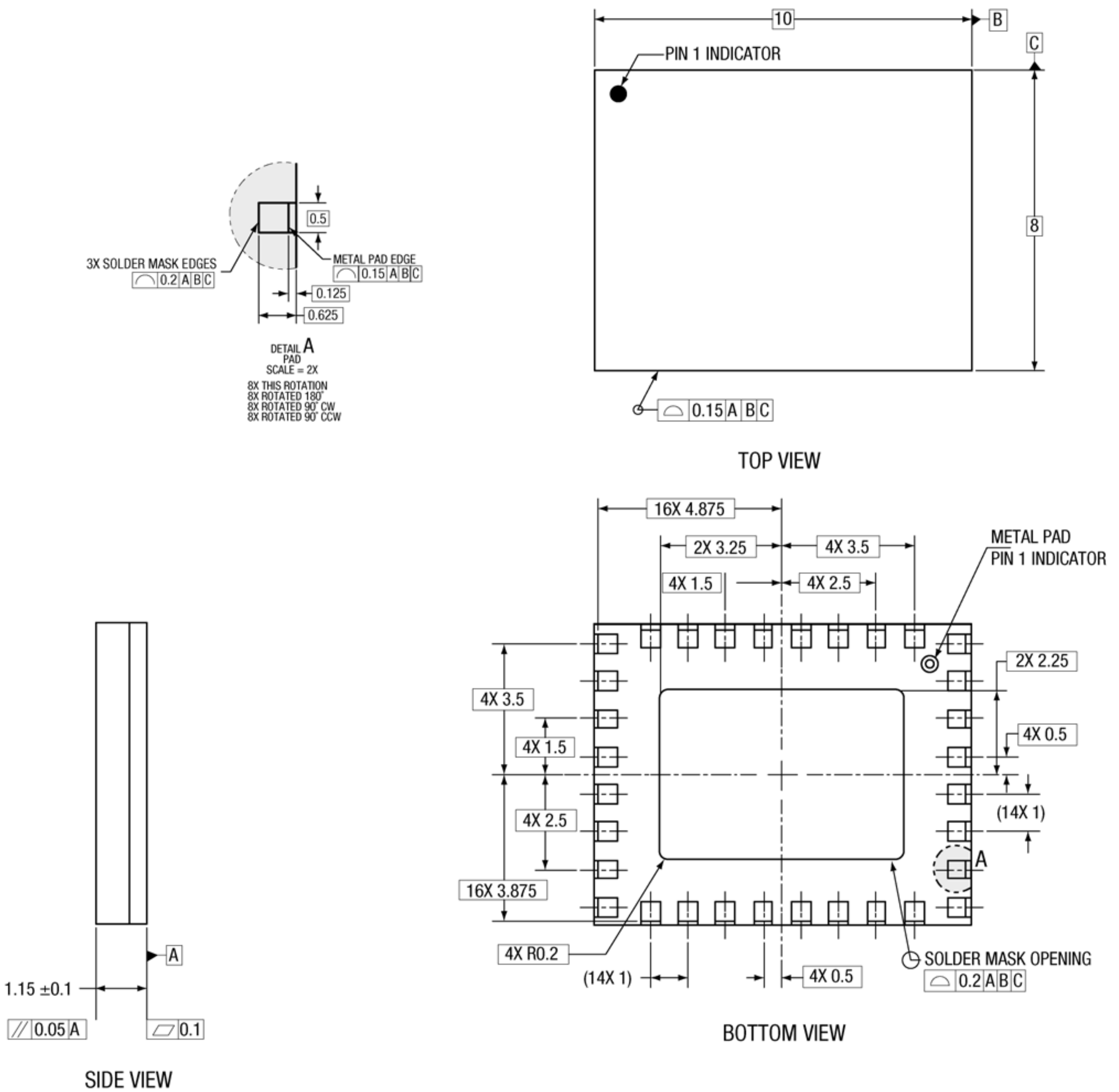
1. The value of 33 µF cap is dependent on the noise level on the phone board.
2. Depending on noise level on phone board, not all 0402, 0.01 µF caps may be needed.
3. Make sure to have sufficient number of vias connecting VBATT pin to battery trace.
4. VBATT trace width should be ≥ 1 mm.
5. Ensure a sufficient number of vias connecting VCC1A, B, and C to battery trace.
6. VCC1A, B, and C trace widths should be ≥ 0.25 mm.
7. Ground terminals of all bypass caps are connected to ground plane with vias.
8. Dotted traces can be routed in the inner layers.

103146_002

Figure 2. Typical SKY77500 FEM Application

Package Dimensions and Pin Description

Figure 3 is a mechanical diagram of the pad layout for the SKY77500, a 32-pin leadless quad-band FEM module. Figure 4 provides a recommended phone board layout footprint for the FEM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals. Figure 5 shows the device pin configuration and the pin numbering convention, which starts with pin 1 at the upper left, as indicated, and increments counter-clockwise around the package. Table 5 lists the pin names and signal descriptions. Typical case markings are shown in Figure 6.



NOTES: unless otherwise specified.
1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. ALL PADS ARE SOLDER MASK DEFINED.

103146_003

Figure 3. SKY77500 FEM Package Dimensions – 32-pin Leadless (All Views)

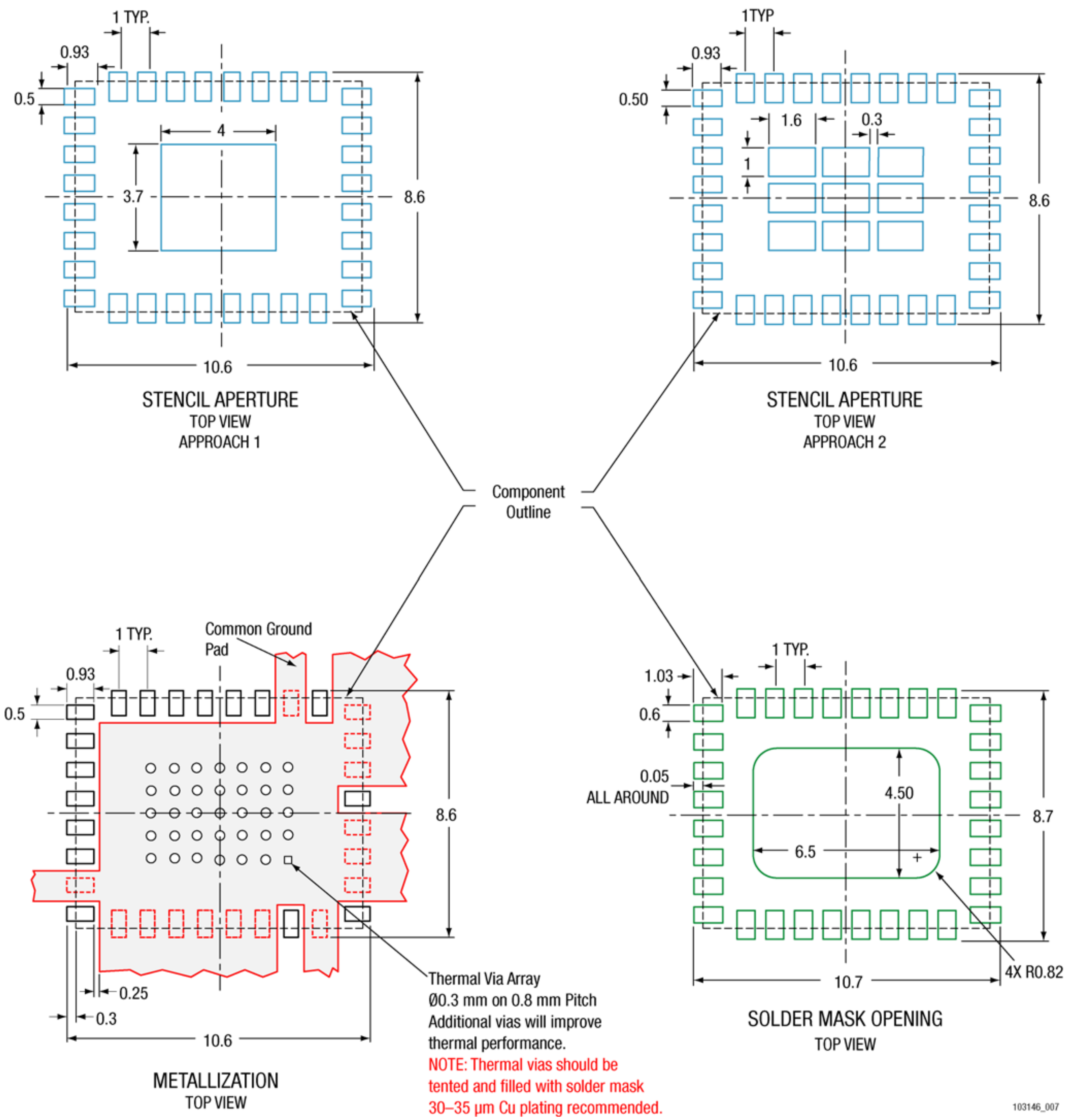


Figure 4. Phone PCB Layout Footprint for 8 x 10 mm, 32-Pin Package – SKY77500

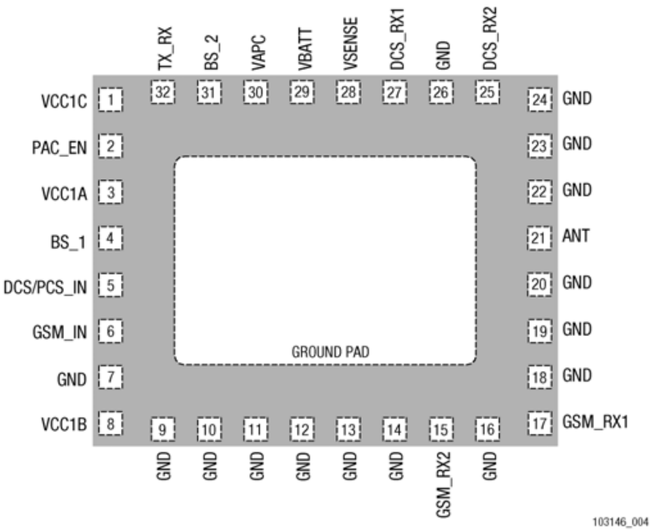


Figure 5. SKY77500 FEM Package Pin Configuration – 32-pin Leadless (Top View)

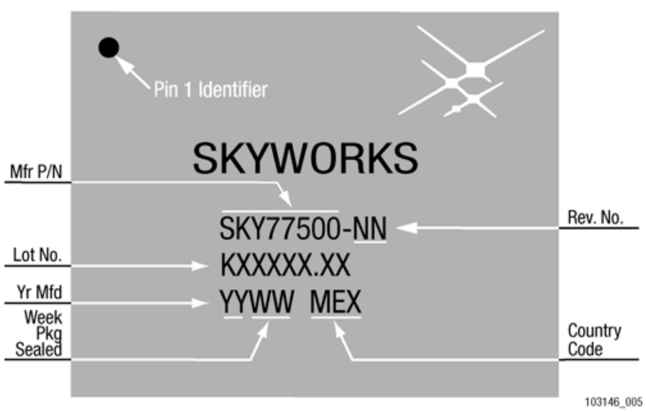


Figure 6. Typical Case Markings

Table 5. Pin Names and Signal Descriptions

Pin	Name	Description
1	VCC1C	VCC (to PAC and switch control)
2	PAC ENABLE	Closed loop PAC mode CMOS enable
3	VCC1A	VCC (to GSM 1st stage, DCS 1st stages)
4	BS_1	Band Select 1 (mode control)
5	DCS/PCS_IN	RF input 1710–1910 MHz
6	GSM_IN	RF input 824–915 MHz
7	GND	RF and DC Ground
8	VCC1B	VCC (to GSM 2nd stage, DCS 2nd stage)
9–14	GND	RF and DC Ground
15	GSM_RX2	GSM Receive RF output, 869 to 960 MHz
16	GND	RF and DC Ground
17	GSM_RX1	GSM Receive RF output, 869 to 960 MHz
18–20	GND	RF and DC Ground
21	ANT	RF IN / RF OUT to Antenna
22–24	GND	RF and DC Ground
25	DCS_RX2	DCS / PCS Receive RF output, 1805–1990 MHz
26	GND	RF and DC Ground
27	DCS_RX1	DCS / PCS Receive RF output, 1805–1990 MHz
28	VSENSE	Feedback voltage for current sense (DO NOT CONNECT THIS PIN ON CIRCUIT BOARD FOR CLOSED LOOP OPERATION.)
29	VBATT	Battery input voltage
30	VAPC	Power Control bias voltage input
31	BS_2	Band Select 2 (mode control)
32	TX_RX	Transmit / Receive select (mode control)
(33)	GROUND PAD	Ground Pad, bottom of package

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77500 is capable of withstanding an MSL 3/250 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 250 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 250 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD-020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568.*

Electrostatic Discharge Sensitivity

The SKY77500 is a Class I device. Figure 7 lists the Electrostatic Discharge (ESD) immunity level for each pin of the SKY77500 module. The numbers specify the ESD threshold levels for each pin where the I-V curve between the pin and ground starts to show degradation. ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after "the pin fails the electrical specification limits" or "the pin becomes completely non-functional". Skyworks' most stringent criteria fail devices as soon as the pin begins to show any degradation on a curve tracer. To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 6.

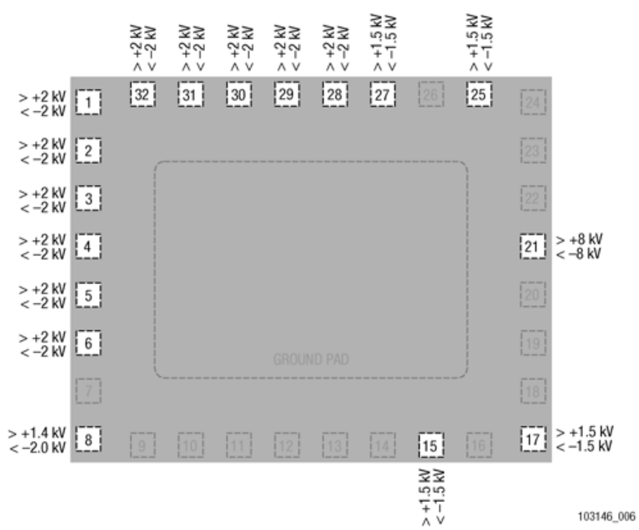


Figure 7. ESD Sensitivity Areas (Top View)

Table 6. Precautions for Handling GaAs IC based Products to Avoid ESD Induced Damage

Personnel Grounding	Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges
Facility	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation	Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors
Protective Packaging and Transportation	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

Technical Information

Closed loop control of the amplifier is enabled when PAC ENABLE is driven to logic high. The FEM PA collector current will then be directly proportional to the V_{APC} input voltage over the range of 400 mV to 2.1 V.

To meet the GSM power versus time mask and switching transient requirements the FEM must be provided with a DAC ramp profile on the V_{APC} input as well as proper timing on digital controls for the PAC circuitry and transmit/receive switches.

Note: Please refer to 3GPP TS 51.010-1: Mobile Station (MS) conformance specification. All GSM specifications are now the responsibility of 3GPP. The standards are available at http://www.3GPP.org.

The SKY77500 has been designed to comply with interface requirements and DAC resolution of leading base band devices. The ramp profile typically consists of a pedestal voltage, 10–16 discrete voltage steps on the rising edge of the burst, a constant region, 10–16 steps on the falling edge, and a final voltage. Typically, the user defines the start, stop, and 10–16 percentage values for each rising and falling edge, which are then applied as discrete voltages at the V_{APC} input. For the SKY77500, generally the same profile, scaled in amplitude, is used for all frequencies and power control levels. The ultimate purpose is to keep the RF output power ramp within the time mask and to maintain acceptable spectral limits at specified offset frequencies. The V_{APC} input has an internal reconstruction filter such that external resistors or capacitors are unnecessary on the phone board or the test fixture.

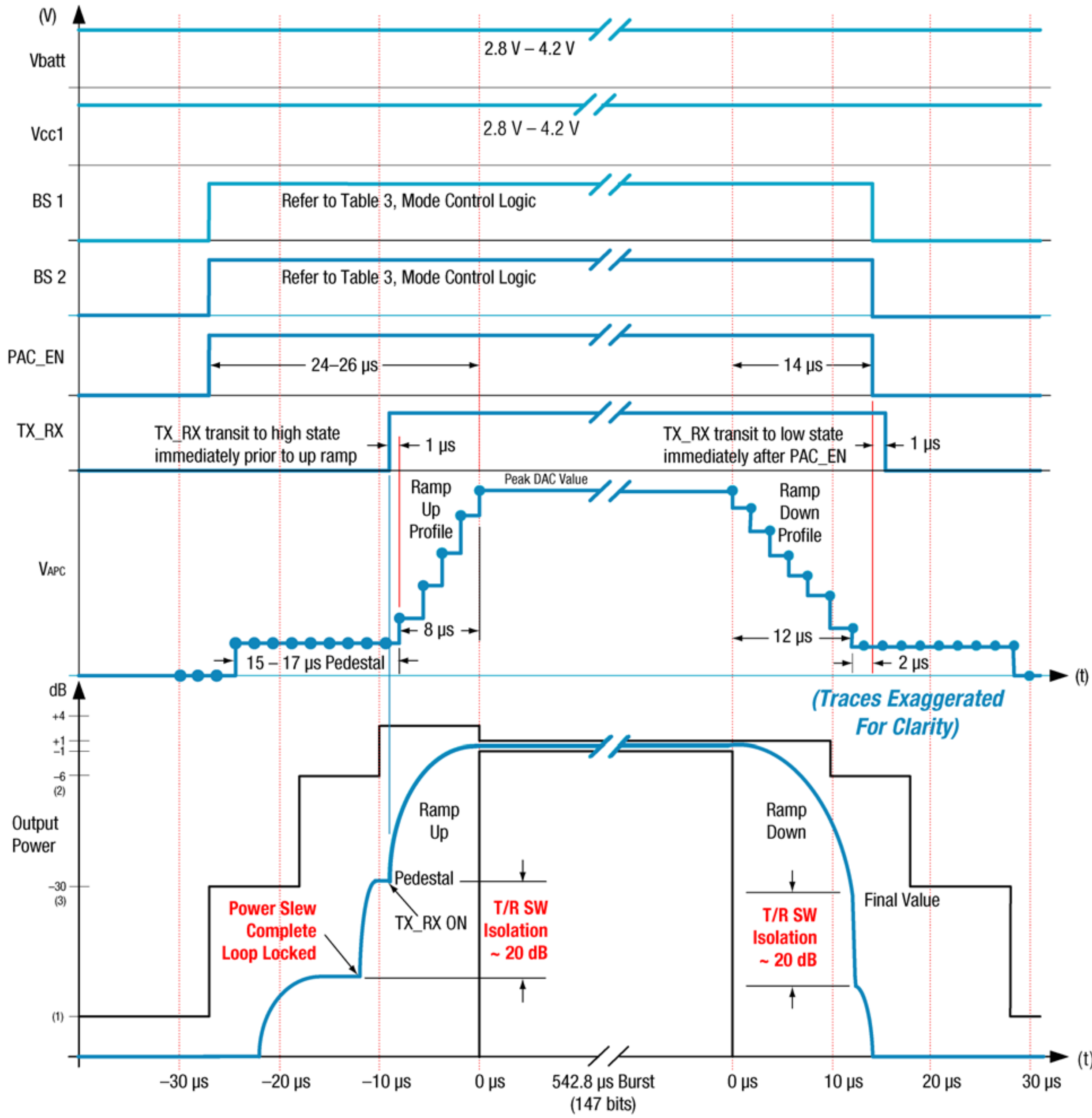
Figure 8 represents the dynamic characteristics of the RF output burst power that results from the ramp profile delivered by the DAC to the V_{APC} input. The transmit power must not exceed the given limits at the time specified relative to the start and end of the data burst. Additional requirements are placed on spectral components generated by switching transients. Ramping at high rates will result in components that violate these spectral limits. A ramp control signal must be applied to the V_{APC} pin, which results in the desired power ramp response. The log relationship of V_{APC} to P_{OUT}, along with the finite bandwidth and potential slew rate limitations of the feedback loop, results in a complex mapping of the ramp profile to the actual output power. Careful attention is required in generating the input waveform which results in the desired output response.

Figure 9 shows an example of the Skyworks FEM test setup for evaluation of RF performance with various ramp profiles.

Open Loop Control Mode

With PAC ENABLE at logic low, the voltage applied to V_{APC} is buffered and applied directly to the bases of the RF devices. This mode of operation provides backward compatibility with the existing amplifier designs and allows for various test scenarios. As with previous designs, an active clamp acts as a protection mechanism limiting the maximum voltage that can be applied to the base of the RF devices. This clamp voltage decreases with increasing supply voltage.

The enable threshold on the V_{APC} input for open loop operation exhibits a wide tolerance, which may vary from 200 mV to 800 mV. When enabled in Open Loop mode, the internal PAC circuitry (V-I converter and integrator) is placed in standby.



(1)	For GSM850 / E-GSM For DCS1800/PCS1900	–59 dBc or –36 dBm, whichever is higher –48 dBc or –48 dBm, whichever is higher
(2)	For GSM850 / E-GSM	–4 dBc for power control level 16, –2 dBc for power control level 17, –1 dBc for power control levels 18 and 19.
	For DCS1800 / PCS1900	–4 dBc for power control level 11, –2 dBc for power control level 12, –1 dBc for power control levels 13, 14, and 15.
(3)	For GSM850 / E-GSM For DCS1800/PCS1900	–30 dBc or –17 dBm, whichever is higher –30 dBc or –20 dBm, whichever is higher

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Figure 8. Example of FEM Recommended Timing Diagram

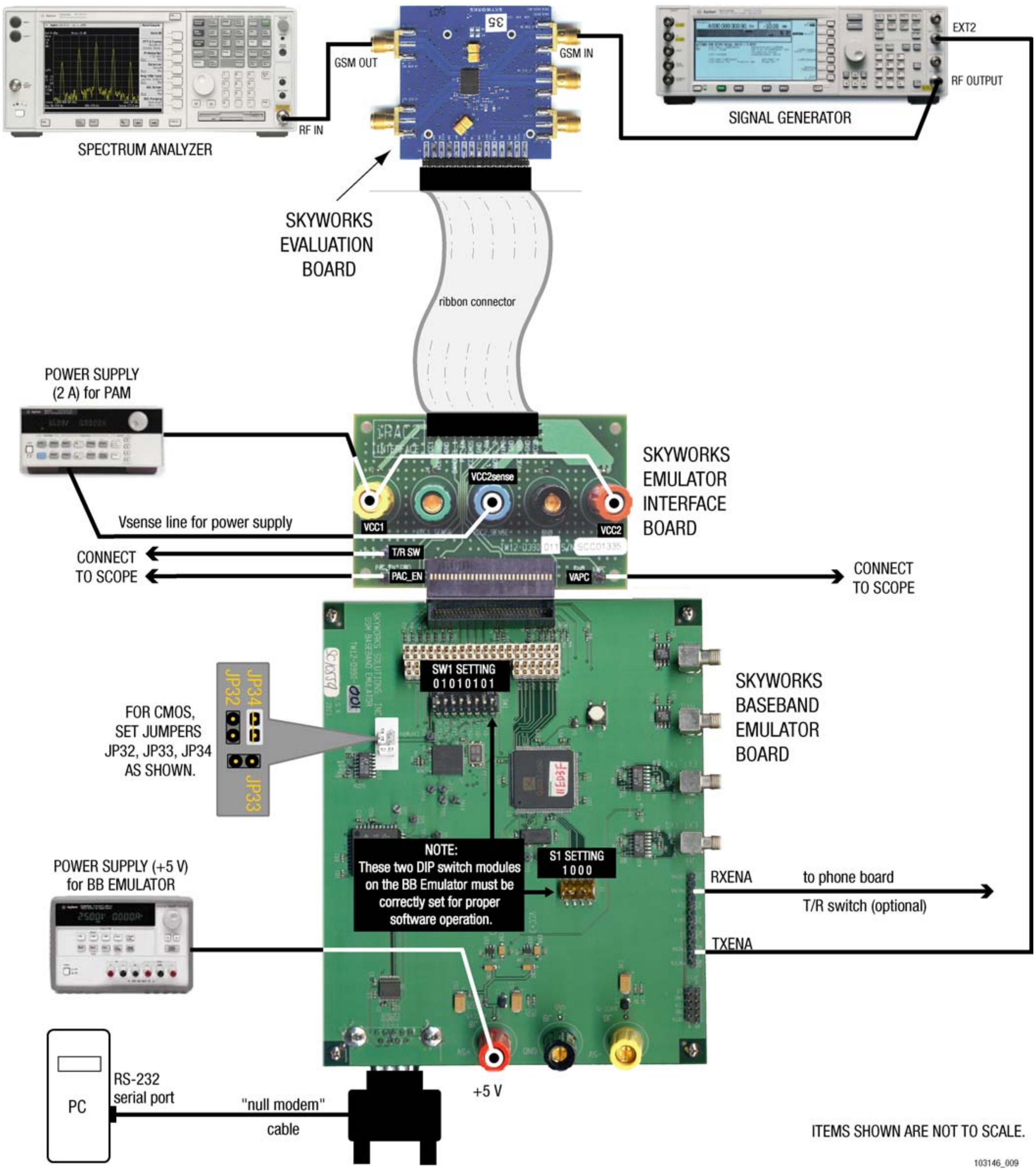

Figure 9. FEM Evaluation Test Setup – CMOS

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
SKY77500	SKY77500		MCM 8 x 10 x 1.2 mm	–20 °C to +100 °C

Revision History

Revision	Level	Date	Description
A		May 16, 2005	Initial Release

References

Application Note: Tape and Reel – RF Modules, Document Number 101568.

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Application Brief: iPAC™ – GSM Transmitter Timing, Calibration and Baseband Control, Document Number 103138

Application Note: iPAC™ Peak Output Power Calibration, Document Number 103180

Application Note: SKY77500 iPAC™ FEM Quad-Band GSM / GPRS Applications, Document Number 103164

User Guide: iPAC™ Test and Control – Baseband Emulator Interface, Document Number 103125

JEDEC Standard J-STD-020

3GPP TS 51.010-1; Mobile Station (MS) Conformance Specification

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