LRF07
8 x 8-bit Register File (3-Port)

FEATURES

- 8-word x 8-bit Three-Port Memory
- Independently Addressable Ports: 1 Input, 1 Output, 1 Bidirectional
- Low Power CMOS Technology
- Internally Latched Control Bits
- High-Speed Scratchpad Memory with Overlapped Data Fetch/Store
- Fully TTL Compatible
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Ceramic LCC

DESCRIPTION

The **LRF07** is an 8-word x 8-bit expandable register file with three independently addressable ports, designated A, B, and C. Each port has eight data lines, three address lines, and a port enable control. All address and control lines are registered to facilitate instruction pipelining in microprogrammed systems. All ports may be used simultaneously in any clock cycle.

The C port is a read only port. C port address lines (CA_{2-0}) are latched on the rising edge of CLK. The data indicated by the port address will be presented on the output lines one t_{ACC} following the rising clock edge on which the address is latched. If the same register is simultaneously addressed for writing from a different port, the data presented to the outputs is the contents of the register prior to the write operation.

The B port is a write port. B port address lines (BA_{2-0}) are latched on the rising edge of CLK. The contents of the B address register are decoded to control data routing multiplexers.

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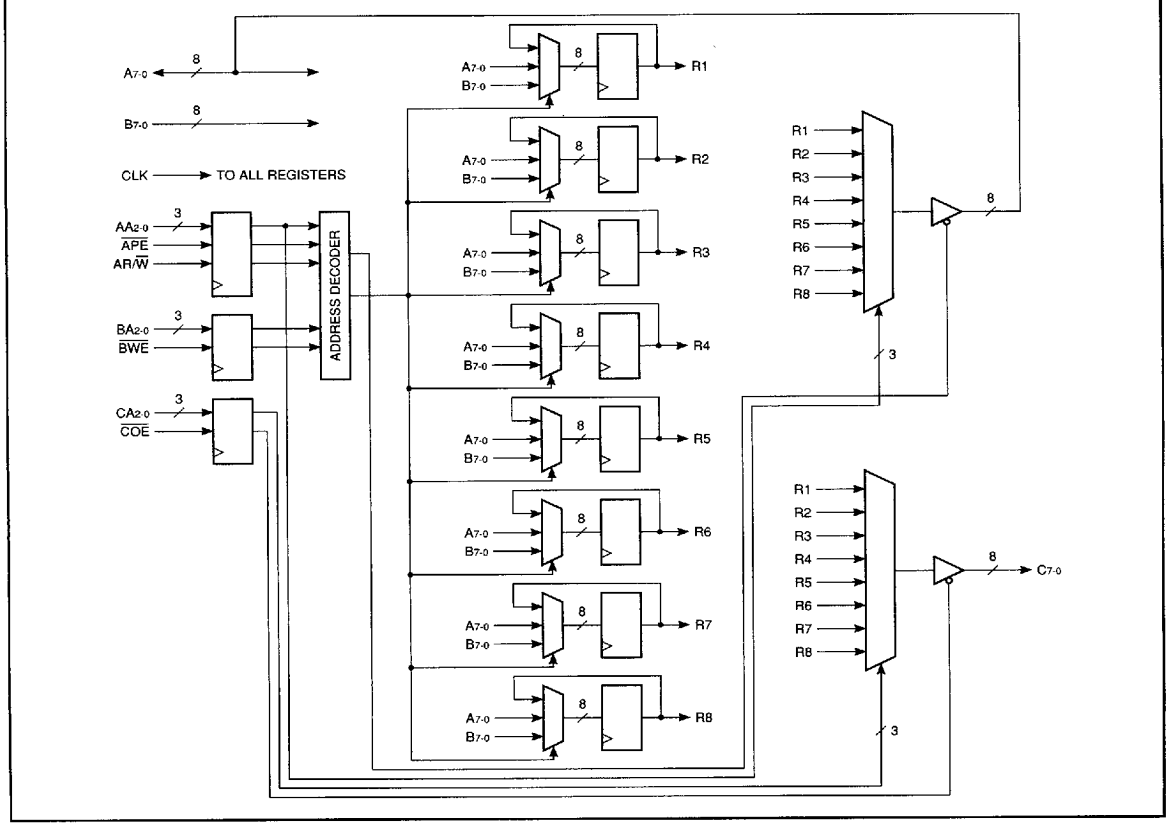
LRF07 BLOCK DIAGRAM



These supply data from the input pins to the desired register. The input data is latched into the addressed register on the rising clock edge following the one which latched the address.

The A port is a bidirectional port. The A READ/$\overline{\text{WRITE}}$ (AR/$\overline{\text{W}}$) control is latched along with the address lines ($AA_{2\text{-}0}$) and determines whether the A port acts as an input or an output during any clock period. When AR/$\overline{\text{W}}$ is HIGH at the rising clock edge, the A port presents the addressed data on the $A_{7\text{-}0}$ data lines.

Read operations on the A port are performed identically to C port reads. When AR/$\overline{\text{W}}$ is LOW at the rising clock edge, an A port write operation is executed in the same manner as a B port write. The input data is latched on the rising clock edge following the one which latched the address.

All ports have associated port enable inputs. These inputs are internally registered and are applied simultaneously with the corresponding port address. In the case of the C port, the $\overline{\text{COE}}$ input is a three-state output control. A HIGH latched in this input places $C_{7\text{-}0}$ in a high impedance state beginning one t_{DIS} following the rising clock edge that latched $\overline{\text{COE}}$. The B port enable $\overline{\text{BWE}}$ serves as a registered write enable input. A HIGH latched in this input disables write operations from the port on the following rising clock edge. The A port enable $\overline{\text{APE}}$, serves the dual function of write enable or three-state enable depending on the direction of the A port.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2.0	mA

SWITCHING CHARACTERISTICS

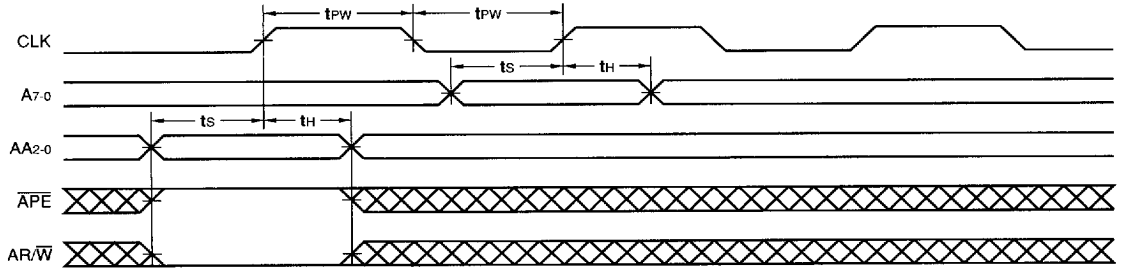
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LRF07– 35 Min	LRF07– 35 Max	LRF07– 20 Min	LRF07– 20 Max
t_{ACC}	Output Delay		35		20
t_{PW}	Clock Pulse Width	25		12	
t_S	Input Setup Time	15		7	
t_H	Input Hold Time	5		0	
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		15

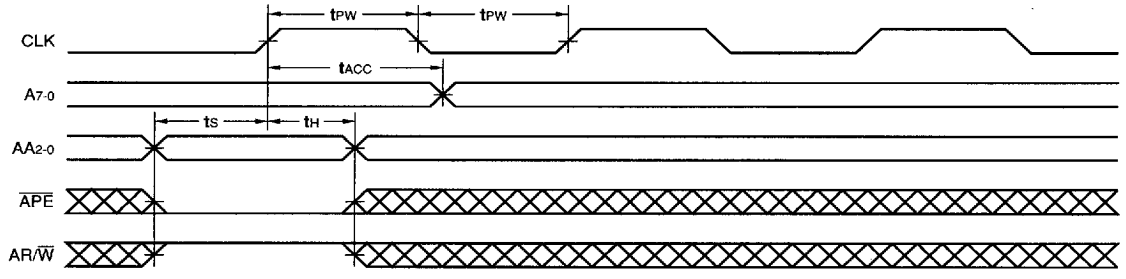
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LRF07– 40 Min	LRF07– 40 Max	LRF07– 25 Min	LRF07– 25 Max
t_{ACC}	Output Delay		40		25
t_{PW}	Clock Pulse Width	25		15	
t_S	Input Setup Time	15		10	
t_H	Input Hold Time	5		0	
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		20

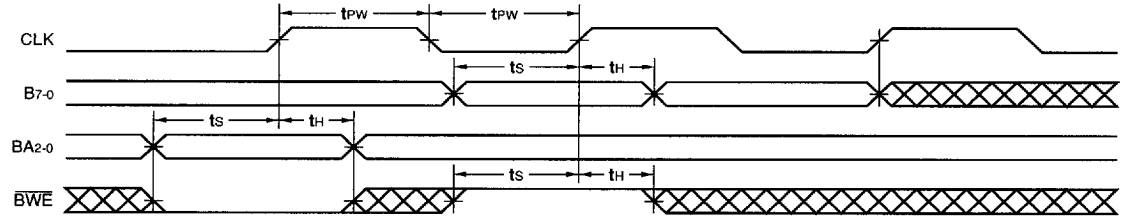
SWITCHING WAVEFORMS: PORT A WRITE OPERATION



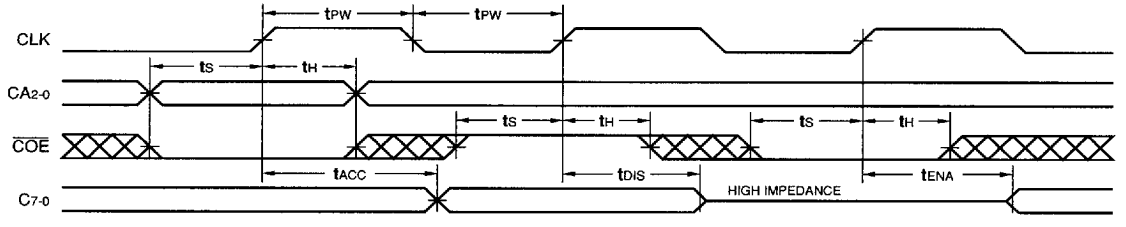
Switching Waveforms: Port A Read Operation



Switching Waveforms: Port B Write Operation



Switching Waveforms: Port C Read Operation



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

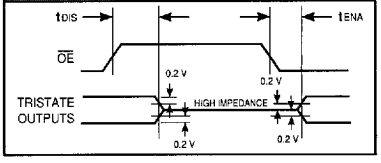
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. THRESHOLD LEVELS



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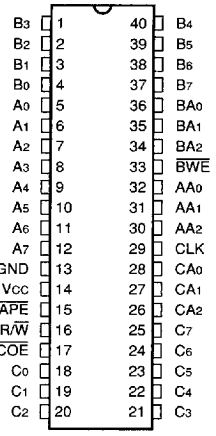
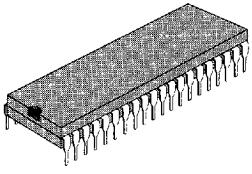
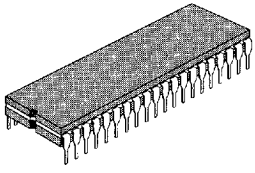
ORDERING INFORMATION

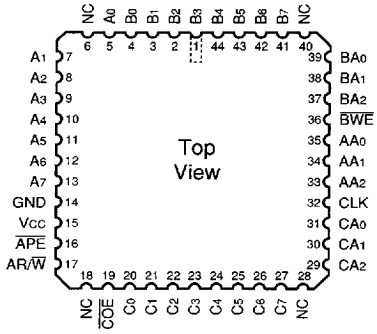
40-pin — 0.6" wide

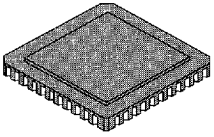






44-pin





Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING		
35 ns	LRF07PC35	LRF07CC35	LRF07KC35
20 ns	LRF07PC20	LRF07CC20	LRF07KC20
	–55°C to +125°C — COMMERCIAL SCREENING		
40 ns		LRF07CM40	LRF07KM40
25 ns		LRF07CM25	LRF07KM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
40 ns		LRF07CMB40	LRF07KMB40
25 ns		LRF07CMB25	LRF07KMB25