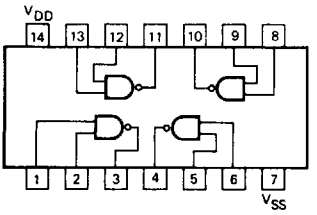
# GD4011B • GD4012B

## 4011B QUAD 2-INPUT NAND GATE

## 4012B DUAL 4-INPUT NAND GATE

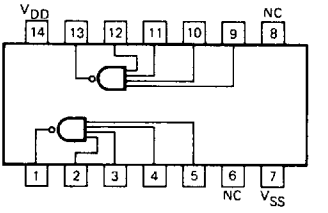
**DESCRIPTION** – These CMOS logic elements provide the positive input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

**4011B**
**LOGIC AND CONNECTION DIAGRAM**
**DIP (TOP VIEW)**




**NOTE:**
**The SO Package have the same pinouts (Connection Diagram) as the Dual In-line Package.**

**4012B**
**LOGIC AND CONNECTION DIAGRAM**
**DIP (TOP VIEW)**




**DC CHARACTERISTICS:** $V_{DD}$ as shown, $V_{SS}$ = 0 V (See Note 1)

| SYMBOL | PARAMETER | | LIMITS | | | | | | | | | UNITS | TEMP | TEST CONDITIONS See Note 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ = 5 V | | | $V_{DD}$ = 10 V | | | $V_{DD}$ = 15 V | | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| $I_{DD}$ | Quiescent Power Supply Current | XC | | | 1 | | | 2 | | | 4 | µA | MIN, 25°C | All inputs at 0 V or $V_{DD}$ |
| | | | | | 7.5 | | | 15 | | | 30 | | MAX | |
| | | XM | | | 0.25 | | | 0.5 | | | 1 | µA | MIN, 25°C | |
| | | | | | 7.5 | | | 15 | | | 30 | | MAX | |

**AC CHARACTERISTICS:** $V_{DD}$ as shown, $V_{SS}$ = 0 V, $T_A$ = 25°C, 4011B only (See Note 2)

| SYMBOL | PARAMETER | LIMITS | | | | | | | | | UNITS | TEST CONDITIONS See Note 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ = 5 V | | | $V_{DD}$ = 10 V | | | $V_{DD}$ = 15V | | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| $t_{PLH}$ | Propagation Delay | | 60 | 110 | | 25 | 60 | | 20 | 48 | ns | $C_L$ = 50 pF, |
| $t_{PHL}$ | | | 60 | 110 | | 25 | 60 | | 20 | 48 | ns | $R_L$ = 200 kΩ |
| $t_{TLH}$ | Output Transition Time | | 60 | 135 | | 30 | 70 | | 20 | 45 | ns | Input Transition |
| $t_{THL}$ | | | 60 | 135 | | 30 | 70 | | 20 | 45 | ns | Times ⩽ 20 ns |

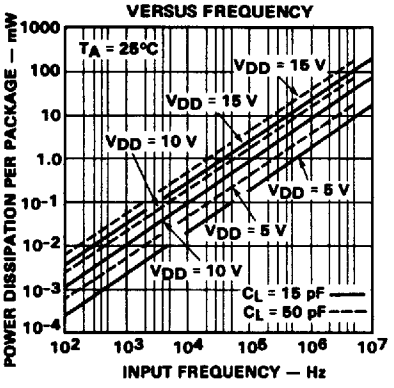
**AC CHARACTERISTICS:** $V_{DD}$ as shown, $V_{SS}$ = 0 V, $T_A$ = 25°C, 4012B only

| SYMBOL | PARAMETER | LIMITS | | | | | | | | | UNITS | TEST CONDITIONS See Note 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ = 5 V | | | $V_{DD}$ = 10 V | | | $V_{DD}$ = 15V | | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| $t_{PLH}$ | Propagation Delay | | 73 | 110 | | 33 | 60 | | 24 | 48 | ns | $C_L$ = 50 pF, |
| $t_{PHL}$ | | | 85 | 110 | | 31 | 60 | | 20 | 48 | ns | $R_L$ = 200 kΩ |
| $t_{TLH}$ | Output Transition Time | | 76 | 135 | | 37 | 70 | | 27 | 45 | ns | Input Transition |
| $t_{THL}$ | | | 67 | 135 | | 25 | 70 | | 17 | 45 | ns | Times ⩽ 20 ns |

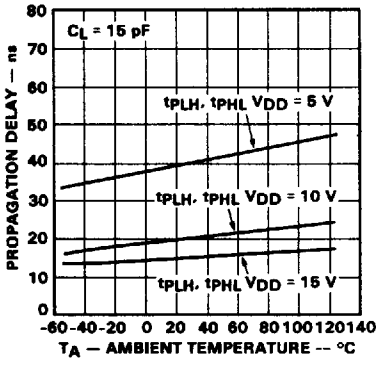
NOTES
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

## TYPICAL ELECTRICAL CHARACTERISTICS

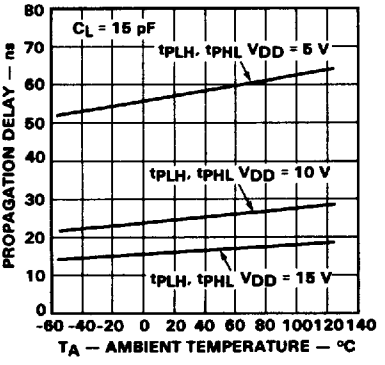
4011B AND 4012B
POWER DISSIPATION
VERSUS FREQUENCY



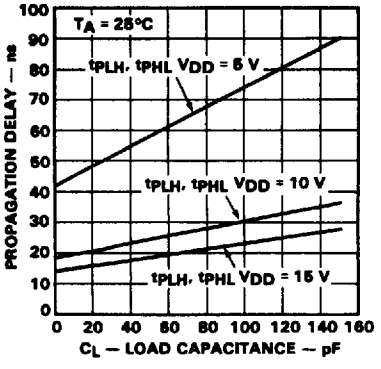

4011B
PROPAGATION DELAY
VERSUS TEMPERATURE




4012B
PROPAGATION DELAY
VERSUS TEMPERATURE




4011B
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE




4012B
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE