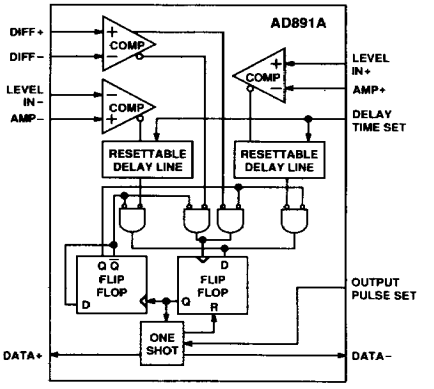
50 Mb/s Rigid Disk Data Qualifier

AD891A

FEATURES

Three Matched, Offset-Trimmed Comparators
ECL Logic Permits 50 Mb/s Transfer Rates
Three Levels of Data Qualification
Amplitude
Time Above Threshold
Polarity of Data
100 ps Typical Additional Pulse Pairing
Temperature Compensated Operation
Compatible with 10KH ECL Logic
One-Shot Period Set Using External Resistor
Time Above Threshold Qualification Set Using an External Resistor

AD891A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD891A disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891A provides three levels of data qualification. Level qualification is performed on alternating half-cycles of the data waveform using a user-defined threshold level which is applied to each of two comparators. The outputs of each comparator drive a user-programmable "resettable" delay-line. The "resettable" delay-line function allows the user to define the minimum time a data pulse must exceed the amplitude qualification level before a zero-crossing can be detected. The resettable delay-lines drive NAND gated flip-flops. A third zero-crossing comparator is employed to clock the NAND gated flip-flop. The NAND-gated flip-flop in turn drives the second flip-flop. The second flip-flop feeds back to the input of the NAND-gated flip-flop. The toggle action of the second flip-flop, therefore, provides alternate polarity data qualification. To ensure symmetric operation and low pulse pairing, all three comparators have trimmed offsets.

An external RLC passive delay-line/differentiator should be used with the AD891A; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

Each valid data pulse causes a one-shot to generate a pulse with a user-defined width. During the one-shot period the NAND-gated flip-flop is disabled, preventing detection of additional zero-crossing events. The one-shot also drives the ECL "Data Output" driver. The one-shot requires a single metal-film resistor to set its pulse width. Temperature stability is maintained by the use of an internal bandgap reference.

The AD891A's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10KH ECL logic levels. The AD891A can drive a properly terminated 75 Ω transmission line.

The AD891A is specified to operate over the commercial (0 to +70°C) temperature range. It is available in a 20-pin PLCC package (samples are available in a 14-pin side braze package).

9

SPECIFICATIONS (@ +25°C and +5 V, −5.2 V dc, unless otherwise noted)

Parameter	Conditions	AD891AJ Min	AD891AJ Typ	AD891AJ Max	Units
COMPARATOR SPECIFICATIONS					
Input Offset Voltage			0.25	**1.0**	mV
Input Offset Current			100		nA
Input Bias Current			1.6	**3.0**	μA
Open Loop Gain	f = 10 MHz		66		dB
Input Resistance	Differential		500		kΩ
Input Capacitance	Differential		**1**	5	pF
Input Common Mode Range	Referred to Digital GND	−1.5		+2.2	V
RESETTABLE DELAY-LINE SPECIFICATIONS					
Resistor Scaling[1]			Delay ≈ 2 + 5 × R_{SET}		ns
Pulse Duration	R_{SET} = 1 kΩ	**5**	7	**12**	ns
	R_{SET} = 5 kΩ	**18**	27	**36**	ns
Resistor Range	R_{SET} = R_{min} to R_{max}	0.30		33	kΩ
OUTPUT ONE-SHOT SPECIFICATIONS					
Resistor Scaling[1]			One-Shot Pulse ≈ 3 + 5 × R_{SET}		ns
Pulse Duration	R_{SET} = 4 kΩ	**17**	23	**31**	ns
	R_{SET} = 10 kΩ	**40**	53	**72**	ns
Resistor Range	R_{SET} = R_{min} to R_{max}	0.60		33	kΩ
EXTERNAL LOGIC SPECIFICATIONS[2]					
Output Logic "1"		−0.98	−0.85	−0.81	V
Output Logic "0"		−1.95	−1.85	−1.63	V
Rise Time			1.4		ns
Fall Time			1.2		ns
DATA THROUGHPUT SPECIFICATIONS					
Propagation Delay[3]	Differentiator Input to 10% of Data Output		6.0		ns
Additional Pulse Pairing[4]	200 mV Overdrive 5 ns Input Rise Time		100	1000	ps
Max Transfer Rate		50			Mb/s
POWER SUPPLY REQUIREMENTS					
Operating Range V_{CC}		+4.5		+5.5	V
Operating Range V_{EE}		−4.68		−5.72	V
Quiescent Current	T_{min} to T_{max}				
I_{CC}		**12**	16	**30**	mA
I_{EE}		**−40**	−55	**−80**	mA

NOTES
[1]R_{SET} specified in kΩ.
[2]Logic specifications obtained for the "Data +" and "Data −" outputs using 50 Ω pull down to −2.0 volts.
[3]Propagation delay is measured from the zero crossing comparator input to the "Data +" output with 200 mV overdrive.
[4]Measurements were performed using a ±100 mV square wave having a rise time under 5 ns; this was applied to the input of the zero crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.

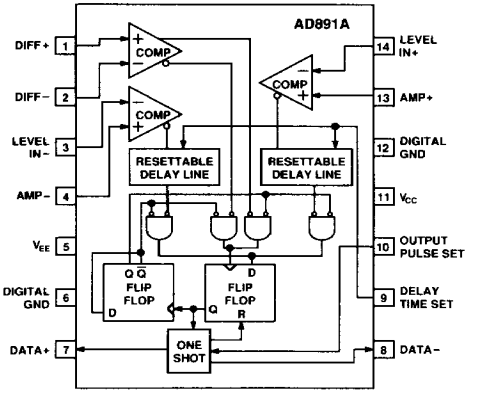
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±7.5 V
Comparator Differential Input Voltage . . . . . ±5.6 V
Storage Temperature Range P, Q . . . . . −65°C to +150°C
Operating Temperature Range[2]
AD891AJP, AD891AJD . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

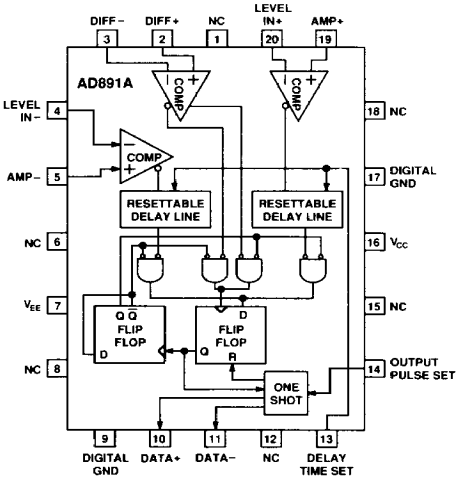
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]20-pin PLCC package: θ_{JC} = 70°C/Watt;
14-pin side brazed package (samples only): θ_{JA} = 105°C/Watt.

PIN CONFIGURATIONS

14-Pin Side Brazed Package (D)



20-Pin PLCC Package (P)



ORDERING GUIDE*

Model	Package	Package Option
AD891AJP	20-Pin PLCC	P-20A
AD891AJD	14-Pin Side Brazed (Samples Only)	D-14

*See Section 20 for package outline information.

Typical Characteristics (@ +25°C with +5 V, −5.2 V Supplies)

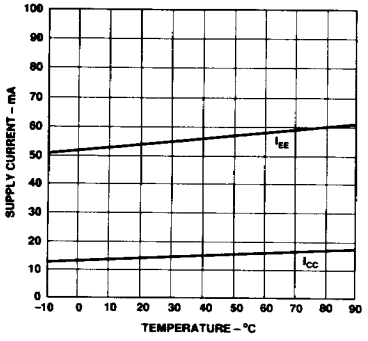


Figure 1. Supply Current vs. Temperature

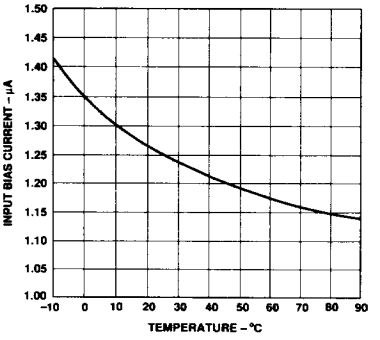


Figure 2. Comparator Input Bias Current vs. Temperature

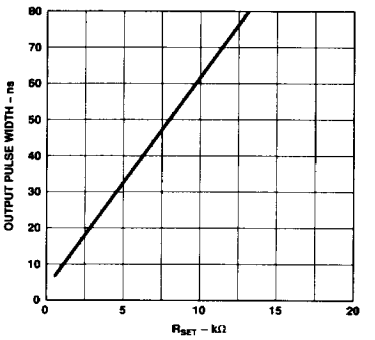


Figure 3. Output One-Shot Pulse Width vs. R_{SET}

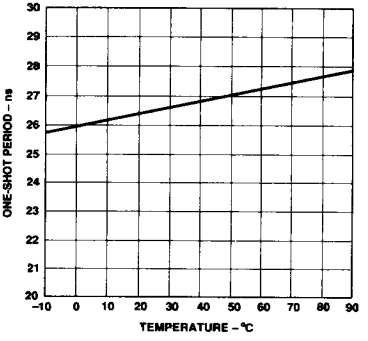


Figure 4. Output One-Shot Pulse Width vs. Temperature (R_{SET} = 4 kΩ)

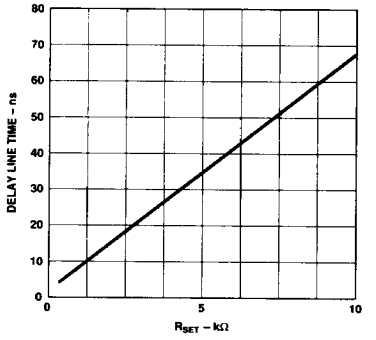


Figure 5. Delay-Line Time vs. R_{SET}

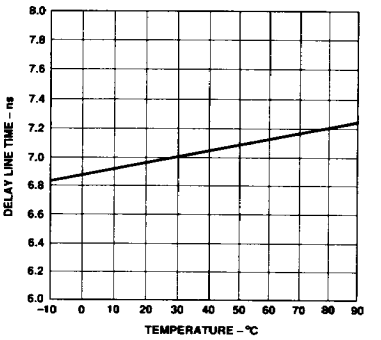


Figure 6. Delay-Line Time vs. Temperature (R_{SET} = 1 kΩ)

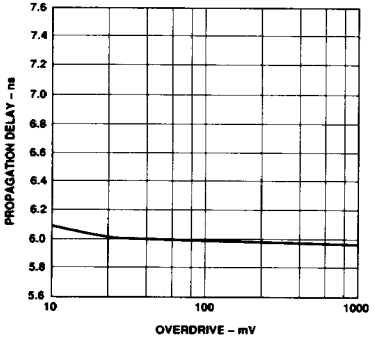


Figure 7. Propagation Delay (Comparator to Data Out) vs. Input Overdrive

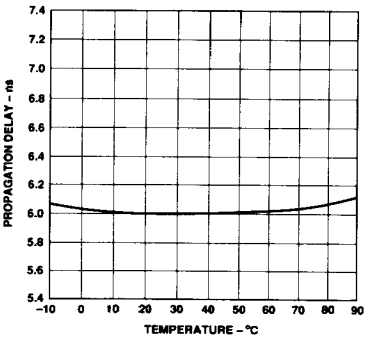


Figure 8. Propagation Delay (Comparator to Data Out) vs. Temperature

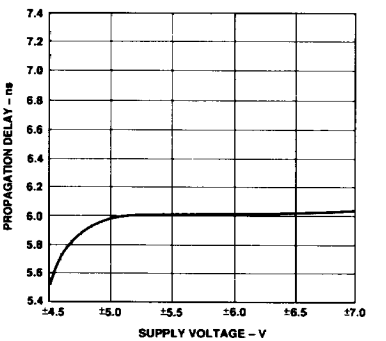


Figure 9. Propagation Delay (Comparator to Data Out) vs. Power Supply Voltage

THEORY OF OPERATION

The AD891A consists of three comparators, a pair of externally adjustable "resettable" delay-lines, four NAND gates, two D-type flip-flops, an internal bandgap reference and an externally adjustable one-shot (refer to the AD891A block diagram).

Figure 10 illustrates the operation of the AD891A, using the recommended passive delay-line/differentiator described in the following section. Sequence "A" represents the pattern written on the disk, where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD891A consists of a sequence of alternating pulses "B." The data pattern shown is for worst case RLL 1–7 code input. The AD891A requires that the analog data input pass three criteria in order to qualify a signal and produce an output bit. The triple data qualification requirement significantly reduces errors by ensuring that noise will not be misinterpreted.

The first data qualification criteria is signal amplitude and is accomplished through the use of two amplitude threshold comparators. The outputs of each comparator drive a "resettable" delay-line. The "resettable" delay-line implements the second valid-data criteria: minimum time above valid-signal threshold before a zero-crossing can be detected. The minimum time above valid-signal threshold is set through an external resistor. The output of the "resettable" delay-line is then used to determine if the data exhibits the correct polarity, the third data qualification criteria. To determine if the data exhibits the correct polarity, a D-type flip-flop is used. The flip-flop is toggled with each valid data pulse, thereby, ensuring an alternate polarity qualification for each valid incoming data bit.

"C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock an internal D-type flip-flop. The flip-flop is enabled using the output from the data polarity check, such that the flip-flop output changes state only when all three of the data qualification criteria, described earlier, have been satisfied. If all three data qualification criteria were met, and a zero-crossing event occurs, the flip-flop changes state, producing an output pulse "E." The duration of this pulse, seen at the Data +/Data – outputs, is set using an external resistor. The one-shot also triggers the second D-type flip-flop, toggling the required valid-data polarity. The final output data sequence is shown in "F." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a reconstructed version of the write data.

Since the 1–7 code input is the most demanding of the popular encoding schemes to qualify, the AD891A easily handles such other codes as MFM and RLL 2–7.

9

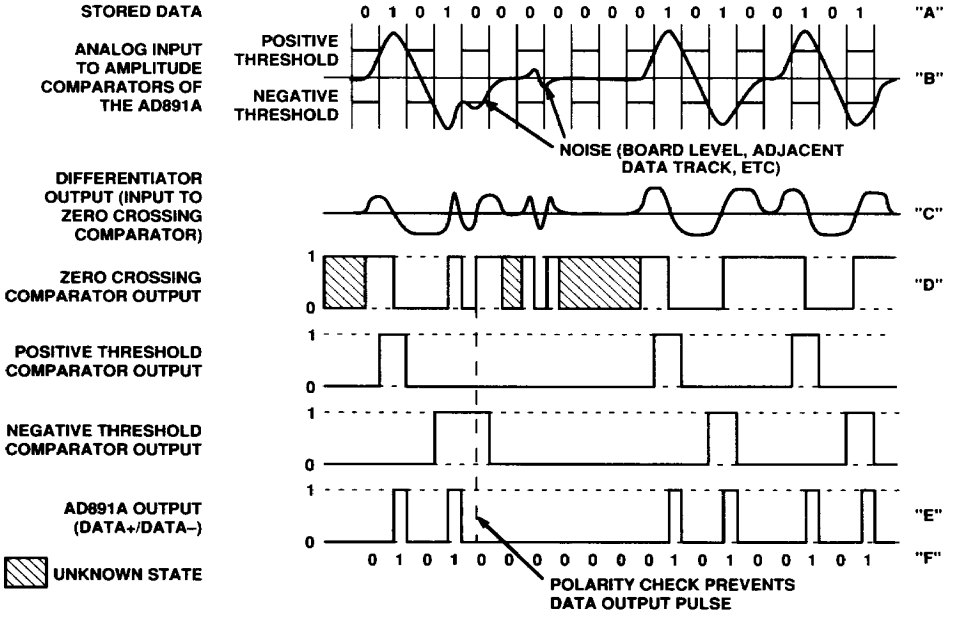


Figure 10. AD891A Operation for Worst Case 1–7 RLL Code

DESIGN CONSIDERATIONS

In designing a suitable passive delay-line differentiator, either the fully differential (Figure 11a) or single-ended (Figure 11b) configuration can be used. The equations governing component selection for both connections are as shown.

If the single-ended configuration is employed, then the inputs to the negative half-cycle comparator need to be biased such that the comparator is turned off. This can be accomplished by placing the "Amp −" input at a potential at least 100 mV more negative than the "Level In −" input. The "Amp −" pin may be connected to the "V_{EE}" pin and the "Level In −" pin may be connected to the "Digital GND" pin, provided that the potential difference does not exceed 5.6 volts, which is the absolute maximum differential input rating of the device.

Good RF layout practice should be obeyed, with decoupling networks of 0.1 μF in parallel with 0.01 μF at both the "V_{CC}" and "V_{EE}" pins. A ground plane should be used extensively. Two digital grounds are supplied: Pin 17 is for the internal logic while Pin 9 is provided for the "Data" outputs only. (These pins are for the PLCC package; the corresponding Side Braze package pins are 12 and 5, respectively.) The "resettable" delay-line and output pulse setting resistors should be tied, as directly as possible, to the "V_{EE}" pin.

The "Data −" and "Data +" pins require pull-down resistors to "V_{EE}" as per normal practice in ECL. The use of a 4 kΩ resistors connected between the "Output Pulse Set" pin and "V_{EE}" will produce a nominal 23 ns one-shot pulse width; 10 kΩ resistors will nominally produce 53 ns one-shot pulse width. A 7 ns minimum time above threshold qualification may be implemented with a 1 kΩ resistor connected between the "Delay Set" pin and "V_{EE}."

For best performance, the three input comparators should be operated at a common mode potential close to digital ground. The digital ground should be connected to the analog ground as near to the power supply as possible, to minimize noise injection.

INTEGRATING WITH THE AD890 WIDEBAND CHANNEL PROCESSING ELEMENT

Figure 12 shows a typical application using the AD891AJP and AD890JP connected together to create a 30 MHz channel. This circuit includes a 5-pole 30 MHz gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. The fully differential passive delay-line differentiator previously discussed is also included. The analog and digital grounds should be connected only to the power supply common.

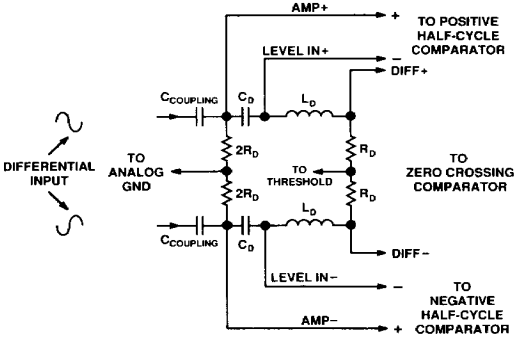


Figure 11a. Fully Differential Configuration of Passive Delay-Line Differentiator

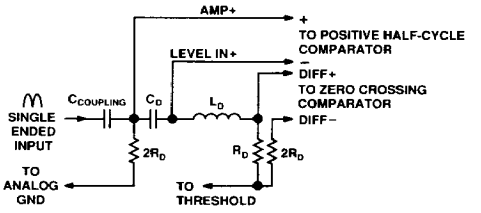


Figure 11b. Single-Ended Configuration of Passive Delay-Line Differentiator

RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

f_D = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

R_D Minimum Value: 120 Ω
150 Ω or Greater is Recommended

1.3 (Best Magnitude Response) ≤K ≤1.7 (Best Group Delay Response)

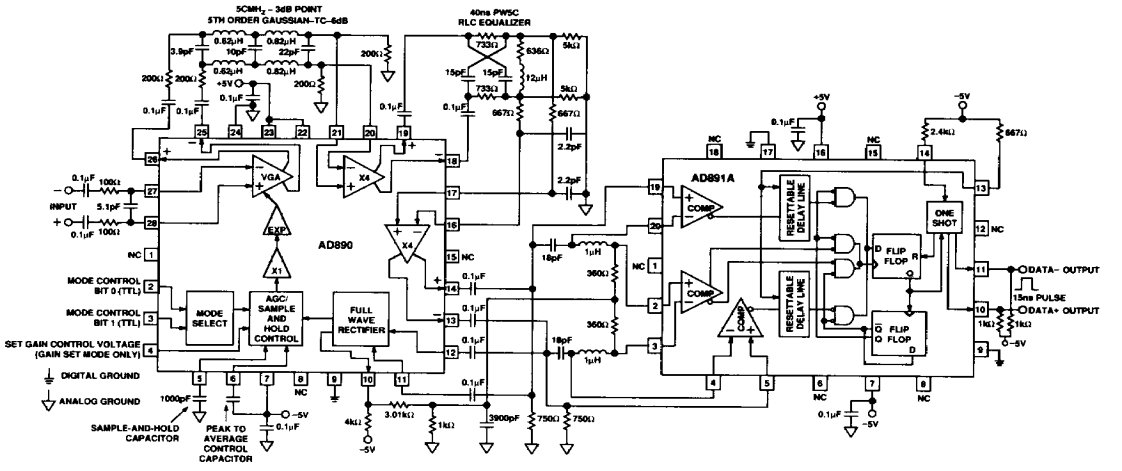


Figure 12. Typical AD890/AD891A Connection for a 30 MHz Channel

9

OPERATION WITH +5 V, +12 V SUPPLIES

Operation with +5 V (±0.5 V) and +12 V (±0.6 V) supplies is readily achieved. The digital ground pins must be connected to the +5 V line. The specified output ECL logic levels are therefore referred to the +5 V supply. Pull-down resistors for the "Data +" and "Data −" pins should be connected to "V_{EE}." Thus connected, a current of approximately 23 mA will flow in the +5 V supply under normal operation.

In order to ensure correct comparator operation, a pair of 100 mA diodes should be added in series with the +12 V supply which is connected to the "V_{CC}" terminal. This connection is shown in Figure 13 (shown for PLCC package).

Both the +5 V and +12 V supplies should be RF bypassed to ground; the values of 0.1 μF and 0.01 μF in parallel are recommended. In addition, some higher value of decoupling capacitance – such as 3.3 μF – may be desirable. This decoupling should be applied directly at the AD891A "V_{CC}" and "Digital GND" pins. Finally, the common mode range for the comparators is now referred to the +5 V supply line and care must be taken to operate within the common mode limits.

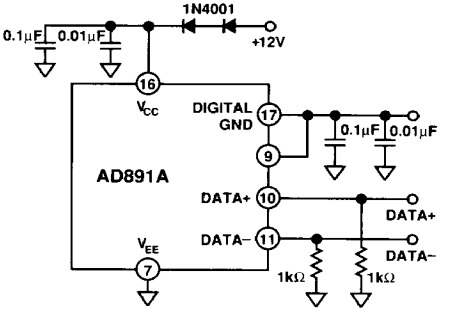


Figure 13. AD891AJP Connection for +5 V, +12 V Operation (+12 V ±5%, +5 V ±10%)

RESPONSE CHARACTERISTICS OF THE FULLY DIFFERENTIAL DELAY-LINE DIFFERENTIATOR

Figures 14 through 17 show typical performance to be expected from the recommended passive, fully differential, delay-line differentiator previously discussed. Figures 14 and 15 depict magnitude and phase response for the undifferentiated output, respectively. Figure 16 shows magnitude response for the differentiated output, and Figure 17 shows phase error between the two outputs.

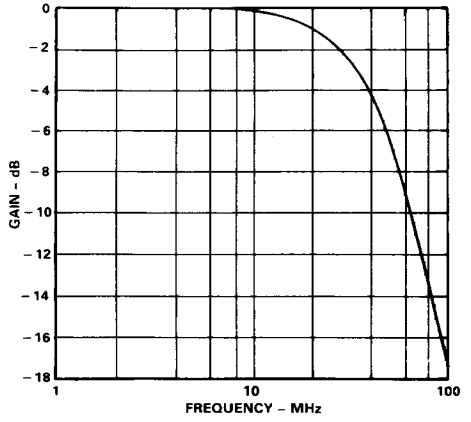


Figure 14. Magnitude Response of Undifferentiated Output

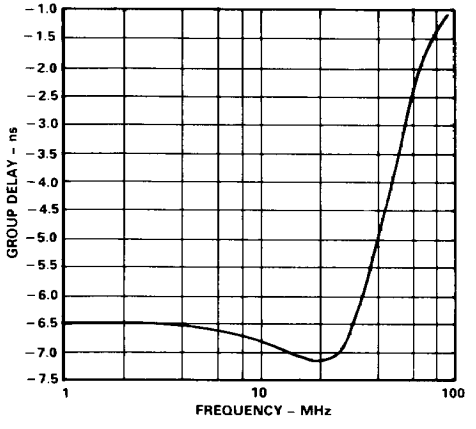


Figure 15. Group Delay Characteristics of Undifferentiated Output

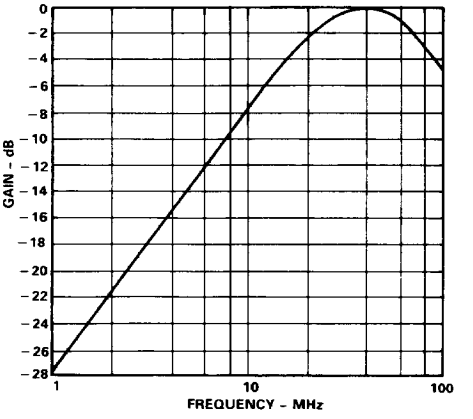


Figure 16. Magnitude Response of Differentiated Output

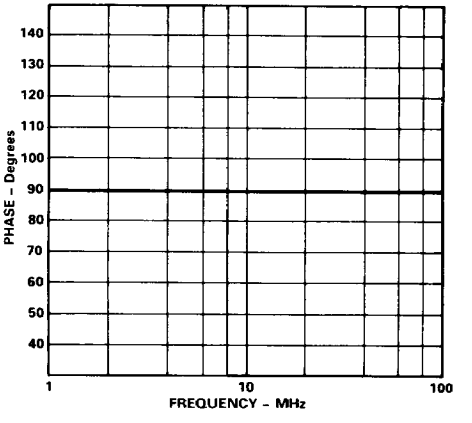


Figure 17. Relative Phase Between Differentiated and Undifferentiated Outputs