REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added burn-in condition C to 4.2.a.1 and 4.3.2.b.1. Device types 03 and 04 inactive for new design. Not available from an approved source. Editorial changes throughout.	90-07-03	W. Heckman
B	Added burn-in condition A to 4.2.a.1 and 4.3.2.b.1.	91-11-14	M. Poelking
C	Added device types 05 and 06. Editorial changes throughout.	92-12-11	M. Poelking

REV																			
SHEET																			
REV	C	C																	
SHEET	15	16																	

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

SC N/A

PREPARED BY
Tim H. Noh

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
87-12-02

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, HIGH PERFORMANCE CMOS 9-WIDE AND 10-WIDE BUS INTERFACE REGISTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88516
A	67268	

SHEET 1 OF 16

DESC FORM 193
JUL 91

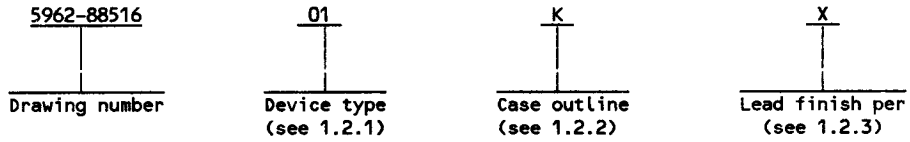
5962-E584-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number. The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29C821	High performance CMOS 10-wide bus interface register
02	29C823	High performance CMOS 9-wide bus interface register
03	29C921	High performance CMOS 10-wide bus interface register (rotated die) 1/
04	29C923	High performance CMOS 9-wide bus interface register (rotated die) 1/
05	29C821A	High performance CMOS 10-wide bus interface register (edge-rate controlled outputs)
06	29C823A	High performance CMOS 9-wide bus interface register (edge-rate controlled outputs)

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or GDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
3	CQCC1-N28	28	square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Not available from an approved source of supply.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
DC input voltage range	
Devices 01-04	-0.5 V dc to V_{CC} +0.5 V dc
Devices 05,06	-0.5 V dc to +6.0 V dc
DC output voltage range	
Devices 01-04	-0.5 V dc to V_{CC} + 0.5 V dc
Devices 05,06	-0.5 V dc to +6.0 V dc
DC output diode current: Into output	
All devices	+50 mA
DC output diode current: Out of output	
All devices	-50 mA
DC input diode current: Into input	
All devices	+20 mA
DC input diode current: Out of input	
All devices	-20 mA
DC output current per pin (I_{sink})	
Devices 01-04	+48 mA (2 x I_{OL})
Devices 05,06	+100 mA
DC output current per pin (I_{source})	
Devices 01-04	-30 mA (2 x I_{OH})
Devices 05,06	-100 mA
Total dc ground current	(n x I_{OL} + m x I_{CCT}) mA 1/
Total dc V_{CC} current	(n x I_{OH} + m x I_{CCT}) mA 1/
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases L, K and 3	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc

1/ n = number of outputs, m = number of inputs.

2/ For T_A = +100°C to +125°C derate linearly at 10 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY
MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -15.0 mA V_{IN} = V_{IL}, V_{IH}		1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IN} = V_{IL}, V_{IH}	I_{OL} = 24.0 mA	1,2,3	01-04		0.5	V
			I_{OL} = 32 mA		05,06		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1,2,3	All		-1.2	V
Low level input current	I_{IL1}	V_{CC} = 5.5 V	V_{IN} = 0 V	1,2,3	01-04		-10	µA
					05,06		-5	µA
	I_{IL2}		V_{IN} = 0.4 V		01-04		-5	µA
High level input current	I_{IH1}	V_{CC} = 5.5 V	V_{IN} = 2.7 V	1,2,3	01-04		5	µA
	I_{IH2}		V_{IN} = 5.5 V	1,2,3	01-04		10	µA
					05,06		5	µA
Off state current	I_{OZH}	V_{CC} = 5.5 V	V_{OUT} = 5.5 V	1,2,3	All		10	µA
	I_{OZL}		V_{OUT} = 0.0 V	1,2,3	All		-10	µA
Output short circuit current	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0 V 1/		1,2,3	All	-60		mA
Static supply current	I_{CCQ}	V_{CC} = 5.5 V, outputs open	V_{IN} = 5.5 V or GND	1,2,3	01-04		160	µA
					05,06		1500	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Static supply current	I_{CCT}	V_{CC} = 5.5 V, outputs open; V_{IN} = 3.4 V; Data input		All		1.5	mA/bit
		V_{CC} = 5.5 V, outputs open; V_{IN} = 3.4 V; $\overline{OE}$, CP		01,03, 05		3.0	mA/bit
		V_{CC} = 5.5 V, outputs open; V_{IN} = 3.4 V; $\overline{OE}$, $\overline{EN}$, $\overline{CLR}$, CP		02,04, 06		3.0	mA/bit
Input capacitance	C_{IN}	See 4.3.1c	4	All		16	pF
Output capacitance	C_{OUT}	See 4.3.1c	4	All		20	pF
Functional testing		See 4.3.1d	7,8	All			
Propagation delay clock (CP) to Y_I	t_{PLH}	See figure 4 C_L = 50 pF R_1 = 500 ohms R_2 = 500 ohms	9,10,11	01-04		14	ns
				05,06		9.5	ns
Propagation delay clock (CP) to Y_I	t_{PHL}		9,10,11	01-04		14	ns
				05,06		9.5	ns
Propagation delay clear to Y_I	t_{PHL}		9,10,11	02,04		15	ns
				06		10.5	ns
Propagation delay output enable (OE) to Y_I	t_{PZH}		9,10,11	01-04		14	ns
				05,06		9	ns
Propagation delay output enable (OE) to Y_I	t_{PZL}		9,10,11	01-04		14	ns
				05,06		13	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay output disable (OE) to Y_I	t_{PHZ}	See figure 4 C_L = 50 pF R_1 = 500 ohms R_2 = 500 ohms	9,10,11	01-04		14	ns
				05,06		8.5	ns
Propagation delay output disable (OE) to Y_I	t_{PLZ}		9,10,11	01-04		14	ns
				05,06		8.5	ns
Data (D_I) to CP setup time	t_S		9,10,11	01-04	6		ns
				05,06	3		ns
Data (D_I) to CP hold time	t_H		9,10,11	01-04	3		ns
				05,06	2		ns
Enable (high to low) to CP setup	t_S		9,10,11	02,04	6		ns
				06	4		ns
Enable (low to high) to CP setup time	t_S		9,10,11	02,04	6		ns
				06	4		ns
Enable hold time	t_H		9,10,11	02,04	3		ns
				06	0		ns
Clear (low to high) to CP setup time	t_S		9,10,11	02,04	6		ns
	t_{REC}			06	6		ns
Clock low pulse width	t_{PWL}		9,10,11	01-04	11		ns
				05,06	6		ns

See footnote at end of table.

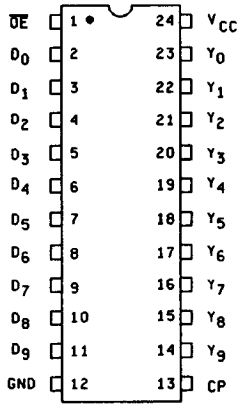
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock high pulse	t_{PWH}		9,10,11	01-04	11		ns
				05,06	6		ns
Clear pulse width	t_{PWL}		9,10,11	02,04	11		ns
				06	6		ns

1/ Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.

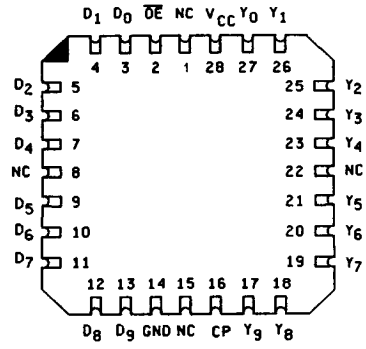
Device types 01 and 05

Cases K and L



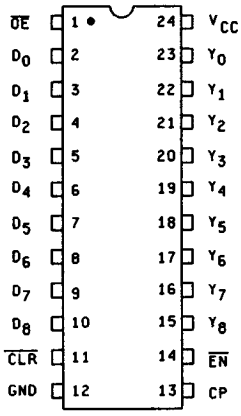
Device types 01 and 05

Case 3



Device types 02 and 06

Cases K and L



Device types 02 and 06

Case 3

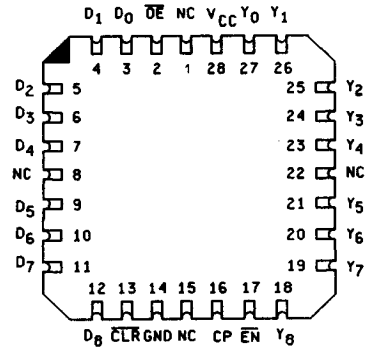
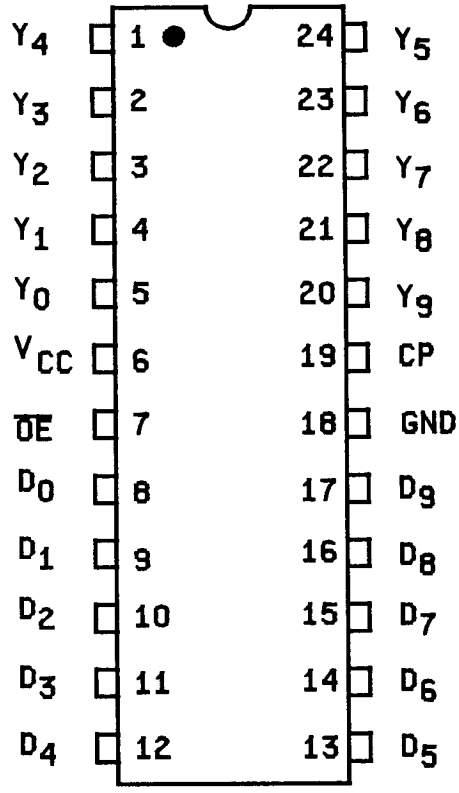


FIGURE 1. Terminal connections.

Device type 03

Case L



Device type 04

Case L

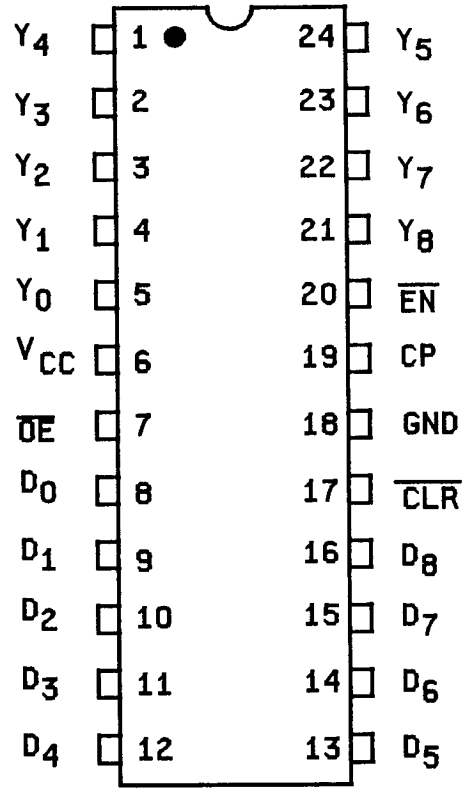


FIGURE 1. Terminal connections - Continued.

Device types 01, 03, and 05

Inputs			Internal	Outputs	Function
$\overline{OE}$	D_i	CP	$\overline{Q}_i$	Y_i	
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

Device types 02, 04, and 06

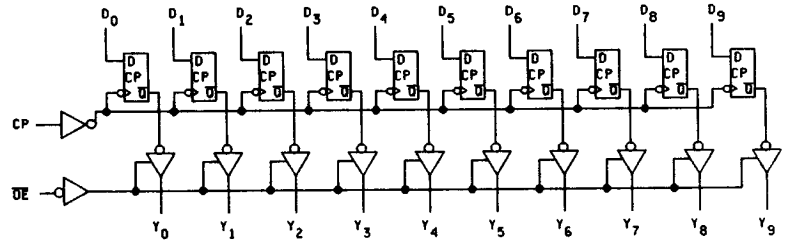
Inputs					Internal	Outputs	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i	
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

H = High
L = Low
X = Don't care

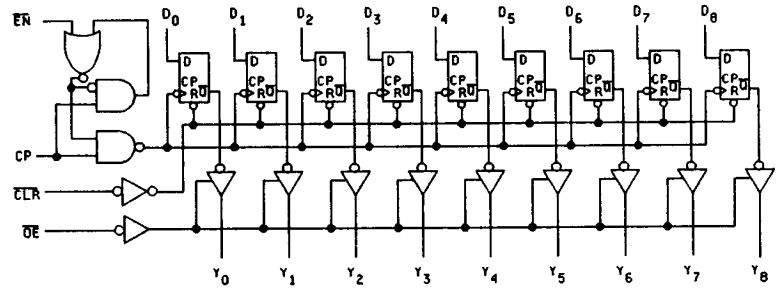
NC = No change
↑ = Low-to-high transition
Z = High impedance

FIGURE 2. Truth tables.

Device types 01, 03, and 05



Device types 02 and 04



Device type 06

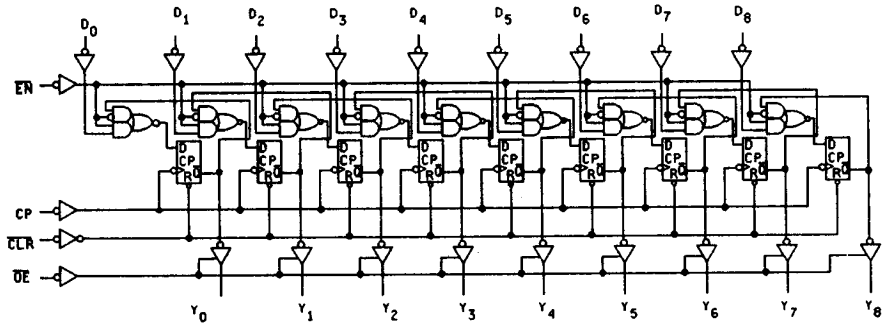
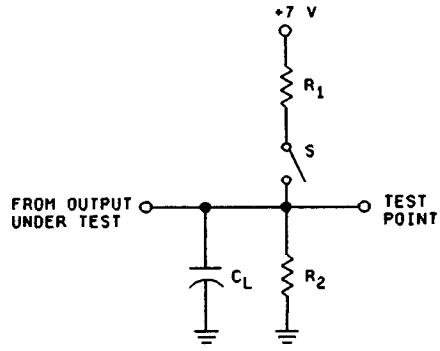


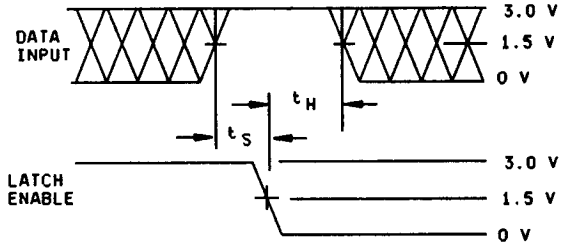
FIGURE 3. Logic diagrams.



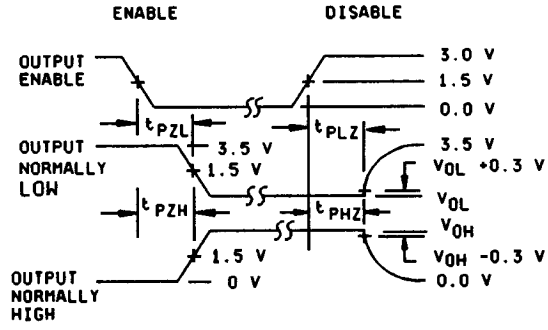
Load circuit for three-state outputs

Parameter	S Position
t_{PLH}	Open
t_{PHL}	Open
t_{PHZ}	Open
t_{PZH}	Open
t_{PLZ}	Closed
t_{PZL}	Closed

Setup and hold times

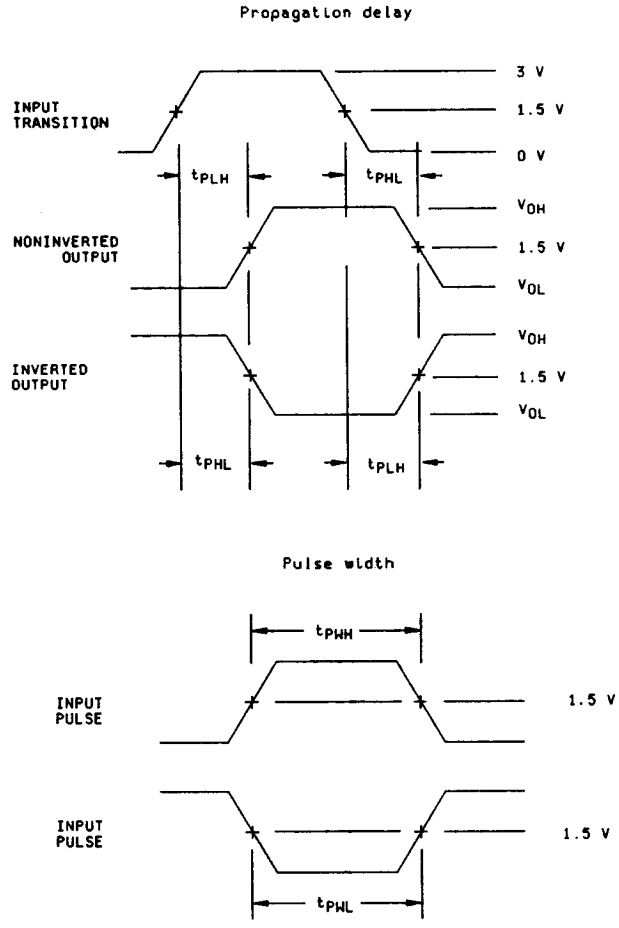


Enable and disable times



NOTES:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

FIGURE 4. Test circuit and switching waveforms.



NOTE: Pulse generator for all pulses rate ≤ 1.0 MHz; Z_O = 50Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

FIGURE 4. Test circuit and switching waveforms - Continued.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accodance with 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5004)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.