REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, change t_{OD2}. Editorial changes throughout.	1988 NOV 7	M. A. Frye

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV	A		A		A																			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY: M. A. Frye

DRAWING APPROVAL DATE: 15 APRIL 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL BIPOLAR 8-BIT I/O PORT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-86851

SHEET 1 OF 19

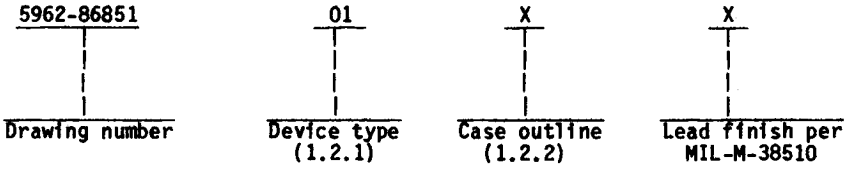
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8X376	Programmable addressable bidirectional asynchronous I/O port

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-11 (24-lead, 1.250" x .410" x .225") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range 1/	+7.0 V dc maximum
Input voltage	+5.5 V dc maximum
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	.825 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	
Case X	(See MIL-M-38510, appendix C)
Junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc

1/ Not applicable during address programming.

2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ Unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
High level input voltage 2/	V_{IH}		1,2,3	2.0		V
Low level input voltage 2/	V_{IL}		1,2,3		0.8	V
Input clamp voltage	V_{IC}	V_{CC} = minimum; I_{IN} = -10 mA	1,2,3		-1.5	V
High level input current 3/	I_{IH}	V_{CC} = maximum; V_{IH} = 2.7 V	1,2,3		100	µA
Low level input current 3/	I_{IL}	V_{CC} = maximum; V_{IL} = 0.5 V	1,2,3		-550	µA
Low level output voltage IV bus ($\overline{IV0}$-$\overline{IV7}$) user bus (UD0-UD7)	V_{OL}	V_{CC} = minimum; I_{OL} = 16 mA V_{CC} = minimum; I_{OL} = 24 mA	1,2,3		0.55 0.55	V
High level ouput voltage	V_{OH}	V_{CC} = minimum; I_{OH} = -3.2 mA	1,2,3	2.4		V
Short circuit output current IV bus ($\overline{IV0}$-$\overline{IV7}$) 4/ user bus (UD0-UD7)	I_{OS}	V_{CC} = maximum	1,2,3	-20 -10		mA
Supply current	I_{CC}	V_{CC} = maximum; $\overline{ME}$ = $\overline{UOC}$ = V_{CC}	1,2,3		150	mA
Functional test		see 4.3.1c	7			
Pulse width clock high	t_{W1}		9,10,11	30		ns
Pulse width user input control	t_{W2}	MCLK = high	9,10,11	35		ns
Propagation delay, UD to TV	t_{PD1}	MCLK = high SC = WC = $\overline{ME}$ = $\overline{UIC}$ = low	9,10,11		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ Unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay, ↓ $\overline{UIC}$ to $\overline{IV}$	t_{PD2}	UD = stable; MCLK = high SC = WC = $\overline{ME}$ = low	9,10,11		55	ns
Propagation delay, $\overline{IV}$ to UD	t_{PD3}	MCLK = WC = $\overline{UIC}$ = high $\overline{ME}$ = $\overline{UOC}$ = SC = low	9,10,11		45	ns
Propagation delay, ↑ MCLK to UD	t_{PD4}	WC = $\overline{UIC}$ = high; $\overline{IV}$ = stable $\overline{ME}$ = $\overline{UOC}$ = SC = low	9,10,11		55	ns
UD output enable time ↓ UOC to UD	t_{OE1}	$\overline{UIC}$ = high	9,10,11		45	ns
UD input recovery time 5/ ↑ $\overline{UIC}$ to UD	t_{OE2}	$\overline{UOC}$ = low	9,10,11		45	ns
$\overline{IV}$ data master enable ↓ $\overline{ME}$ to $\overline{IV}$	t_{OE3}	WC = SC = low	9,10,11		45	ns
$\overline{IV}$ data write recovery ↓ WC to $\overline{IV}$	t_{OE4}	SC = $\overline{ME}$ = low	9,10,11		45	ns
$\overline{IV}$ data select recovery ↓ SC to $\overline{IV}$	t_{OE5}	SC = $\overline{ME}$ = low	9,10,11		45	ns
UD output disable ↑ $\overline{UOC}$ to UD	t_{OD1}	$\overline{UIC}$ = high	9,10,11		40	ns
UD input override ↓ $\overline{UIC}$ to UD	t_{OD2}	$\overline{UOC}$ = low	9,10,11		55	ns
$\overline{IV}$ data master disable 6/ ↑ $\overline{ME}$ to $\overline{IV}$	t_{OD3}	WC = SC = low	9,10,11		40	ns
$\overline{IV}$ data write override 6/ ↑ WC to $\overline{IV}$	t_{OD4}	SC = $\overline{ME}$ = low	9,10,11		40	ns
$\overline{IV}$ data select override 6/ ↑ SC to $\overline{IV}$	t_{OD5}	WC = $\overline{ME}$ = low	9,10,11		40	ns
UD control setup time UD to ↑ $\overline{UIC}$	t_{S1}	MCLK = high	9,10,11	25		ns
$\overline{IV}$ data setup time $\overline{IV}$ to ↓ MCLK	t_{S2}	WC = high or SC = high; $\overline{ME}$ = low; $\overline{UIC}$ = high	9,10,11	15		ns

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ Unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{IV}$ master enable setup time 7/ ↓ $\overline{ME}$ to ↓ MCLK	t_{S3}	WC = high or SC = high; $\overline{UIC}$ = high	9,10,11	20		ns
$\overline{IV}$ write control setup time ↑ WC to ↓ MCLK	t_{S4}	SC = $\overline{ME}$ = low; $\overline{UIC}$ = high	9,10,11	40		ns
$\overline{IV}$ select control setup time ↑ SC to ↓ MCLK	t_{S5}	WC = $\overline{ME}$ = low	9,10,11	30		ns
UD control hold time ↑ $\overline{UIC}$ to UD	t_{H1}	MCLK = high	9,10,11	10		ns
$\overline{IV}$ data hold time ↓ MCLK to $\overline{IV}$	t_{H2}	WC = high or SC = high; $\overline{ME}$ = low; $\overline{UIC}$ = high	9 10,11	5 20		ns
$\overline{IV}$ master enable hold time 8/ ↓ MCLK to ↑ $\overline{ME}$	t_{H3}	WC = high or SC = high; $\overline{UIC}$ = high	9,10,11	0		ns
$\overline{IV}$ write control hold time ↓ MCLK to ↓ WC	t_{H4}	SC = $\overline{ME}$ = low; $\overline{UIC}$ = high	9,10,11	0		ns
$\overline{IV}$ select control hold time ↓ MCLK to ↓ SC	t_{H5}	WC = $\overline{ME}$ = low	9,10,11	0		ns

1/ See waveforms and test conditions on figure 4. All measurements to the $\overline{IV}$ bus assumes the address selection latch is set.
2/ Guaranteed if not tested to the specified limits.
3/ The input current includes the three-state leakage current of the output driver on the data lines.
4/ Only one output may be shorted at a time.
5/ Recovery time is defined as the delay required to insure $\overline{IV}$ bus has priority after $\overline{UIC}$ goes high.
6/ These parameters are measured with a capacitive loading of 50 pF and represent the output driver turn-off time.
7/ If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.
8/ These limits do not apply during address programming.

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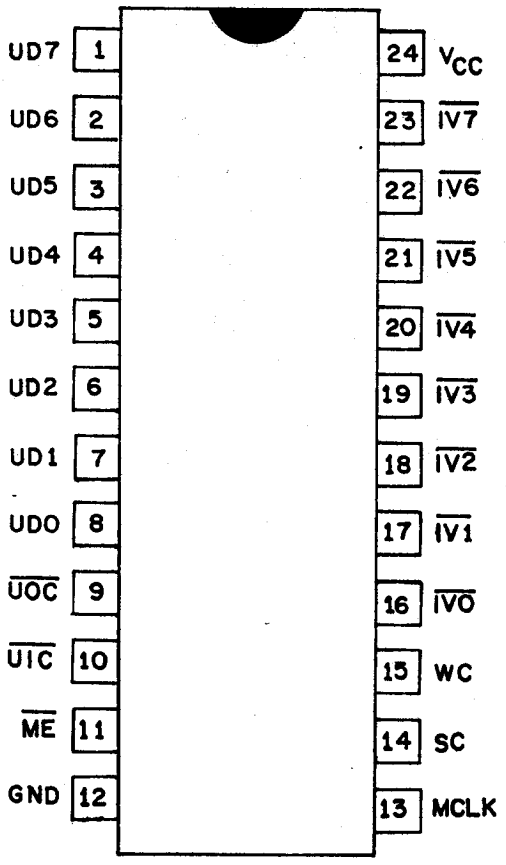

FIGURE 1. Terminal connections (top view).

Pin number	Identifier	Function
1-8	UD7-UD0	Three-state bidirectional user data (UD) bus; UD0 corresponds to $\overline{IV0}$
9	$\overline{UOC}$	User output control - active low input to enable data output to UD0-UD7.
10	$\overline{UIC}$	User input control - active low input to enable data input from UD0-UD7.
11	$\overline{ME}$	Master enable - active low input to enable the $\overline{IV}$ bus for data input, data output, or $\overline{IV}$ address selection/ deselection: UD-bus operations are unaffected.
12	GND	Ground.
13	MCLK	Master clock - active high input from microcontroller used to strobe data into data latches from the $\overline{IV}$ bus and, for the synchronous 8X372, from the UD bus; MCLK also synchronizes $\overline{IV}$ address selection
14	SC	Select command - active high input from microcontroller to enable $\overline{IV}$ address input from the $\overline{IV}$ bus for device selection.
15	WC	Write command - active high input from microcontroller to enable the writing of data into the data latches from the $\overline{IV}$ bus, provided $\overline{UIC}$ is not low.
16-23	$\overline{IV0}$-$\overline{IV7}$	Interface vector (input/output bus) - three-state, bidirectional, microcontroller data bus; $\overline{IV0}$ corresponds to UD0.
24	V_{CC}	+5 V power supply.

FIGURE 1. Terminal connections (top view) - Continued.

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Input/output control of UD bus

$\overline{UIC}$	$\overline{UOC}$	MCLK	Function of UD bus
H	L	X	Output data
L	X	H	Input data
L	X	L	Input data
H	H	X	Inactive

NOTE: X = don't care

Input/output control of UD bus

$\overline{ME}$	SC	WC	MCLK	$\overline{UIC}$	Selection latch	Function of $\overline{IV}$ bus
L	L	L	X	X	Set	Output data
L	L	H	H	H	Set	Input data
L	H	L	H	X	X	Input address*
L	H	H	H	H	X	Input data and address*
L	H	H	H	L	X	Input address*
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not set	Inactive
H	X	X	X	X	X	Inactive

NOTE: X = don't care
* Selection latch is updated

FIGURE 2. Truth tables.

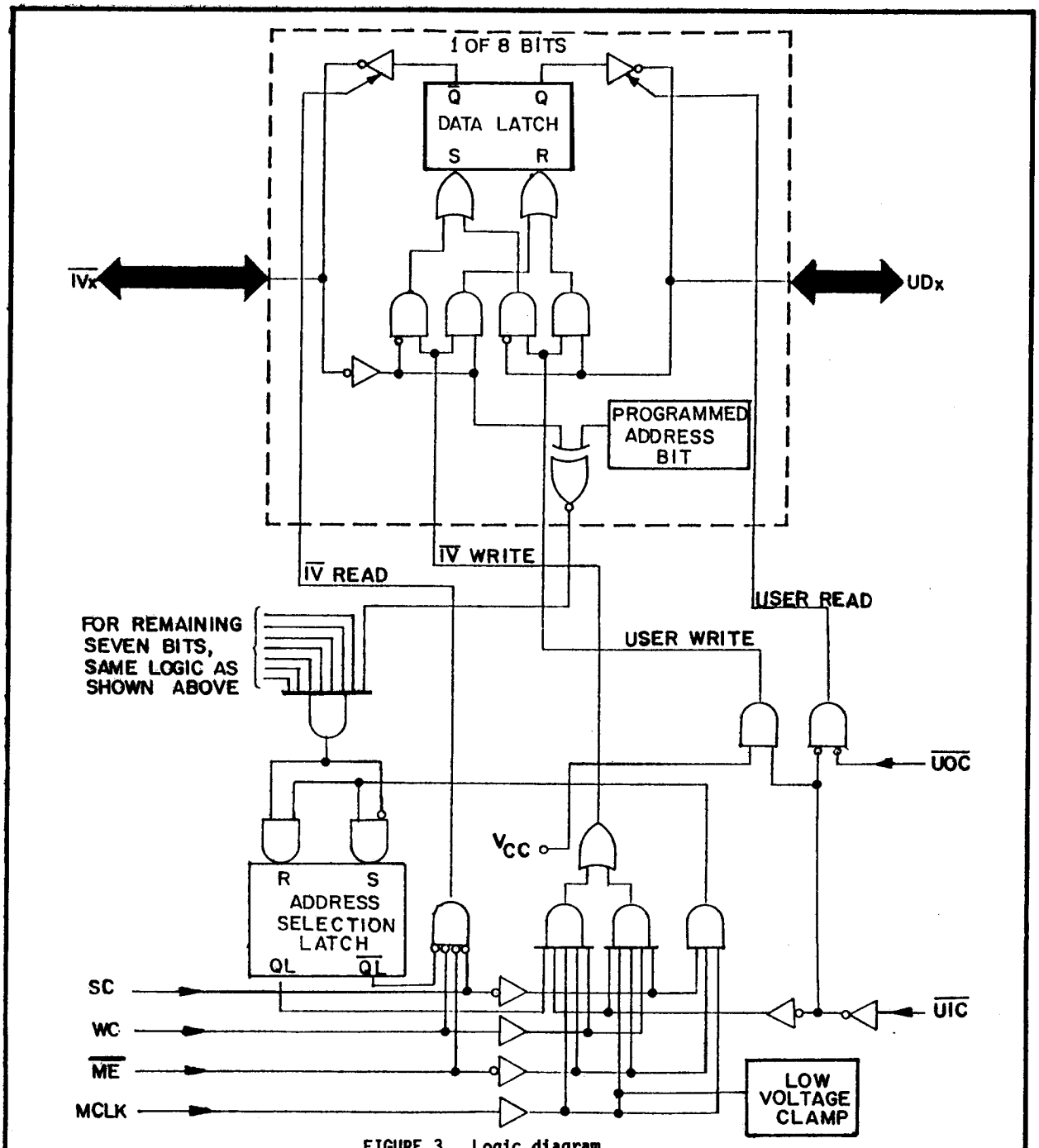

FIGURE 3. Logic diagram.

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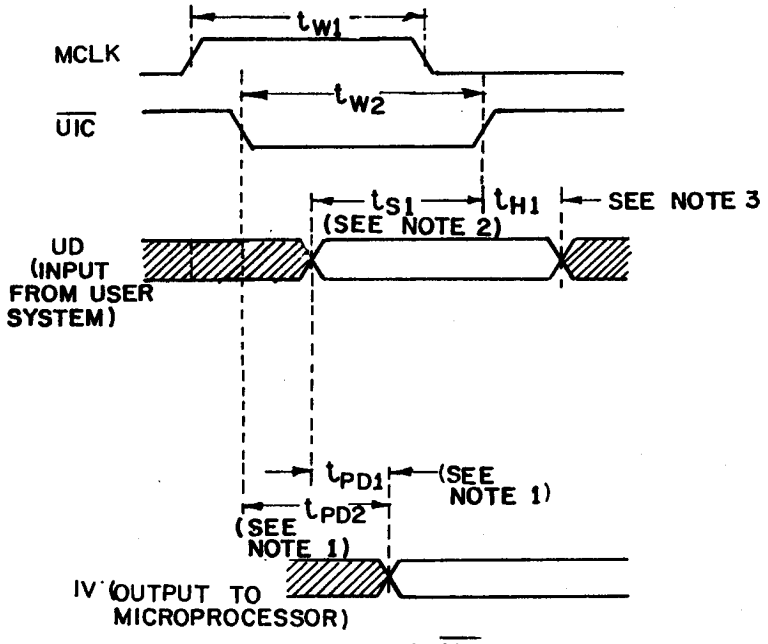


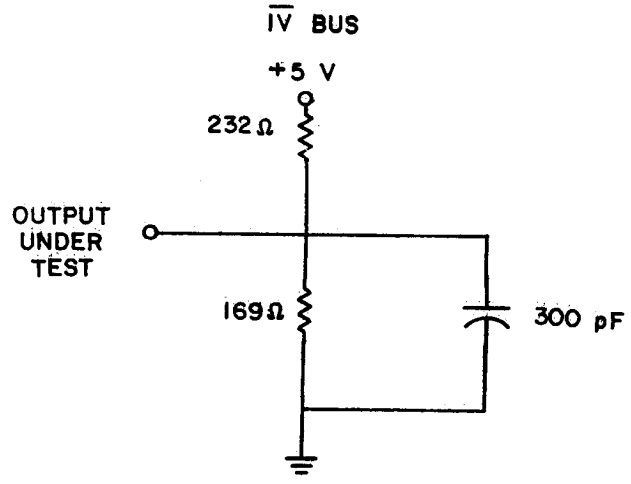
STATIC CONDITIONS: SC, WC, $\overline{ME}$ = LOW
$\overline{UOC}$ = HIGH

USER DATA INPUT TIMING

NOTES:
1. The actual time for stable data on the IV bus is the latest propagation from t_{PD1} and t_{PD2}.
2. The UD input must satisfy the setup-time requirements for t_{S1}.
3. Minimum hold-time required for the UD input is the earlier of the times specified by t_{H1}.

FIGURE 4. Waveforms and test circuits.

AC TEST LOADING CIRCUITS



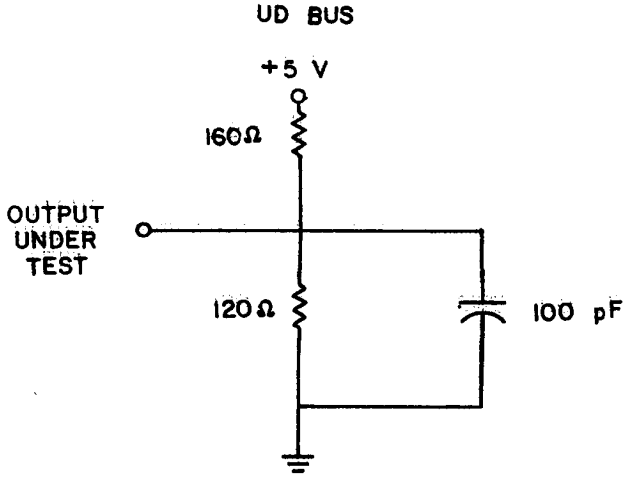
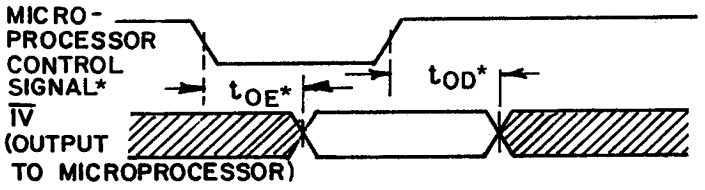


FIGURE 4. Waveforms and test circuits - Continued.



MICROCONTROLLER OUTPUT ENABLE TIMING

*Parameter key

Microprocessor control signal	AC timing parameters	Static Conditions
$\overline{ME}$	t_{OE3} t_{OD3}	SC=WC=LOW
WC	t_{OE4} t_{OD4}	SC=$\overline{ME}$=LOW
SC	t_{OE5} t_{OD5}	WC=$\overline{ME}$=LOW

FIGURE 4. Waveforms and test circuits - Continued.

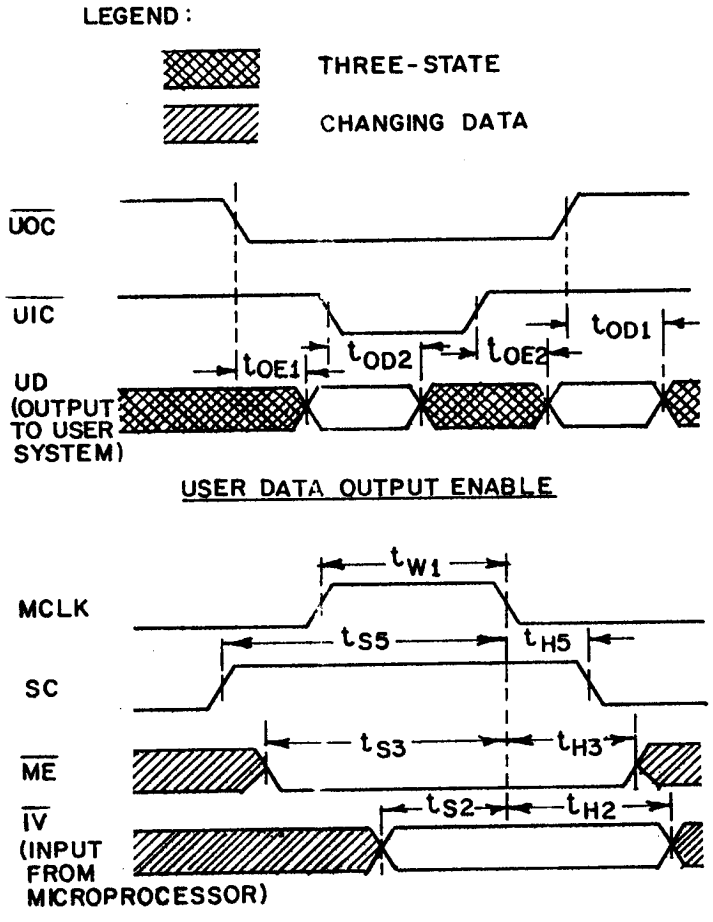
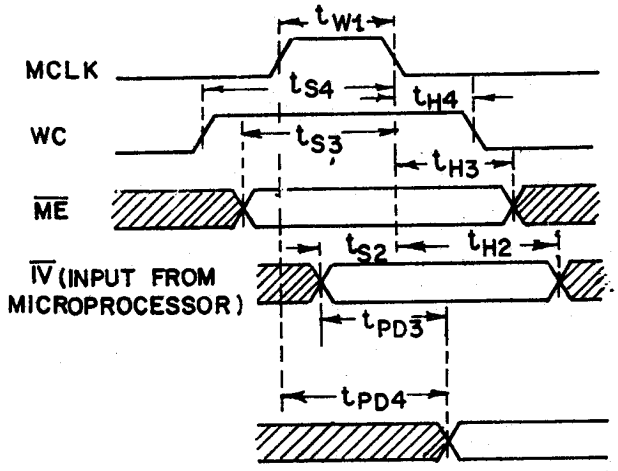


FIGURE 4. Waveforms and test circuits - Continued.



MICROCONTROLLER WRITE CYCLE TIMING

FIGURE 4. Waveforms and test circuits - Continued.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 tested sufficiently to verify the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*,2,3,9
Group A test requirements (method 5005)	1,2,3,7,9, 10,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Address programming and address protect characteristics. The device herein can be programmed to respond to any address within a range of 0_{10} through 255_{10}. In an unprogrammed state, low level (<0.8 V) inputs on all IV bus lines (address 255_{10}) will select the device. To program a given address bit to match a high level (>2.0 V) input on the corresponding IV pin (a logical 0 to the microcontroller), the counterpart UD-bus pin must be pulsed according to table III and the following procedures:

a. Set all control inputs to the inactive state. $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = V_{CC} and SC = WC = MCLK = GND; leave the UD and $\overline{IV}$ pins open.

b. Increase V_{CC} to V_{CCP}.

c. After V_{CC} has stabilized, apply a single programming pulse to the user-bus bit that corresponds to the desired high-level $\overline{IV}$ address bit. The I/O port is programmed from the user bus (UDO-UD7) for addressing from the microcontroller bus ($\overline{IV0}$-$\overline{IV7}$).

d. Return V_{CC} to 0-volts. If the programming of all address bits is completed in less than one second, V_{CC} can remain at 9.0 volts for the required interval of time.

e. Steps a through c are applicable to the programming of each address bit that requires a high-level $\overline{IV}$ match.

f. To verify that the address is properly programmed, return V_{CC} to +5.0 V, set $\overline{IV0}$-$\overline{IV7}$ to the desired (inverted) binary address pattern, set $\overline{ME}$=WC = low and SC = MCLK = high. If there are no programming errors, subsequent data written from $\overline{IV0}$-$\overline{IV7}$ (WC = high) will appear inverted on UDO-UD7.

g. To address protect set V_{CC} and all control inputs to 0 volts (V_{CC} = $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = SC = WC = MCLK = GND); $\overline{IV0}$-$\overline{IV7}$ = open circuit. Taking one pin at a time, apply a protect programming pulse to each user-bus bit (UDO-UD7). Verify that the address circuits for each bit is isolated by applying V_{CCP}, in turn, to each user-bus pin (UDO-UD7) and measuring less than 200 microamperes of input current. (Note. Setup conditions are the same as those in step a.).

TABLE III. Electrical performance characteristics.

Test	Symbol	Limits		Unit
		Min	Max	
Programming supply voltage Address Protect	V_{CCP}	8.75	9.25 0	V
Maximum time V_{CCP} > 5.25 V			1.0	s
Programming voltage Address Protect		8.75 8.75	9.25 9.25	V
Programming current Address Protect			5 50	mA
Programming pulse rise time Address Protect	t_r	10 10	100 100	µs
Programming pulse width	t_w	0.5	1.0	ms

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8685101XX	18324	8X376/BXX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834