REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Editorial changes throughout. Table I changes include: V_{IH} change, regrouped devices to different limits. Table II, subgroups changed. Figures have been combined, some deleted. Quality Assurance and Quality conformance inspection paragraphs changed. Vendor CAGE number 34335 removed as a source of supply. The 01XX, 02XX, and the 05XX devices are inactive for new design.	1989 JAN 10	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A										
SHEET	22	23	24	25	26	27	28	29	30	31	32	33	34	35										

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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APPROVED BY: M.A. Frye

DRAWING APPROVAL DATE: 30 APRIL 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, NMOS 8K x 8 EEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-86830
A	14933	

SHEET 1 OF 35

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E882

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86830	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Acess time	Write speed	Write mode	End of Write Indicator	Endurance
01			250 ns	10 ms	byte	Rdy/$\overline{\text{Busy}}$	10,000 cycles
02			350 ns	10 ms	byte	Rdy/$\overline{\text{Busy}}$	10,000 cycles
03			300 ns	10 ms	byte	Rdy/$\overline{\text{Busy}}$	10,000 cycles
04			250 ns	1 ms	byte		10,000 cycles
05	(see 6.4)	(8K X 8 EEPROM)	250 ns	2 ms	byte	Rdy/$\overline{\text{Busy}}$	10,000 cycles
06			250 ns	10 ms	byte/page	$\overline{\text{DATA}}$ Polling	10,000 cycles
07			350 ns	10 ms	byte/page	$\overline{\text{DATA}}$ Polling	10,000 cycles
08			250 ns	10 ms	byte/page	$\overline{\text{DATA}}$ Polling	10,000 cycles
09			300 ns	10 ms	byte/page	$\overline{\text{DATA}}$ Polling	10,000 cycles
10			350 ns	12 ms	byte/page	$\overline{\text{DATA}}$ Polling	10,000 cycles

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier
Z	F-12 (28-lead, .740" x .420" x .130"), flat package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300° C
Junction temperature (T_J) 2/	+175° C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Input voltage range	-0.3 V dc to +6.25 V dc 3/
Data retention	10 years (minimum)
Endurance	10,000 cycles/byte (minimum) all devices

1/ All voltages are referenced to V_{SS} (ground).
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
3/ Does not apply to V_H.

1.4 Recommended operating conditions. 4/

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage, low (V_{IL})	-0.1 V dc to +0.8 V dc
Input voltage, high (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Block diagrams. The block diagrams shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

4/ All voltages are referenced to V_{SS} (ground).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $V_{CC} = +5.0$ V dc ±10% unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Supply current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = open, other inputs = V_{CC}	All	1, 2, 3		140	mA
Supply current (standby)	I_{SB}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = open, other inputs = V_{CC}	All	1, 2, 3		70	mA
Input leakage current	I_{IL}	$V_{IN} = 0.1$ to 5.5 V	All	1, 2, 3		10	µA
Output leakage current	I_{OZ} 1/	$V_{OUT} = 0.1$ to 5.5 V $\overline{CE} = \overline{OE} = V_{IH}$	All	1, 2, 3		10	µA
Low level input voltage	V_{IL}		All	1, 2, 3	-0.1	0.8	V
High level input voltage	V_{IH}		All	1, 2, 3	2.0	V_{CC} +0.5	V
Low level output voltage	V_{OL}	$I_{OL} = 2.1$ mA; $V_{CC} = 4.5$ V	All	1, 2, 3		0.45	V
High level output voltage	V_{OH}	$I_{OH} = -400$ µA; $V_{CC} = 4.5$ V	All	1, 2, 3	2.4		V
Input capacitance	C_I 2/	$V_{IN} = 0$ V, $V_{CC} = 5$ V f = 1.0 MHz $T_A = +25°C$	All	4		10	pF
Output capacitance	C_O 2/	$V_{OUT} = 0$ V, $V_{CC} = 5$ V f = 1.0 MHz $T_A = +25°C$	All	4		12	pF
Read cycle time	t_{AVAV}	See figure 4, as applicable 3/	03,09	9,10,11	300		ns
			01,04,05,06,08		250		
			02,07,10		350		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V dc, $V_{CC} = +5.0$ V dc ±10% unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Address access time	t_{AVQV}	$\overline{CE} = \overline{OE} = V_{IL}$ See figure 4, as applicable	03,09	9,10,11		300	ns
			01,04, 05,06, 08			250	
			02,07, 10			350	
Output enable access time	t_{OLQV}	$\overline{CE} = V_{IL}$ See figure 4, as applicable	01,04, 05,08	9,10,11		100	ns
			03,09			110	
			02,10			120	
			06,07			150	
Chip enable access time	t_{ELQV}	$\overline{OE} = V_{IL}$ See figure 4, as applicable	03,09	9,10,11		300	ns
			01,04, 05,06, 08			250	
			02, 07,10			350	
Chip disable to output in high Z	t_{EHQZ} 2/	See figure 4, as applicable	01,02, 03,04, 05,08, 09,10	9,10,11	0	100	ns
			06		10	60	
			07		10	80	
Output enable to output in low Z	t_{OLQV} 2/		04,05, 01,02, 06,07	9,10,11	10		ns
Output disable to output in high Z	t_{OHQZ} 2/		01,02, 03,04, 05,08, 09,10	9,10,11	0	100	ns
			06		10	60	
			07		10	80	
Output hold from address change	t_{AXQX}	$\overline{CE} = \overline{OE} = V_{IL}$ See figure 4, as applicable	All	9,10,11	0		ns
Write cycle time	t_{WC}	See figure 4, as applicable	01, 02,03, 06,07, 08,09	9,10,11	10		ms
			10		12		
			04		1		
			05		2		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V dc, $V_{CC} = +5.0$ V dc ±10% unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Address set-up time	t_{AVWL}	$\overline{CE} = \overline{OE} = V_{IL}$ See figure 4, as applicable	03,04, 08,09,	9,10,11	50		ns
			10		60		
			01,02, 05,06, 07		10		
Address hold time	t_{WLAX}	See figure 4, as applicable	04,05	9,10,11	50		ns
			02,10		100		
			01,03, 08		80		
			06,07, 09		200		
Write set-up time	t_{ELWL}		01-03, 05-10	9,10,11	0		ns
			04		50		
Write hold time	t_{WHEH}		01-04, 05-10	9,10,11	0		ns
Output enable set-up time	t_{OHWL}		01,02, 03,04, 05,08, 09,10	9,10,11	50		ns
			06,07		10		
Output enable hold time	t_{WHOL}		03,08, 09,10	9,10,11	0		ns
			01,02, 05, 06,07		50		
					10		
Chip enable hold time	t_{WLEL}		04	9,10,11	50		ns
Output enable hold time	t_{WLOH}		04	9,10,11	50		ns
Page write window	t_{WW} 4/		03,08	9,10,11	100		µs
			06,07, 09,10		20		
Time to device busy	t_{DB}		01,02	9,10,11		200	ns
			03			100	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $V_{CC} = +5.0$ V dc ±10% unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Write pulse width	t_{WLWH}	See figure 4, as applicable	01,02, 03,05, 06,07, 09	9,10,11	150		ns
			10		300		
			08		100		
			04		1		ms
Data set-up time	t_{DVWH}		04,05, 08		50		ns
			01,03, 06,09,		100		
			10		70		
			02,07		120		
Data hold time	t_{WHDX}		01,02 03,07, 08,10	9,10,11	30		ns
			05,06, 09		20		
	t_{WLDX}		04		50		
Byte load cycle	t_{BLC}		06,07, 09	9,10,11	3	20	µs
Write pulse width high	t_{WPH}		03, 06,09	9,10,11	50		ns
			07		100		
			08		250		
			10		300		
Data valid time	t_{WLDV}		06,07	9,10,11		300	ns
Write recovery 2/	t_{WR}		04	9,10,11		10	µs
Write recovery time from R/$\overline{B}$	t_{RE}		01,02, 05	5/	0	10	µs
			03		0		ns
Write enable pulse width	t_{CWLWH}		04	9,10,11	10		ms
CC set-up time	t_{CCLWL}		04	9,10,11	50		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $V_{CC} = +5.0$ V dc ±10% unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
CC hold time	t_{WLCCL}	See figure 4, as applicable	04	9,10,11	50		ns
Write set-up time	t_{ELWH}		01,02,05	9,10,11	1		µs
Output set-up time	t_{OHWH}		01,02,05	9,10,11	1		µs
Output enable hold time	t_{WLOL}		01,02,05	9,10,11	1		µs
Erase recovery time	t_{OLEX}		01,02,05	9,10,11	10		µs
Write enable pulse width	t_{WHWL}		01,02,05	9,10,11	10		ms

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{LO} with the output under test connected to V_{OUT}.
2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ Tested by application of specified signals and conditions:
$\overline{WE} = V_{IH}$
Output load: 1 TTL gate and C_L = 100 pF (minimum).
Input rise and fall times: ≤ 20 ns.
Input pulse levels: Device types 01-10: 0.4 V to 2.4 V
Timing measurement reference level:
Device types 01-10:
Inputs: 0.8 V and 2 V
Outputs: 0.8 V and 2 V
4/ A timer of t_{WW} duration starts at every low to high transition of $\overline{WE}$. If it is allowed to time out, a page load will start. A transition of $\overline{WE}$ from high to low will stop the timer.
5/ This parameter for information only.

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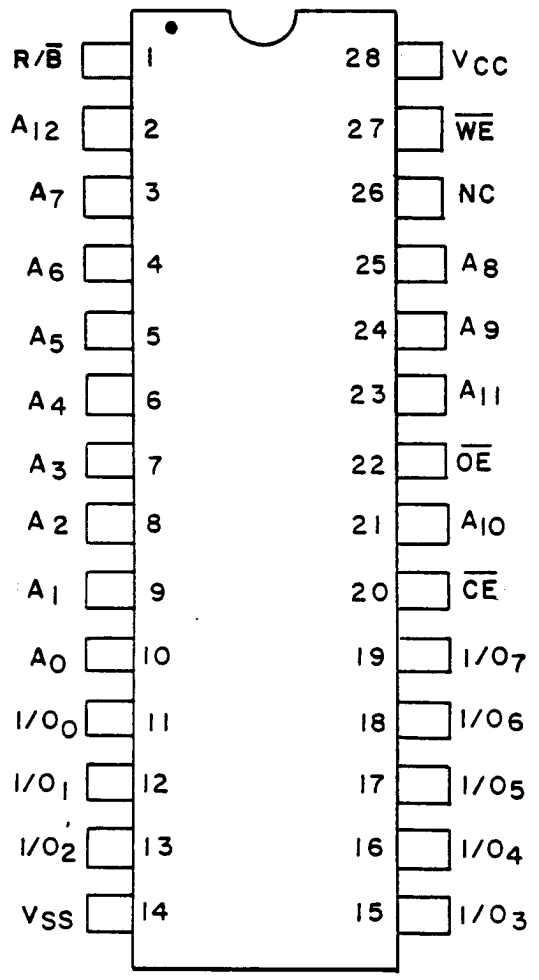
Device types 01 through 10

Cases X and Z

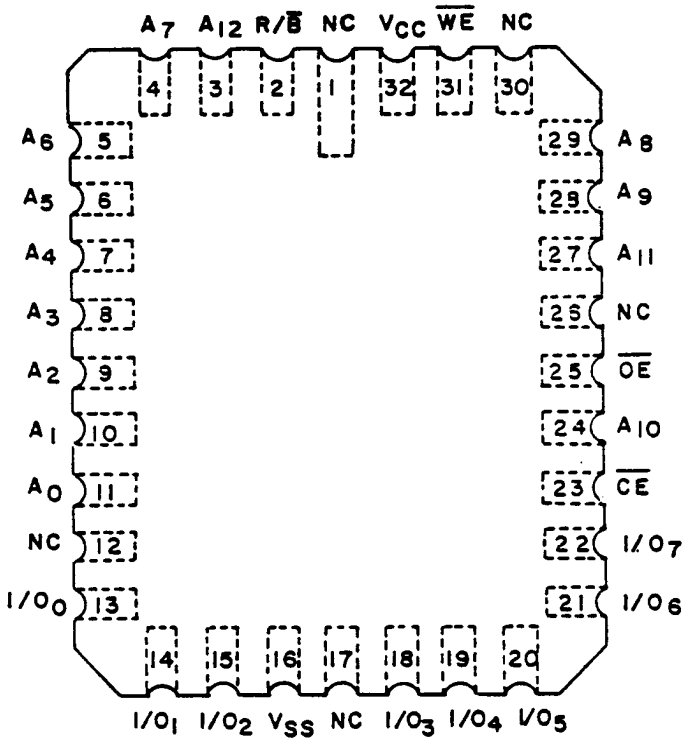


NOTES: Device type 04 has $\overline{CC}$ at pin 1.
Device types 06, 07, 08, 09, and 10 have NC at pin 1.

FIGURE 1. Terminal connections.

Device types 01 through 10

Case Y



NOTES: Device type 04 has $\overline{CC}$ at pin 1.
Device types 06, 07, 08, 09, and 10 have NC at pin 1.

FIGURE 1. Terminal connections - Continued.

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Device types 06 and 07

Programming procedure D

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and write inhibit	Hi Z	Standby
X	L	X	Write inhibit	-	-
X	X	H	Write inhibit	-	-
L	V_{OE}	L	Chip erase	D_{IN} = H	Active

FIGURE 2. Truth table.

Device types 01. 02, and 03

Programming procedure A

Mode select table

Inputs			Outputs			
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	R/$\overline{B}$	I/O	A_g	Mode
L	L	H	Hi Z	Data out	X	Read
L	H	⌐⌐	⌐⌐	Data in	X	Write
H	X	X	Hi Z	Hi Z	X	Standby
L	H	H	Hi Z	Hi Z	X	Read inhibit
X	L	L	---	---	X	Write inhibit
L	L	H	Hi Z	Code	V_H	Auto select
L	L	H	L	$\overline{D_{IN}}$	X	Data polling

V_H = 12.0 V ±.5 V
H = High
L = Low
X = Don't care
⌐⌐= Pulse

Device types 08. 09, and 010

Mode select table

Inputs			Outputs		
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	A_g	Mode
L	L	H	Data out	X	Read
L	H	⌐⌐	Data in	X	Write
H	X	X	Hi Z	X	Standby
L	H	H	Hi Z	X	Read inhibit
X	L	X	---	X	Write inhibit
L	L	H	Code	V_H	Auto select
L	L	H	$\overline{D_{IN}}$	X	Data polling

V_H = 12.0 V ±.5 V
H = High
L = Low
X = Don't care
⌐⌐= Pulse

FIGURE 2. Truth table - Continued

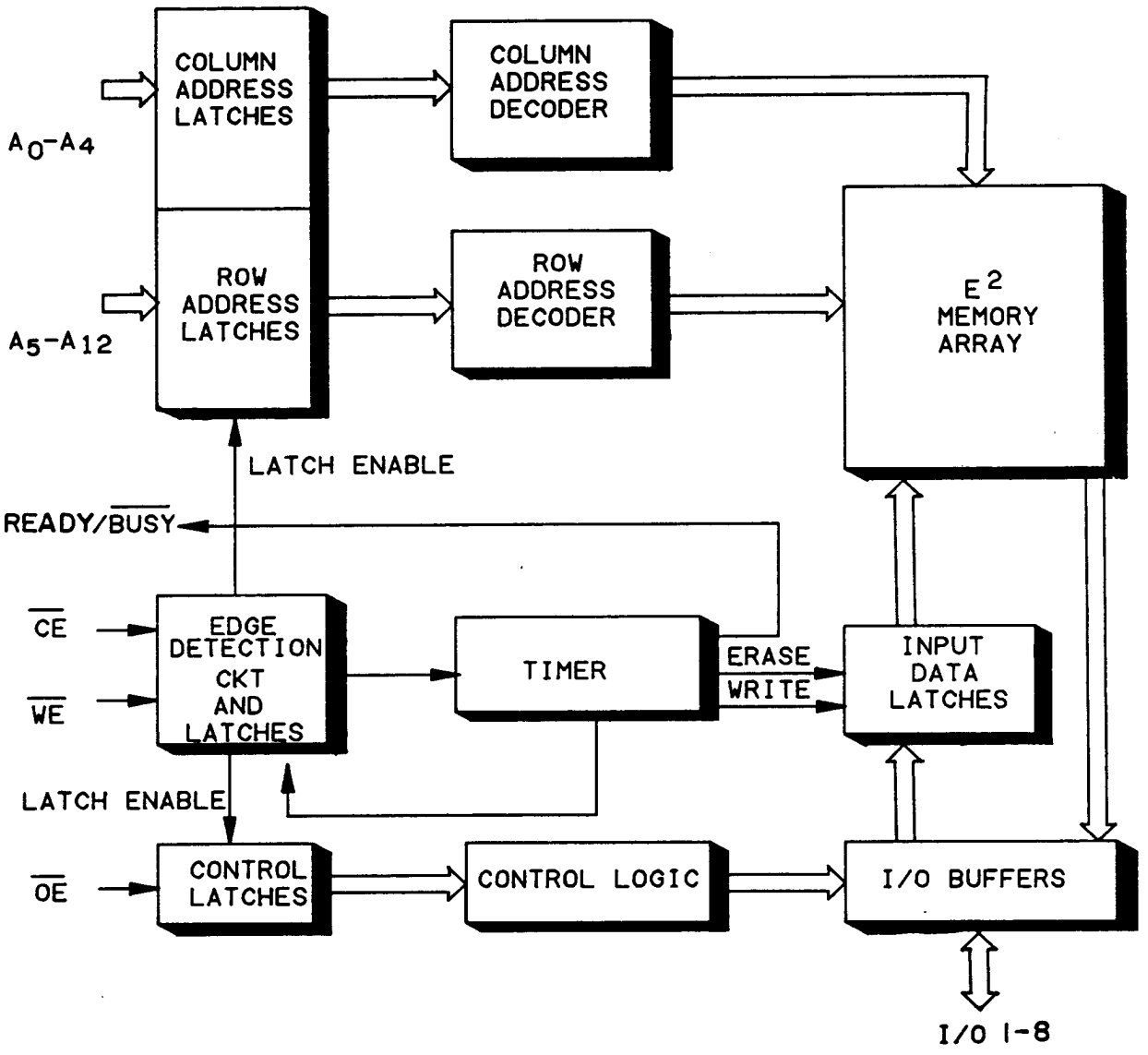
Device types 01, 02, 04, and 05

Programming procedure C (see note 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Pin 1 (see notes 2 and 3)	Device types
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	N/A V_{IH}	01, 02, and 05 04
Standby	V_{IH}	X	X	Hi Z	X	01, 02, 04 and 05
Chip clear	V_{IL} V_{IL}	V_H V_{IH}	V_H V_{IL}	D_{IN} = FF D_{IN} = FF	N/A V_{IL}	01, 02, and 05 04
Byte write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	X V_{IH}	01, 02, and 05 04
Write or read inhibit	V_{IL}	V_{IH}	V_{IH}	Hi Z	X	01, 02, 04 and 05

NOTES:
1. Table definitions:
   - V_{IH} = High logic level
   - V_{IL} = Low logic level
   - V_H = Chip clear high voltage (15 V)
   - X = Don't care
   - H Z = High impedance state
   - D_{IN} = Data input
   - D_{OUT} = Data output
2. Applied to device types 01, 02, and 05 with the Ready/$\overline{Busy}$ function. Pin 1 has an open drain output and requires an external 3 kilohms resistor to V_{CC}. This resistor value is dependent on the number of or-tied Ready/$\overline{Busy}$ pins.
3. Applies to device type 04 with the TTL chip clear function.

FIGURE 2. Truth table - Continued.

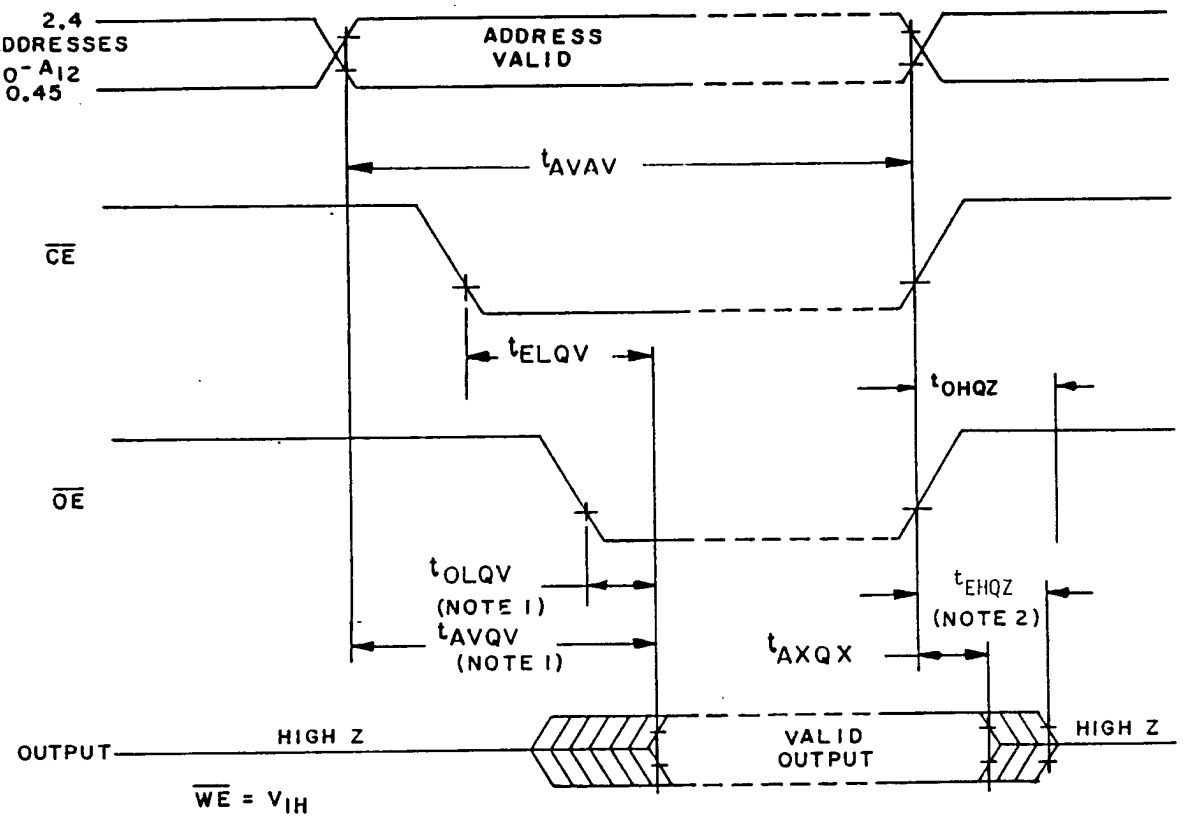


NOTE: Ready/Busy is only connected on devices 01, 02, 03, and 05.

FIGURE 3. Block diagram.

Device types 01 through 10

Read cycle timing



NOTES:

1. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} = t_{EHQZ} or t_{OHQZ}.
3. V_{CC} shall be applied simultaneously or after $\overline{WE}$ and removed simultaneously or before $\overline{WE}$.
4. Output load is TTL gate and 100 pF including jig or probe capacitance.
5. Input rise and fall time $\leq$ 20 ns.
6. Input pulse levels of 0.4 and 2.4 Volts.
7. Timing measurement reference levels:
   Inputs 0.8 and 2.0 volts.
   Outputs 0.8 and 2.0 volts.

FIGURE 4. Switching waveforms.

Device types 01, 02, 03, 05, 08, 09, and 10

Write cycle timing

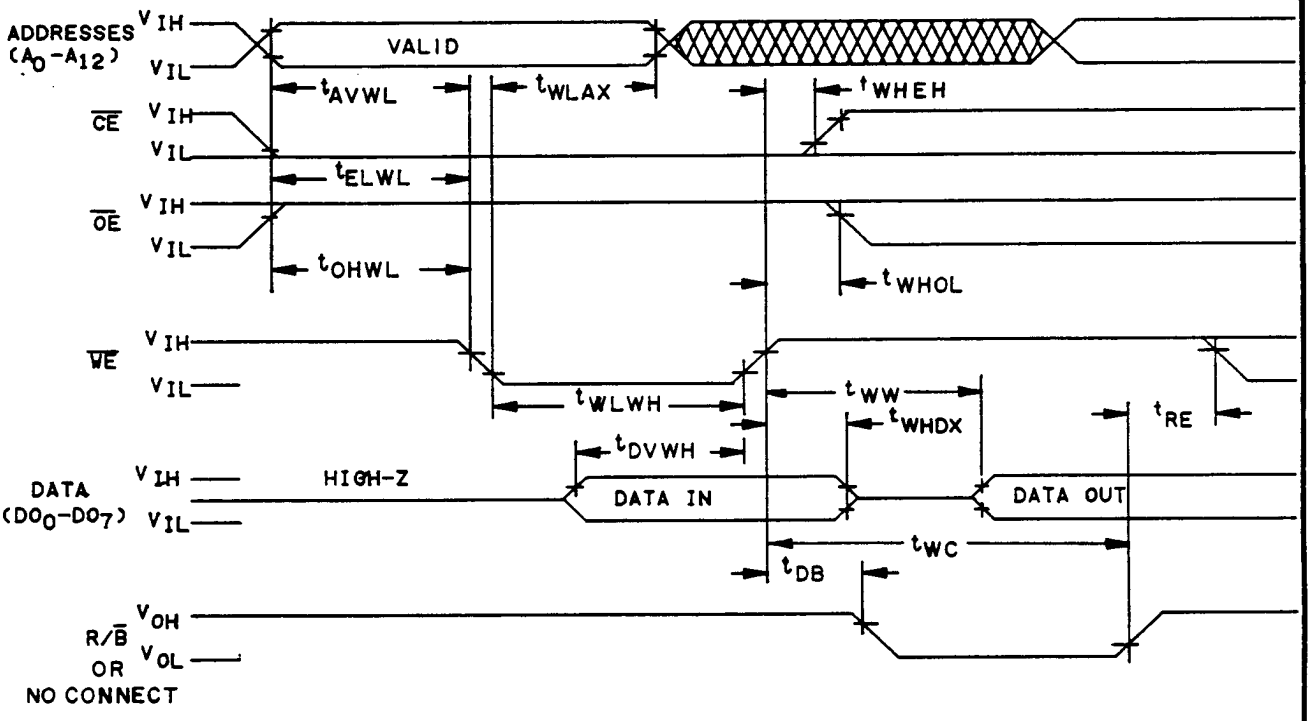


FIGURE 4. Switching waveforms - Continued.

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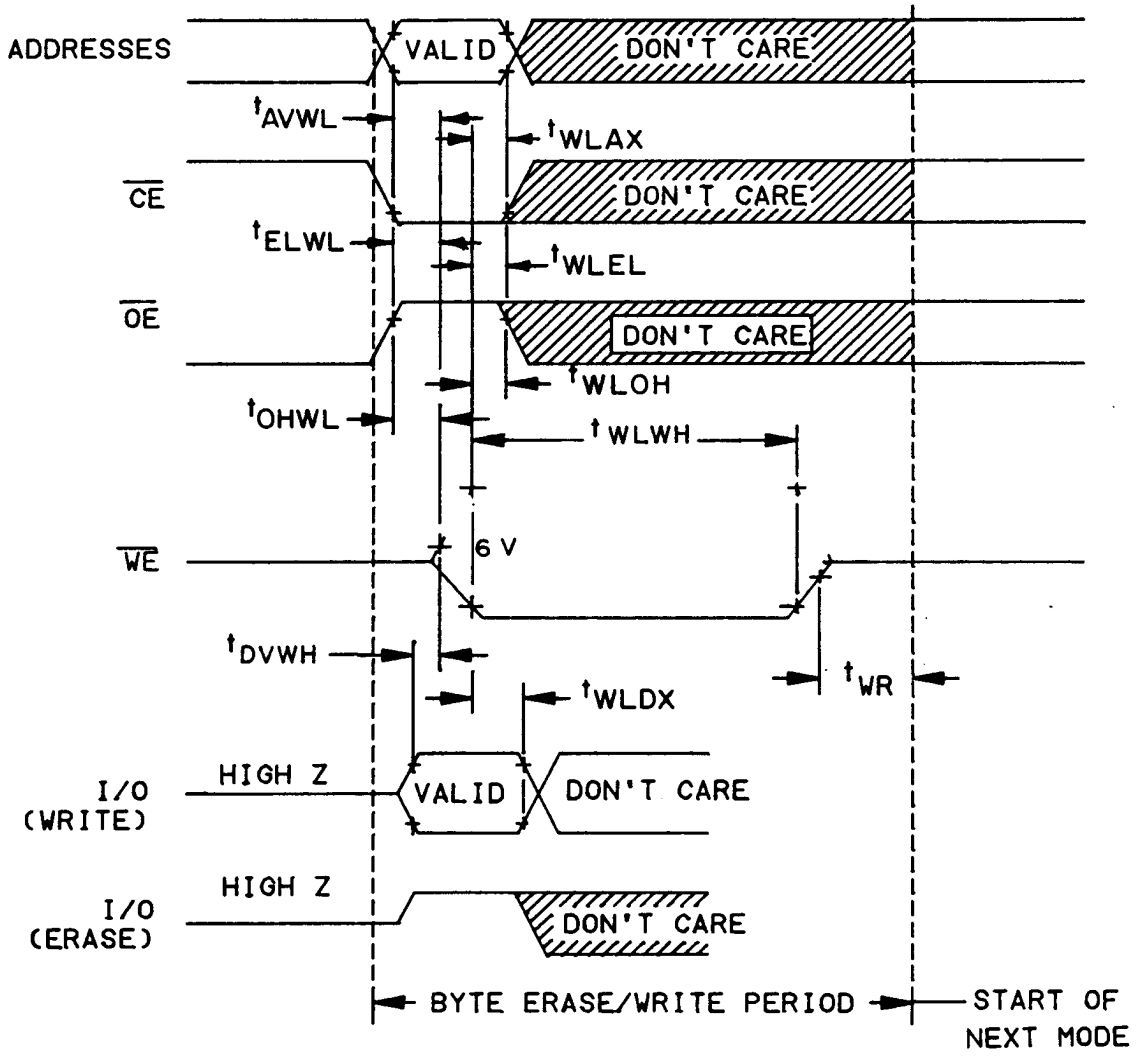
Device type 04

Write cycle timing



NOTES:
1. Input timing reference levels are 1.0 and 2.0 volts.
2. output timing reference levels are 0.8 and 2.0 volts.
3. Input pulse rise and fall times (10% and 90%) $\leq$ 20 ns.
4. Input pulse levels are 0.4 and 2.4 volts.
5. Program verify equivalent to the reade mode.

FIGURE 4. Switching waveforms - Continued.

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Device types 06 and 07

Write cycle timing

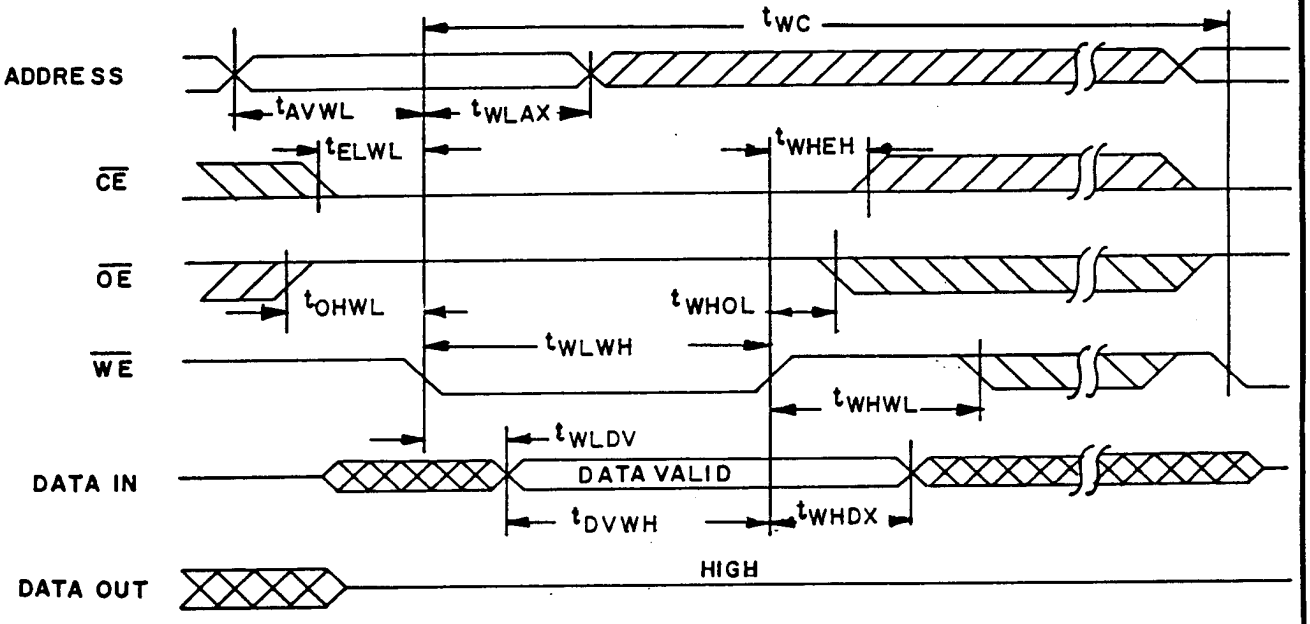

FIGURE 4. Switching waveforms - Continued.

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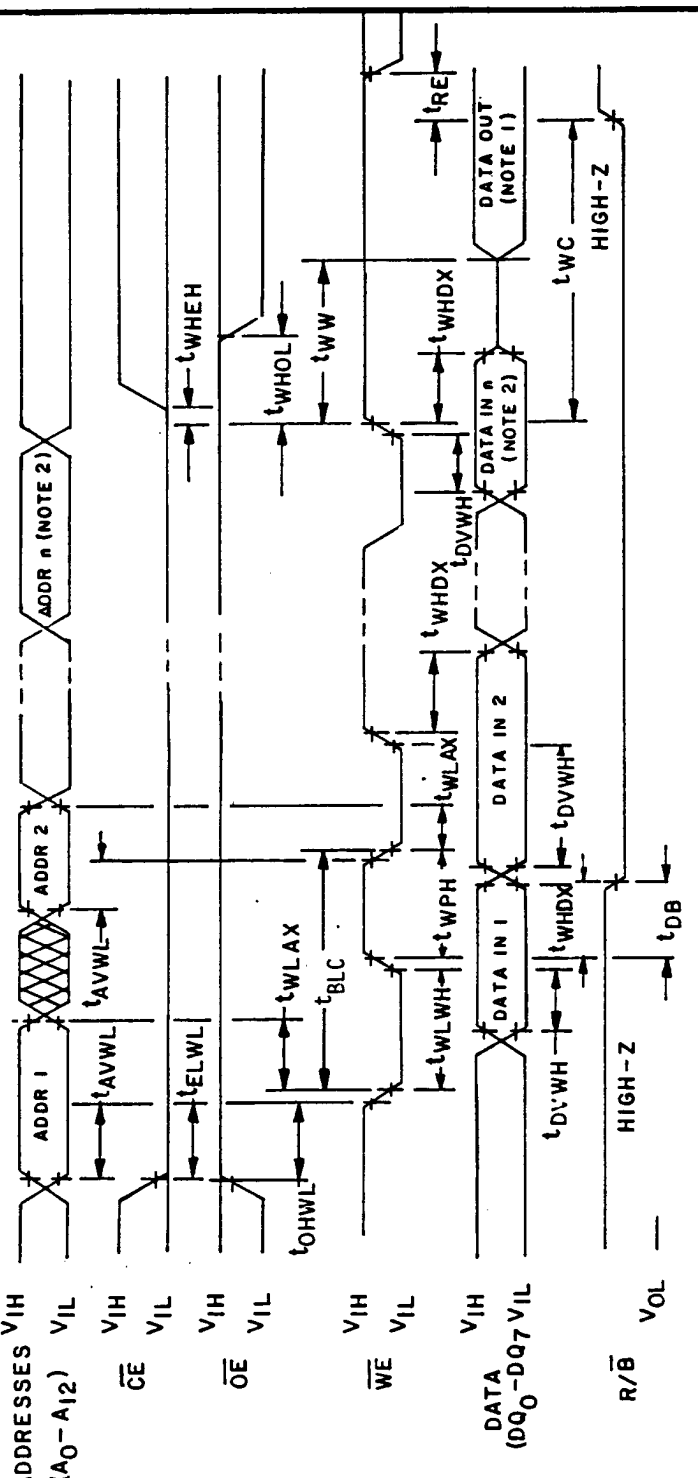
Device types 01, 02, 03, 08, 09, and 10

Programming procedures A1 and A2

Page write cycle timing



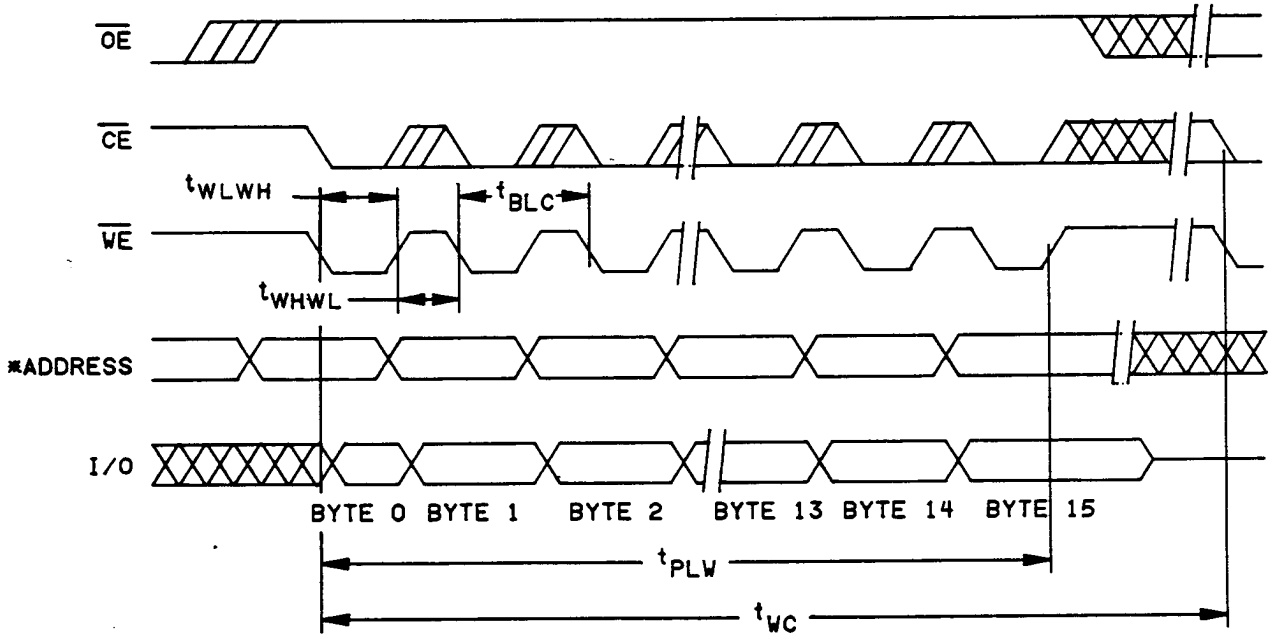
NOTES:
1. This is where Data polling is available. See Data polling timing for setups.
2. $n \leq 32$

FIGURE 4. Switching waveforms - Continued.

Device types 06 and 07

Programming procedure D

Page write cycle timing



NOTE: The page address, addresses A_4 - A_{12} must remain the same throughout the write cycle (t_{PLW}). If a page violation occurs, writes to an unknown address could occur.

FIGURE 4. Switching waveforms - Continued.

Device types 01 through 03 and 06, and 08-10

Chip clear waveform

Programming procedure A1 and A2

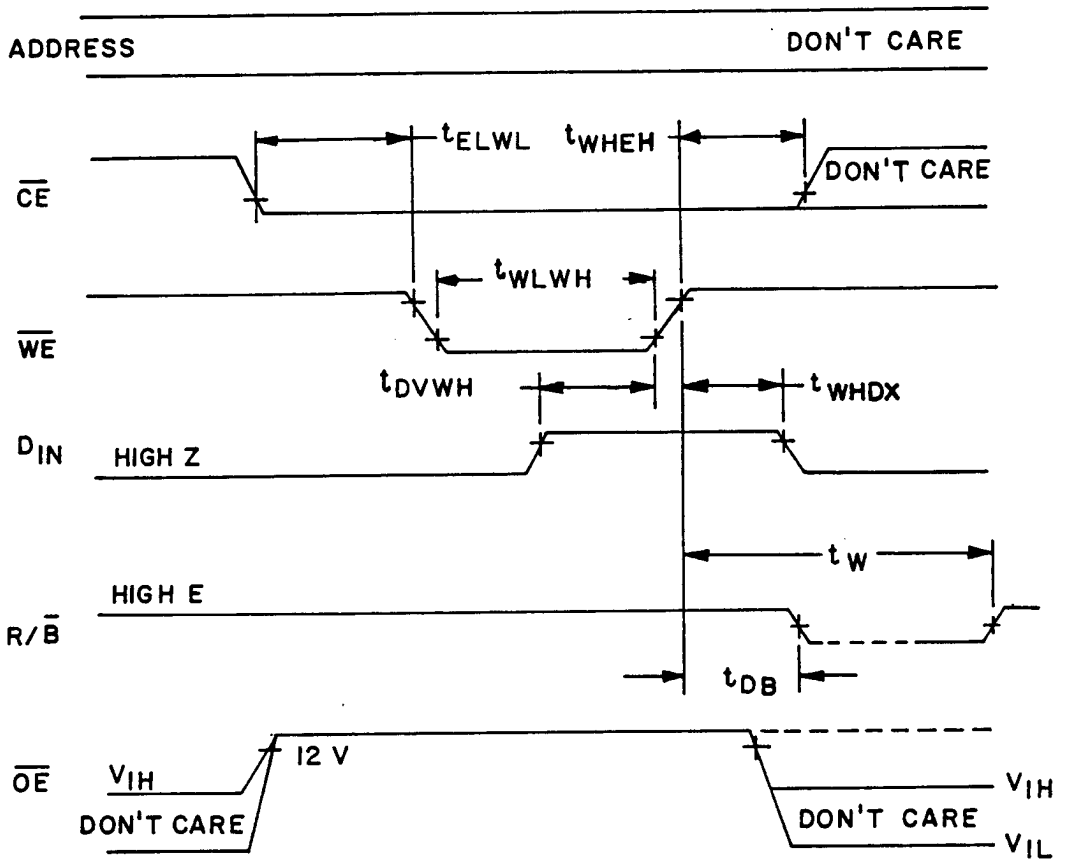


FIGURE 4. Switching waveforms - Continued.

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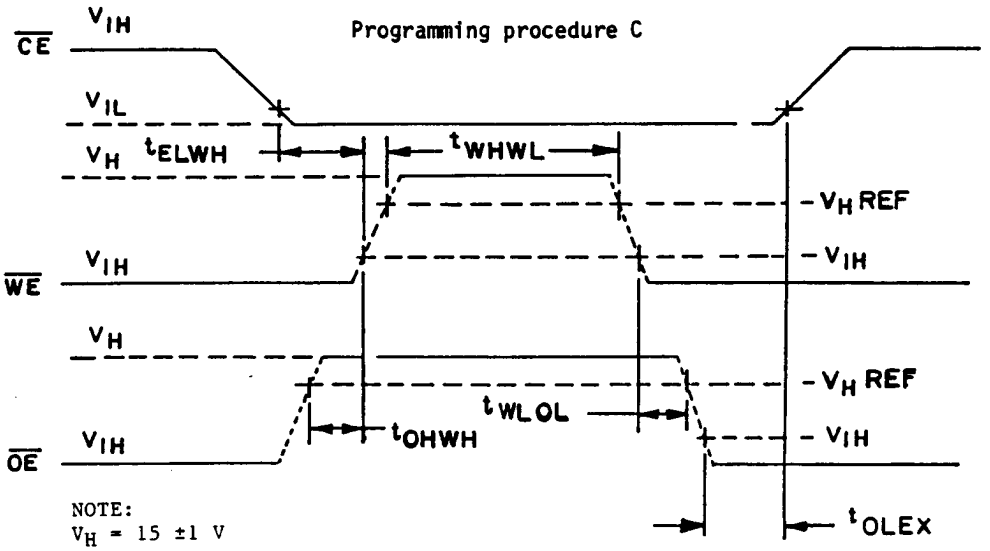
Device types 01, 02 and 05

Chip clear waveform

Programming procedure C



NOTE:
V_H = 15 ±1 V
V_H Ref = 13.5

Device types 06 and 07

Chip clear waveform

Programming procedure D

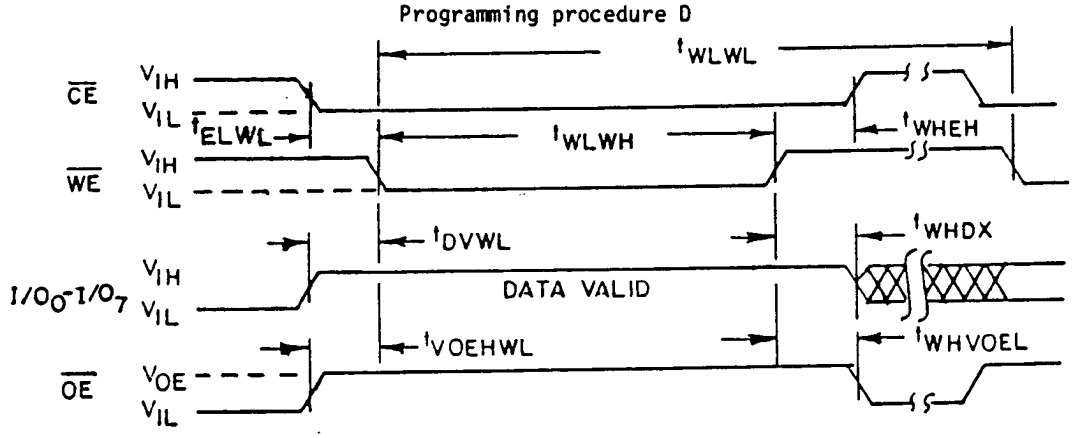
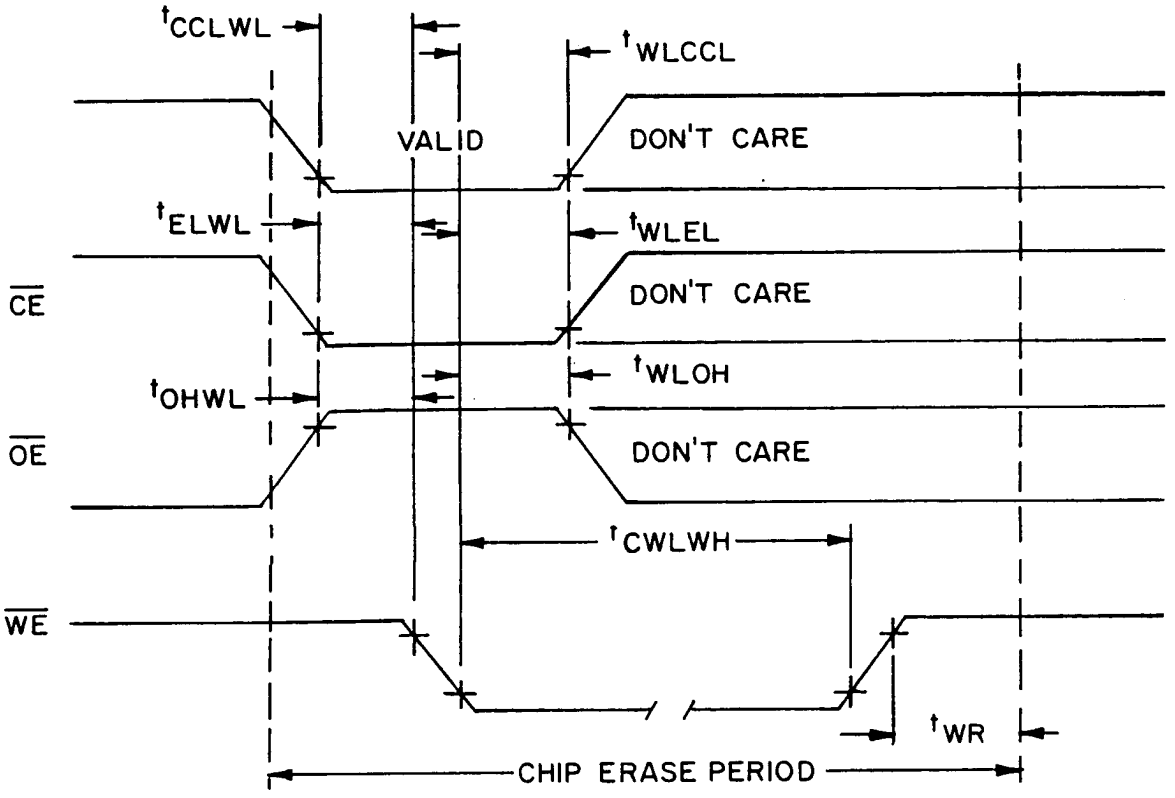


FIGURE 4. Switching waveforms - Continued.

Device type 04

Chip clear waveform



NOTE: Address and Data are don't care during chip earse.

FIGURE 4. Switching waveforms - Continued.

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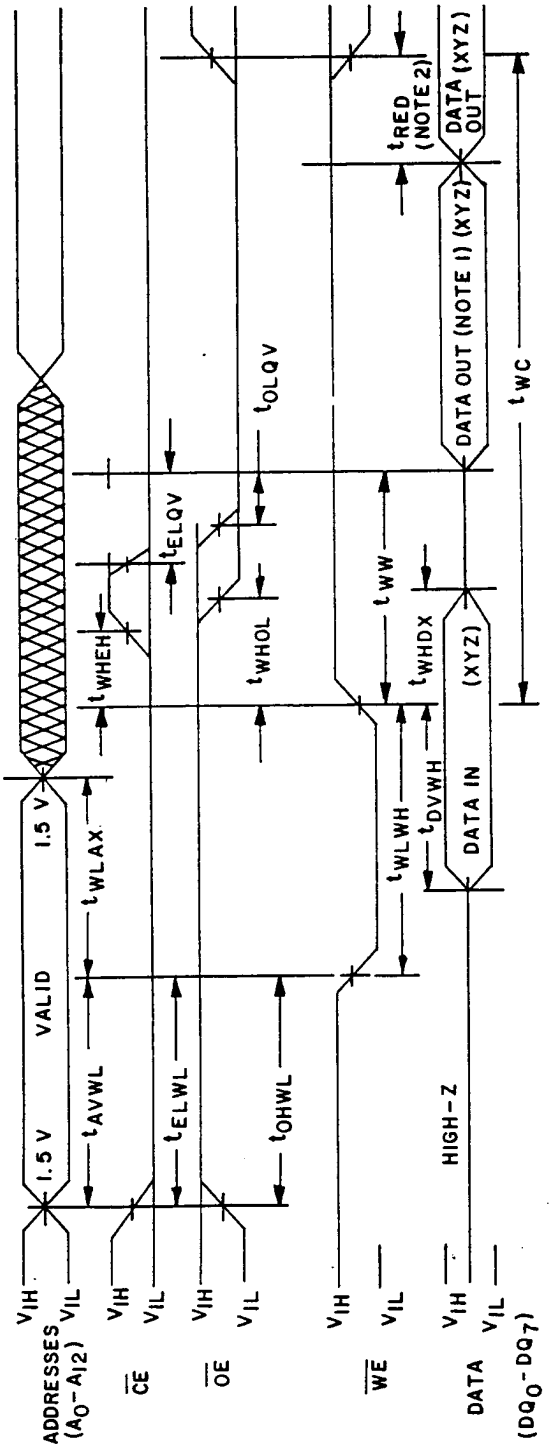
Device types 03, 08, 09, and 10

Data bar polling

Programming procedure C

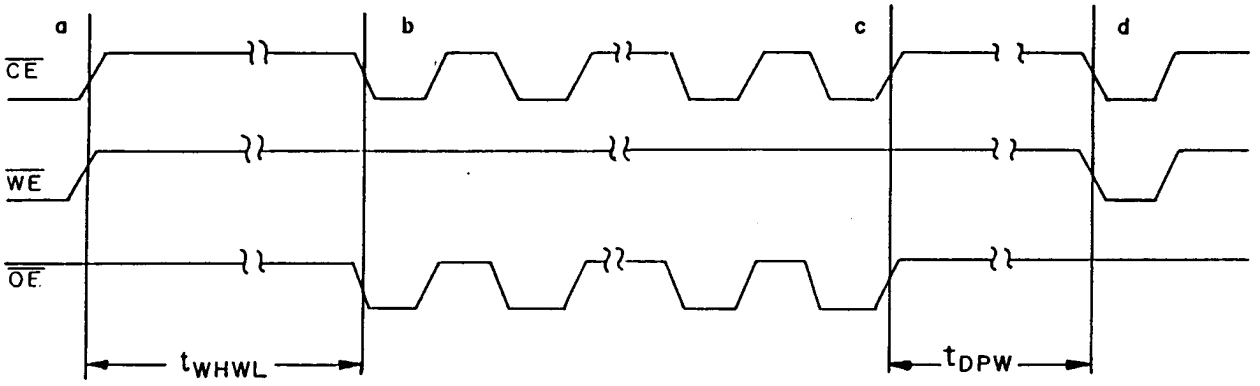


NOTES:
1. This is where Data polling is available (if a read operation is performed).
2. After the write cycle is completed (Data Out True). The user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

FIGURE 4. Switching waveforms - Continued.

Device types 06 and 07

$\overline{\text{Data}}$ polling



a. Last write (byte or page mode) before polling.
b. First attempt to poll.
c. First true data response.
d. Initiate new write operation.

Symbol	Parameter	Min	Max
t_{WPH}	Delay from $\overline{WE}$ $\overline{CE}$ to $\overline{OE}$ $\overline{CE}$	50 ns	
t_{DPW}	Delay from polling true to $\overline{WE}$ $\overline{CE}$	500 µs	

$\overline{\text{Data}}$ polling:
The 2864 features $\overline{\text{Data}}$ polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{\text{Data}}$ polling allows a simple bit test operation to determine the status of the 2864, eliminating additional interrupt inputs or external hardware. during the internal programming cycle, any complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

FIGURE 4. Switching waveforms - Continued.

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Column address (see notes)

		0	1	2	3	4	5	6 . . .	25	26	27	28	29	30	31
	0	AA	AA	AA	AA	AA	AA	AA . . .	AA	AA	AA	AA	AA	AA	AA
	1	55	55	55	55	55	55	55 . . .	55	55	55	55	55	55	55
	2	AA	AA	AA	AA	AA	AA	AA . . .	AA	AA	AA	AA	AA	AA	AA
	3	55	55	55	55	55	55	55 . . .	55	55	55	55	55	55	55
R	.							. . .							
O	.							. . .							
W	.							. . .							
	124	AA	AA	AA	AA	AA	AA	AA . . .	AA	AA	AA	AA	AA	AA	AA
A	125	55	55	55	55	55	55	55 . . .	55	55	55	55	55	55	55
D	126	AA	AA	AA	AA	AA	AA	AA . . .	AA	AA	AA	AA	AA	AA	AA
D	127	55	55	55	55	55	55	55 . . .	55	55	55	55	55	55	55
R	.							. . .							
E	.							. . .							
S	.							. . .							
S	252	AA	AA	AA	AA	AA	AA	AA . . .	AA	AA	AA	AA	AA	AA	AA
	253	55	55	55	55	55	55	55 . . .	55	55	55	55	55	55	55
See note 1	254	AA	AA	AA	AA	AA	AA	AA . . .	AA	AA	AA	AA	AA	AA	AA
See note 2	255	55	55	55	55	55	55	55 . . .	55	55	55	55	55	55	55

NOTES:
1. All address numbers shown in decimal.
2. Each column/row address location corresponds to 1 byte.
3. Manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern.
4. All data numbers shown in hexadecimal.
   A = 10101010 55 = 01010101

FIGURE 5. Array data pattern.

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3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.9.1 Erasure of EEPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in section 6 as applicable. Devices shall be shipped in the erased (logic "1's") and verified state unless otherwise specified.

3.9.2 Programmability of EEPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 6.3, 6.4, 6.5, and 6.6 as applicable.

3.9.3 Verification of erasure or programmability of EEPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of reading the device per the procedures and characteristics specified in 6.3 through 6.6 as applicable. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or F using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a checkerboard pattern or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/data retention test prior to burn-in, in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be block, byte, or page at equipment room ambient temperature and shall cycle all bytes for a minimum of 10,000 cycles for all device types.

(2) After cycling, perform a high temperature unbiased bake for 2.5 hours at 250°C minimum (unassembled devices only), or 24 hours at 170°C minimum, or 72 hours at 150°C minimum. All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g. worst case pattern).

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (minimum, e.g. high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices, all input and output terminals tested, and no failures.

4.3.2 Groups C inspections. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring endpoint electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or F using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. An endurance test, per method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady state life test (see 4.3.3c) and extended data retention (see 4.3.3e). Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially, two groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:

(1) Cell 1 shall be cycled at -55° C and cell 2 shall be cycled at +125° C for a minimum of 10,000 cycles for all devices.

(2) Perform group A subgroups 1, 7, and 9 after cycling. Form two new cells (cell 3 and 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of 1/2 of the devices from cell 1 and 1/2 of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and 2.

(3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C1, as specified in method 5005 of MIL-STD-883.

e. Extended data retention shall consist of:

(1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g. worst case pattern, see 4.2c 2).

(2) Unbiased bake for 1000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship.

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e. t_1 + 273 = °K).
t_1 = time (hrs) at temperature T_1.
t_2 = time (hrs) at temperature T_2.
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 V.
The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.

(3) Read the pattern after bake and perform endpoint electrical tests for table II herein for group C.

4.3.3 Groups D inspections. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring endpoint electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

4.4 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables of method 5005 of MIL-STD-883 and as follows:

4.4.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11

1/ (*) Indicates PDA applies to subgroups 1 and 7
2/ Any or all subgroups may be combined when using multifunction testers.
3/ Subgroup 7 and 8 shall consist of writing and reading the data pattern specified in accordance with the limits of table I, subgroups 9, 10, and 11.
4/ For all electrical tests, the device shall be programmed to the data pattern specified.
5/ (**) Indicates that subgroup 4 will only be performed during initial qualification and after design or process changes (see 4.3.1c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/228XXBXX.

6.3 Programming procedures for method A1.

6.3.1 Byte write programming procedure. The programming characteristics in table I and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms on figure 4 and programming characteristics of table I shall apply.

b. As delivered, all bits are in the high "H" state. Information is introduced by selectively programming "L" or "H" into the desired bit locations. A programmed "L" can be changed to an "H" or vice versa.

c. The word address is selected in the same manner as in the read mode. Data to be programmed, 8-bits in parallel, are presented to the data lines (DQ_0-DQ_7). Logic levels for address and data lines, and the supply voltages are the same as for the read mode. The write cycle is completely self timed, and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. $\overline{WE}$ must be held high for at least t_{WW} maximum in order to remain in the byte write mode. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating the EEPROM is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high the EEPROM has completed writing, and is ready to accept another cycle. The Ready/$\overline{Busy}$ pin is an open-drain output which allows two or more Ready/$\overline{Busy}$ pins to be OR-tied together. A pullup resistor can be attached to the Ready/$\overline{Busy}$ pin. The value of this resistor shall be calculated as follows.

$$R_{PU} = \frac{4.6 \text{ volts}}{2.1 \text{ mA} - I_{IL}}$$

Where I_{IL} = total V_{IL} input current of all devices connected to Ready/$\overline{Busy}$.

d. The $\overline{WE}$ can be toggled during the time period after t_{WW} until t_{WW} +4.0 ms. $\overline{WE}$ has to be held high during the balance of write cycle. Applies to device types 08 and 10 only.

6.3.2 Page write programming procedure.

a. Connect the device in the electrical configuration for programming the waveforms on figure 4 and programming characteristics of table I shall apply.

b. As delivered, all bits are in the high "H" state. Information is introduced by selectively programming "L" or "H" into the desired bit locations. A programmed "L" can be changed to an "H" or vice versa.

c. The page write mode allows 1 to 32 bytes of data to be written in a single cycle. The page write mode consists of a load sequence followed by an automatic write sequence. The word address is selected in the same manner as in the read mode. Data to be programmed, 32 bytes in parallel (256 bits) is presented to the data lines (D_0-D_7), with the logic levels and supply voltages set to the same values as in read mode. Addresses are latched on each falling edge of $\overline{WE}$, while data is latched on each rising edge of $\overline{WE}$. The page address is latched on the falling edge of the last $\overline{WE}$.

The automatic write sequence is initiated when $\overline{WE}$ goes from low to high and stays high for t_{WW} maximum. It consists of an erase cycle, which erases any data that existed in each addressed cell and a write cycle, which puts data back into erased cells.

The Ready/$\overline{Busy}$ pin ($R/\overline{B}$) goes to a logic low level indicating a write mode which signals a microprocessor host that the system bus is free for other activity.

6.3.3 Erasing procedure. Chip erase is performed in accordance with the waveforms and timing relationships shown on figure 4 (per appropriate device type) and the manufacturers applicable data.

6.3.4 $\overline{\text{DATA}}$ polling procedure.

a. Use the $\overline{\text{DATA}}$ polling timing set-up as shown on figure 4, and the characteristics shown in table I.

b. $\overline{\text{DATA}}$ polling requires a simple software routine that performs a read operation when the chip is in automatic write mode. The data that becomes valid during this $\overline{\text{DATA}}$ polling read is the inverse of all 8 bits last written to the outputs. This inverse data can be read after $\overline{\text{WE}}$ has been high for t_{WW} maximum. The true data (DQ_0-DQ_7) will become valid when the automatic write has been completed.

6.4 Programming procedures for method A2.

6.4.1 Byte write programming procedure. The programming characteristics in table I and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms on figure 4 and programming characteristics of table I shall apply.

b. As delivered, all bits are in the high "H" state. Information is introduced by selectively programming "L" or "H" into the desired bit locations. A programmed "L" can be changed to an "H" or vice versa.

c. The word address is selected in the same manner as in the read mode. Data to be programmed, 8-bits in parallel, are presented to the data lines (DQ_0-DQ_7). Logic levels for address and data lines, and the supply voltages are the same as for the read mode. The write cycle is completely self timed, and initiated by a low going pulse on the $\overline{\text{WE}}$ pin. On the falling edge of $\overline{\text{WE}}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{\text{CE}}$ and $\overline{\text{OE}}$) are latched. $\overline{\text{WE}}$ must be held high for at least t_{WW} maximum in order to remain in the byte write mode.

d. The $\overline{\text{WE}}$ can be toggled during the time period after t_{WW} until t_{WW} +4.0 ms. $\overline{\text{WE}}$ has to be held high during the balance of write cycle. Applies to devices 08 and 10 only.

6.4.2 Page write programming procedure.

a. Connect the device in the electrical configuration for programming the waveforms on figure 4 and programming characteristics of table I shall apply.

b. As delivered, all bits are in the high "H" state. Information is introduced by selectively programming "L" or "H" into the desired bit locations. A programmed "L" can be changed to an "H" or vice versa.

c. The page write mode allows 1 to 32 bytes of data to be written in a single cycle. The page write mode consists of a load sequence followed by an automatic write sequence. The word address is selected in the same manner as in the read mode. Data to be programmed, 32 bytes in parallel (256 bits) is presented to the data lines (D_0-D_7), with the logic levels and supply voltages set to the same values as in read mode. Addresses are latched on each falling edge of $\overline{\text{WE}}$, while data is latched on each rising edge of $\overline{\text{WE}}$. The page address is latched on the falling edge of the last $\overline{\text{WE}}$.

The automatic write sequence is initiated when $\overline{\text{WE}}$ goes from low to high and stays high for t_{WW} maximum. It consists of an erase cycle, which erases any data that existed in each addressed cell and a write cycle, which puts data back into erased cells.

6.4.3 Erasing procedure. Chip erase is performed in accordance with the waveforms and timing relationships shown on figure 4 (per appropriate device type) and the conditions specified in table I.

6.4.4 $\overline{\text{DATA}}$ polling procedure.

a. Use the $\overline{\text{DATA}}$ polling timing set-up as shown on figure 4, and the characteristics shown in table I.

b. $\overline{\text{DATA}}$ polling requires a simple software routine that performs a read operation when the chip is in automatic write mode. The data that becomes valid during this $\overline{\text{DATA}}$ polling read is the inverse of all 8 bits last written to the outputs. This inverse data can be read after $\overline{\text{WE}}$ has been high for t_{WW} maximum. The true data (DQ_0-DQ_7) will become valid when the automatic write has been completed.

6.5 Programming procedures for method C.

6.5.1 Programming procedure. The following procedure shall be followed when programming (write) is performed. The waveforms and timing relationship shown on figure 4 (per appropriate device type) and the conditions specified: Table I shall be adhered to. Information is introduced by selectively programming a TTL low or TTL high on each I/O of the address desired. For device type 04, each byte must be erased (TTL high) prior to programming. Functionality shall be verified at all temperatures (group A, subgroups 7 and 8) by programming all bytes of each device and verifying the pattern used.

6.5.2 Erasing procedure. There are two forms of erasure, chip and byte, whereby all bits or the address selected will be erased to a TTL high.

a. Chip erase is performed per the waveforms and timing relationships shown on figure 4 (per appropriate device type) and the conditions specified in table I.

b. Byte erase is performed per the waveforms and timing relationships shown on figure 4 (per appropriate device type) and the conditions specified in table I.

6.5.3 Read mode operation. The waveforms and timing relationships shown on figure 4 and the conditions specified in table I shall be applied when reading the device. Pattern verification utilizes the read mode.

6.6 Programming procedures for method D.

6.6.1 Programming procedure. The following procedure shall be followed when programming (write) is performed. The waveforms and timing relationships shown on figure 4 and the conditions specified in table I shall be adhered to, initially, and after each chip erasure (see 4.8.2), all bits are in the "H" state (output high). Information is introduced by selectively programming "L" and "H" into the desired bit locations. A programmed "L" can be changed to an "H" by programming an "H". No erasure is necessary (see 4.8.2).

6.6.2 Erasing procedure.

a. Chip erase. The device is erased by setting the output enable ($\overline{\text{OE}}$) pin to 18-22 volts, while all inputs are set in the normal byte program mode. After the chip erasure, all bits are in the "H" state. The test conditions and limits specified in table IV shall be applied. To assure erasure of all bits in the array, the chip erase cycle must have been performed three times.

b. Byte erase. The byte is erased by simultaneously programming an "H" state into each bit at the selected address.

6.6.3 Read mode operation. The device is in the read mode whenever the CE and OE pins are at a logic "L" (low level), and the WE pin is at V_{IH}. The waveforms and timing relationships shown on figure 4 and the test conditions and limits specified in table I shall be applied.

6.7 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.8 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part 1/ number	Replacement military specification part number	Programming procedure method
5962-8683001XX	2/	AM2864BE-250/BXA	M38510/22808BXX	A1
		DM2864-250/B		C
5962-8683001YX	3/	AM2864BE-250/BUA	M38510/228	A1
	61394	LM2864-250/B	M38510/228	C
5962-8683001ZX	3/	AM2864BE-250/BYC		A1
	61394	FM2864-250/B		C
5962-8683002XX	2/	AM2864BE-350/BXA	M38510/22807BXX	A1
		DM2864-350/B		C
5962-8683002YX	3/	AM2864BE-350/BUA	M38510/228	A1
	61394	LM2864-350/B	M38510/228	C
5962-8683002ZX	3/	AM2864BB-350/BYC		A1
	61394	FM2864-350/B		C
5962-8683003XX	3/	AM2864BE-300/BXA		A1
5962-8683003YX	3/	AM2864BE-300/BUA		A1
5962-8683003ZX	3/	AM2864BE-300/BYC		A1
5962-8683004XX	61394	DM52B33H-250/B		C
5962-8683004YX	61394	LM52B33H-250/B		C
5962-8683004ZX	61394	FM52B33H-250/B		C
5962-8683005XX	2/	DM2864H-250/B	M38510/22809XX	C
5962-8683005YX	61394	LM2864H-250/B	M38510/228	C
5962-8683005ZX	61394	FM2864H-250/B	M38510/228	C

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number	Programming procedure method
5962-8683006XX	60395	X2864ADMB-25	M38510/228	D
5962-8683006YX	60395	X2864AEMB-25	M38510/228	D
5962-8683006ZX	60395	X2864AFMB-25	M38510/228	D
5962-8683007XX	60395	X2864ADMB-35	M38510/228	D
5962-8683007YX	60395	X2864AEMB-35	M38510/228	D
5962-8683007ZX	60395	X2864AFMB-35	M38510/228	D
5962-8683008XX	3/	AM2864A-25/BXA	M38510/228	A2
5962-8683008YX	3/	AM2864A-25/BUA	M38510/228	A2
5962-8683008ZX	3/	AM2864A-25/BYC	M38510/228	A2
5962-8683009XX	3/	AM2864AE-300/BXA	M38510/228	A2
5962-8683009YX	3/	AM2864AE-300/BUA	M38510/228	A2
5962-8683009ZX	3/	AM2864AE-300/BYC	M38510/228	A2
5962-8683010XX	3/			A2
5962-8683010YX	3/			A2
5962-8683010ZY	3/			A2

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Inactive for new design, use M38510/228XXBXX.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address	Programming procedure
61394	SEEQ Technology, Incorporated 1849 Fortune Drive San Jose, CA 95131	C
60395	XICOR, Incorporated 851 Buckeye Court Milpitas, CA 95035	D

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