



Triple 4-3-3 Input Bus Driver

**ELECTRICALLY TESTED PER:
MPG 10523**

The 10523 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} = -2.1$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the 10523 are "turned-off". This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the 10523, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 2.

- 435 mW Max/Pkg (No Load)
- $t_{pd} = 3.0$ ns typ (1.5 Vdc in to 50% out)
- $t_r, t_f = 2.5$ ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	5	2	GND
BOUT	2	6	3	51 Ω to V_{TT}
AOUT	3	7	4	50 Ω to V_{TT}
A1N	4	8	5	OPEN
A1N	5	9	7	OPEN
A1N	6	10	8	OPEN
A1N	7	11	9	OPEN
VEE	8	12	10	VEE
B1N	9	13	12	OPEN
B1N	10	14	13	OPEN
B1N	11	15	14	OPEN
C1N	12	16	15	OPEN
C1N	13	1	17	OPEN
C1N	14	2	18	OPEN
COUT	15	3	19	51 Ω to V_{TT}
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

$V_{TT} = -2.0$ V MAX/ -2.2 V MIN

$V_{EE} = -5.7$ V MAX/ -5.2 V MIN

Military 10523

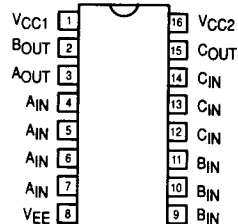


AVAILABLE AS

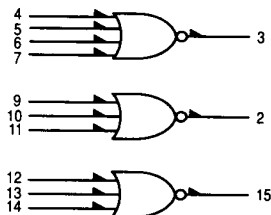
- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: 10523/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

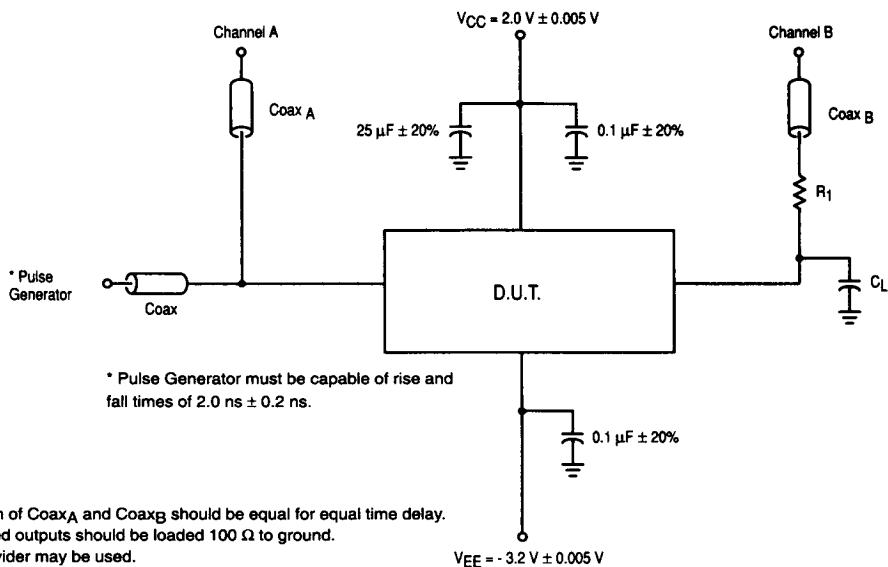
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Length of Coax_A and Coax_B should be equal for equal time delay.
2. Unused outputs should be loaded 100Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0 \text{ ns} \pm 0.2 \text{ ns}$ measured at (20% - 80%).
5. $P_W \geq 20 \text{ ns}$.
6. $PRF = 1.0 \text{ MHz}$.
7. $R_1 = 50 \Omega$ resistor in series with 50Ω coax constituting the 100Ω load.
8. C_L = Jig and stray capacitance $\leq 5.0 \text{ pF}$.

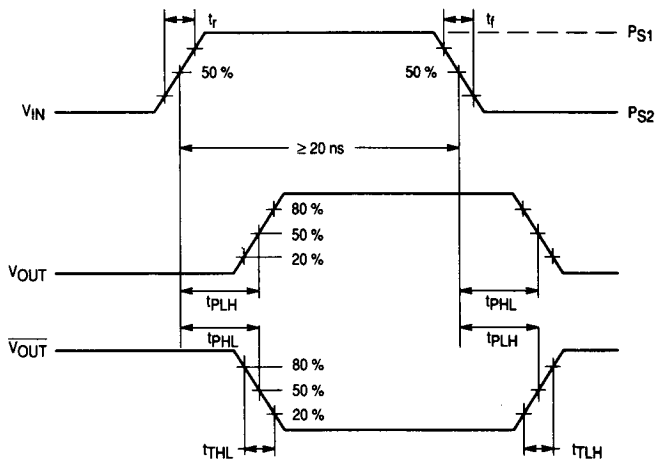


Figure 1. Switching Test Circuit and Waveforms

10523 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EE}	VEEL
T _A = 25 °C	-0.78	-1.85	-1.475	-1.105	+1.11	+0.31	-5.2	-3.2
T _A = 125 °C	-0.63	-1.82	-1.400	-1.000	+1.32	+0.445	-5.2	-3.2
T _A = -55 °C	-0.88	-1.89	-1.510	-1.255	+1.30	+0.385	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
Functional Parameters:		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max									
VOH	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V								
VOL	Low Output Voltage	-2.15	-2.03	-2.15	-2.03	-2.15	-2.03	V	4 - 7, 9 - 15							
VOH1	High Output Voltage	-0.95	-0.78	-0.845	-0.63	-1.10	-0.88	V				4 - 7, 9 - 15	8	1, 16	2, 3, 15	
VOL1	Low Output Voltage	-2.15	-1.60	-2.15	-1.525	-2.15	-1.635	V	4, 9, 12		4 - 7, 9 - 15		8	1, 16	2, 3, 15	
IEE	Power Supply Current	-75		-83		-83		mA	4 - 7, 9 - 15				8	1, 16	8	
IIH	Input Current High		220		373		373	µA	4 - 7, 9 - 15				8	1, 16	4 - 7, 9 - 15	
IIL	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 15			8	1, 16	4 - 7, 9 - 15	

10523 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EE}	V _{EEL}
T _A = 25 °C	- 0.78	- 1.85	- 1.475	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T _A = 125 °C	- 0.63	- 1.82	- 1.400	- 1.400	+ 1.32	+ 0.445	- 5.2	- 3.2
T _A = - 55 °C	- 0.88	- 1.89	- 1.255	- 1.510	+ 1.30	+ 0.385	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW			
Functional Parameters:		+ 25 °C		+ 125 °C				- 55 °C	Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = + 2.0 V, Output Load = 100 Ω to GND			
		Subgroup 9		Subgroup 10		Subgroup 11						
		Min	Max	Min	Max	Min	Max					
t _{TLH}	Rise Time	1.0	3.5	1.0	3.5	1.0	3.5	ns	V _{IN}	V _{OUT}	V _{EEL}	P. U. T.
t _{THL}	Fall Time	1.0	3.5	1.0	3.5	1.0	3.5	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15
t _{PHL}	Propagation Delay High to Low	1.2	4.4	1.2	6.0	1.2	4.4	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15
t _{PLH}	Propagation Delay Low to High	1.2	4.4	1.2	6.0	1.2	4.4	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15

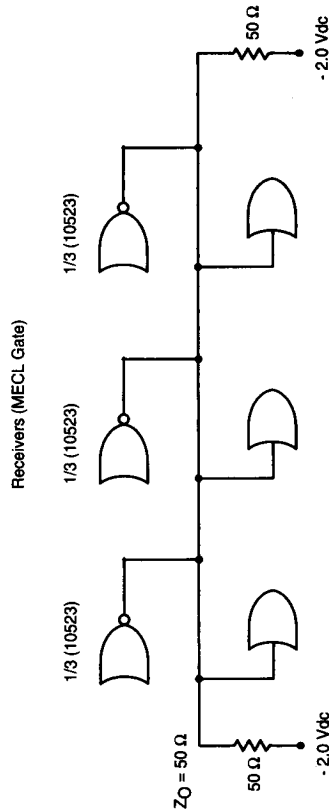


Figure 2. 50 Ohm Bus Driver