



128Kx32 3.3V SRAM MODULE ADVANCED*

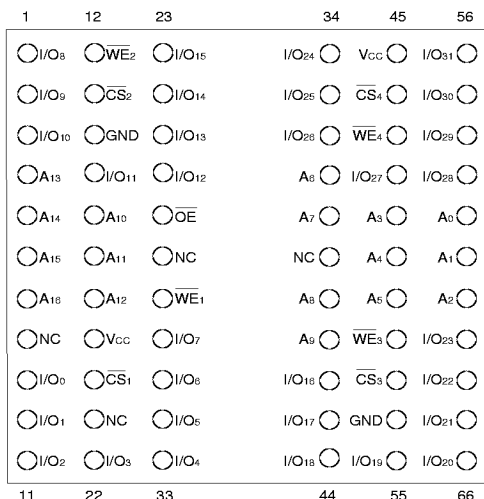
FEATURES

- Access Times of 20, 25, 35, 45, 55nS
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.185 inch square Hermetic Ceramic HIP (Package 401)
 - 68 lead, 40mm, Hermetic CQFP (Package 501)
 - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS128K32V-XG2X - 8 grams typical
 - WS128K32V-XHX - 13 grams typical
 - WS128K32V-XG4X - 20 grams typical

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION FOR WS128K32V-XHX

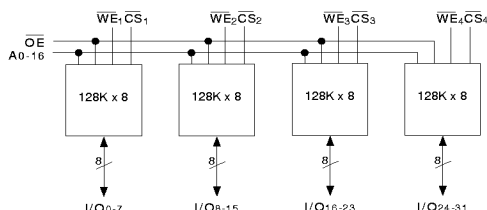
TOP VIEW

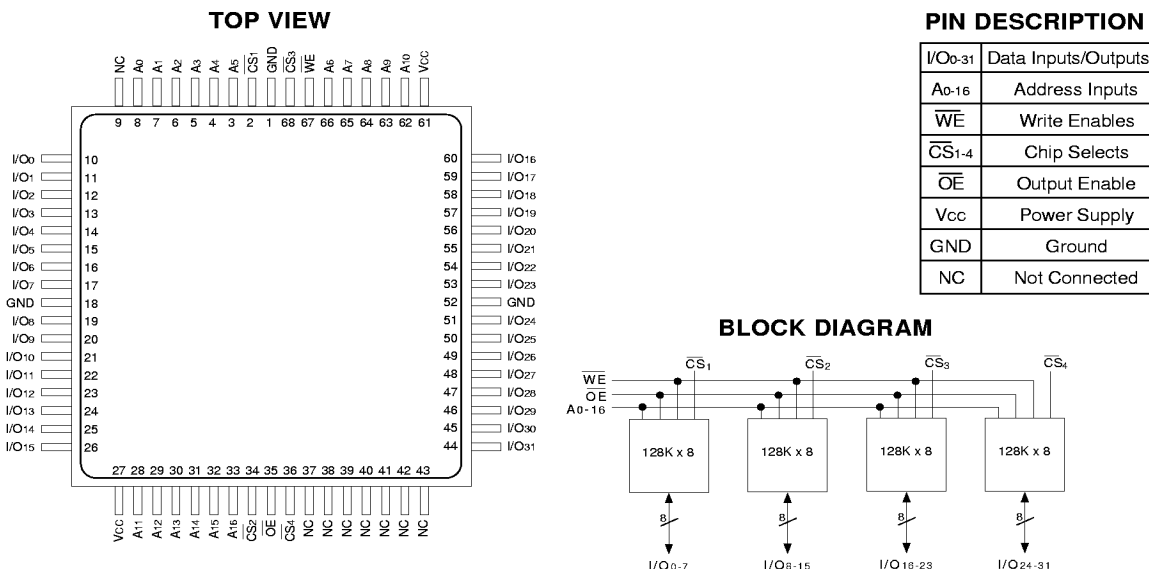
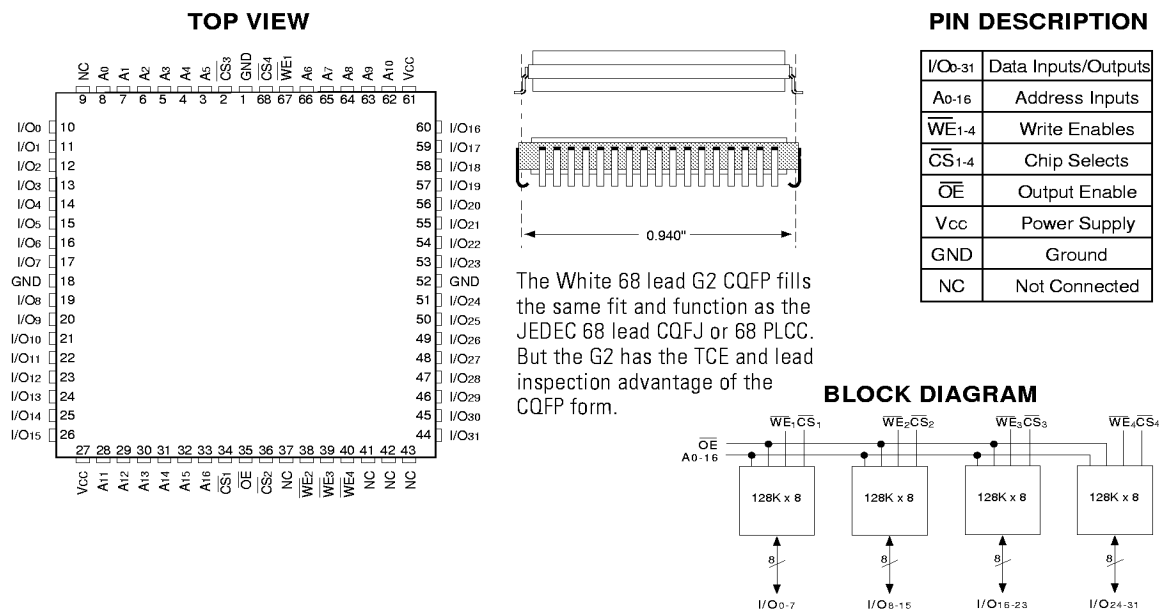


PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₆	Address Inputs
WE ₁₋₄	Write Enables
CS ₁₋₄	Chip Selects
OE	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



**FIG. 2 PIN CONFIGURATION FOR WS128K32V-XG4X****FIG. 3 PIN CONFIGURATION FOR WS128K32V-XG2X**

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4			50	
CQFP G2			20	
$\overline{CS}$ 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS(V_{CC} = 3.3V ±0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz		500	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz		60	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

**AC CHARACTERISTICS**
($V_{CC} = 3.3V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle												
Read Cycle Time	t_{RC}	20		25		35		45		55		nS
Address Access Time	t_{AA}		20		25		35		45		55	nS
Output Hold from Address Change	t_{OH}	3		3		3		3		3		nS
Chip Select Access Time	t_{ACS}		20		25		35		45		55	nS
Output Enable to Output Valid	t_{OE}		12		15		20		25		25	nS
Chip Select to Output in Low Z	t_{CLZ}^1	5		5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}^1	5		5		5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}^1		10		12		15		20		20	nS
Output Disable to Output in High Z	t_{OHZ}^1		10		12		15		20		20	nS

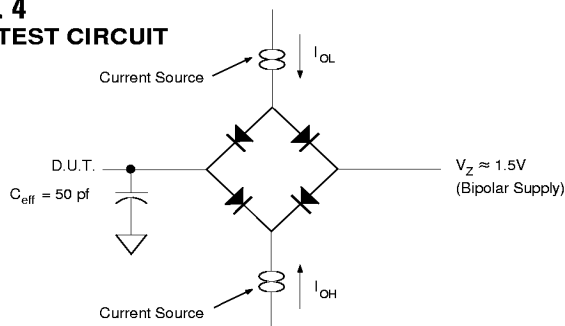
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
($V_{CC} = 3.3V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle												
Write Cycle Time	t_{WC}	20		25		35		45		55		nS
Chip Select to End of Write	t_{CW}	15		20		30		40		50		nS
Address Valid to End of Write	t_{AW}	15		20		30		40		50		nS
Data Valid to End of Write	t_{DW}	12		15		18		20		25		nS
Write Pulse Width	t_{WP}	15		20		30		40		50		nS
Address Setup Time	t_{AS}	0		0		0		0		0		nS
Address Hold Time	t_{AH}	0		0		0		0		0		nS
Output Active from End of Write	t_{OW}^1	5		5		5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}^1		10		10		15		15		15	nS
Data Hold Time	t_{DH}	0		0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT

**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG.5
TIMING WAVEFORM - READ CYCLE

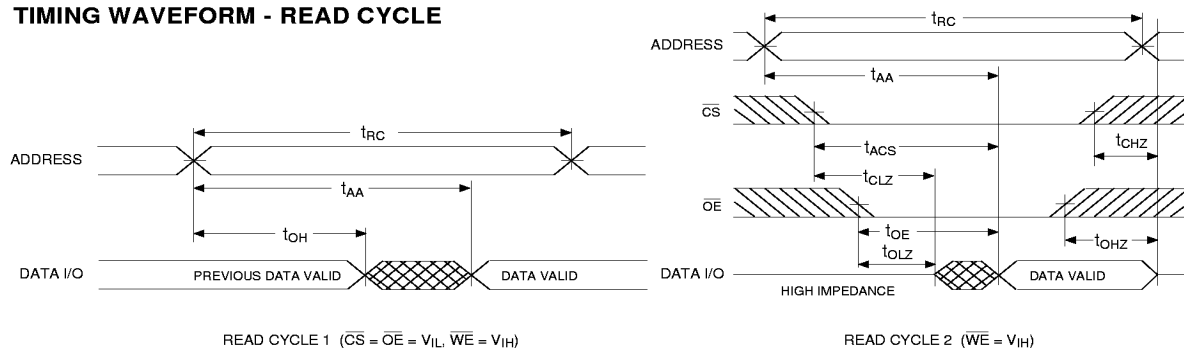


FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED

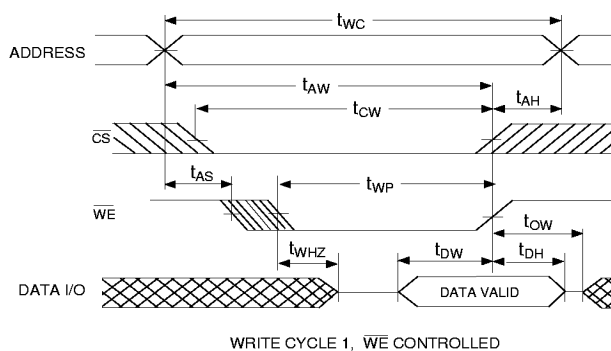
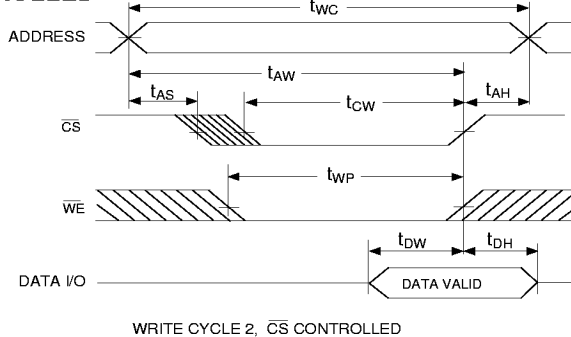
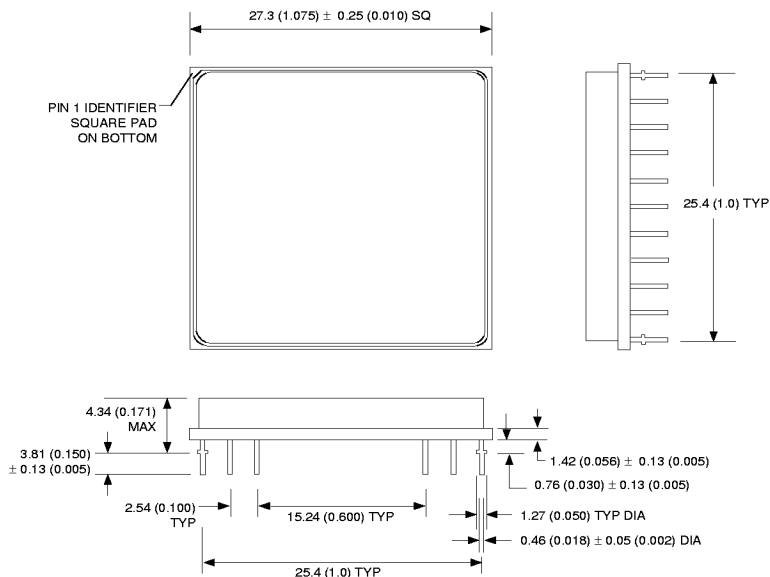
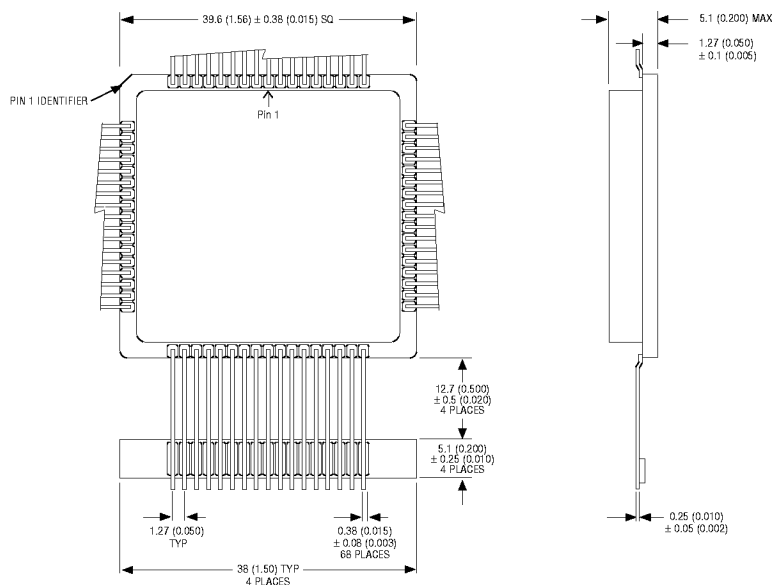


FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED

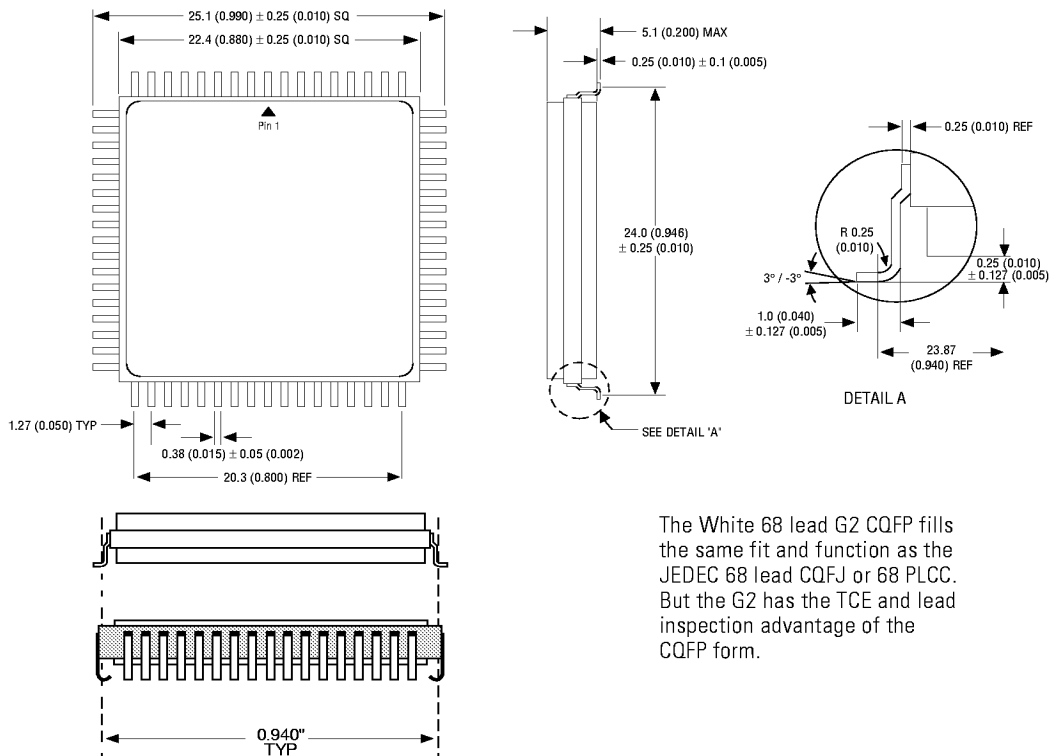


**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)**

The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION****W S 128K 32 V - XXX X X****DEVICE GRADE:**

S = SMD

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H = Ceramic Hex-In-line Package, HIP (Package 401)

G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)

G4 = 40 mm Ceramic Quad Flat Pack, CQFP (Package 501)

ACCESS TIME in nS**IMPROVEMENT MARK:**Low Voltage Supply 3.3V $\pm$ 10%**ORGANIZATION, 128Kx32**

User configurable as 256Kx16 or 512Kx8

SRAM**WHITE MICROELECTRONICS**