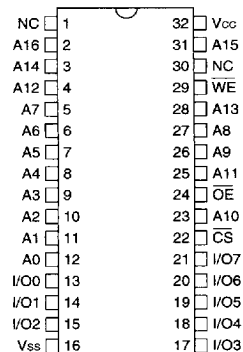




128Kx8 SRAM MODULE

FIG. 1

PIN CONFIGURATION
TOP VIEW

PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground

FEATURES

- Access Times 55 to 120nS
- Standard Microcircuit Drawing, 5962-93156
- MIL-STD-883 Compliant Devices Available
- JEDEC Standard 32 pin, Hermetic Ceramic DIP (Package 302)
- Military Temperature Range (-55°C to +125°C)
- Organized as 128K x 8
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	40	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	40	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

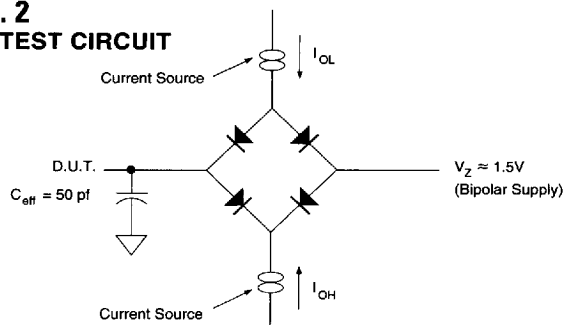
Parameter	Sym	Conditions	-55		-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10		10		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10		10		10		10		10	μA
Operating Supply Current	I _{CC}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		60		30		30		30		30	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz		15		1.0		1.0		1.0		1.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-55			-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		10	900		5	500		5	500		5	400		1	400	μA
	I _{CCDR2}	V _{CC} = 2V		8	500		5	300		5	300		5	300		1	300	μA

FIG. 2
AC TEST CIRCUIT

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V₂ is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V₂ is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

**AC CHARACTERISTICS**(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-55		-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	55		70		85		100		120		nS
Address Access Time	t _{AA}		55		70		85		100		120	nS
Output Hold from Address Change	t _{OH}	5		5		15		15		15		nS
Chip Select Access Time	t _{ACS}		55		70		85		100		120	nS
Output Enable to Output Valid	t _{OE}		40		50		55		60		60	nS
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		10		10		10		nS
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		5		5		nS
Chip Disable to Output in High Z	t _{CHZ} ¹		30		35		40		45		50	nS
Output Disable to Output in High Z	t _{OHZ} ¹		30		30		40		40		50	nS

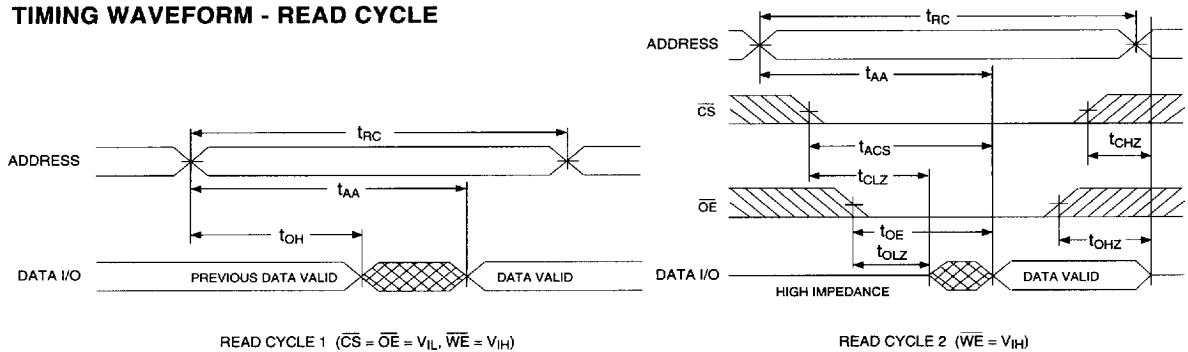
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-55		-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	55		70		85		100		120		nS
Chip Select to End of Write	t _{CW}	45		65		80		90		110		nS
Address Valid to End of Write	t _{AW}	50		50		75		75		85		nS
Data Valid to End of Write	t _{DW}	25		35		40		45		45		nS
Write Pulse Width	t _{WP}	40		40		65		70		80		nS
Address Setup Time	t _{AS}	0		0		0		0		0		nS
Address Hold Time	t _{AH}	0		0		0		0		0		nS
Output Active from End of Write	t _{OW} ¹	5		10		10		10		10		nS
Write Enable to Output in High Z	t _{WHZ} ¹	0	30	0	30	0	35	0	40	0	40	nS
Data Hold Time	t _{DH}	0		0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 3
TIMING WAVEFORM - READ CYCLE



4

SRAM MODULES

FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

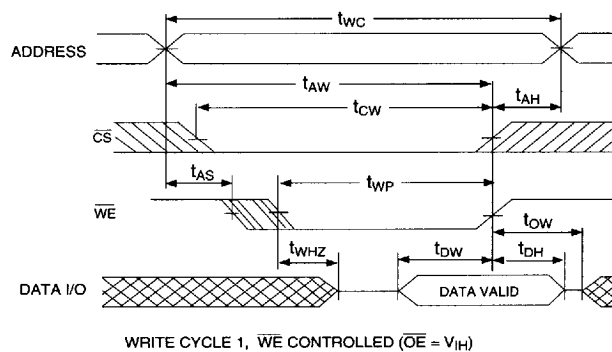
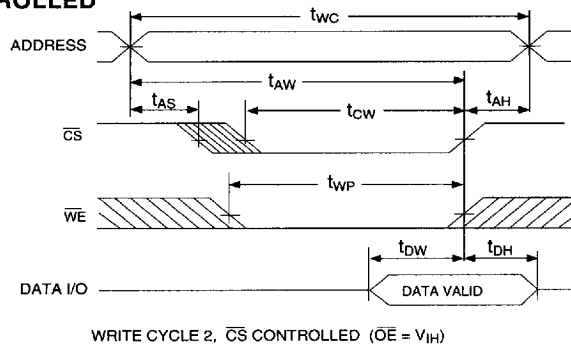


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED





ORDERING INFORMATION

W S 128K 8 - XXX C X

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

C = Ceramic .600" DIP (Package 302)

ACCESS TIME in nS

ORGANIZATION, 128K x 8

SRAM

WHITE MICROELECTRONICS

4

SRAM MODULES

Device Type	Speed	Package	SMD Number
128K x 8 SRAM	120nS	32 pin DIP	5962-93156 01HXX
128K x 8 SRAM	100nS	32 pin DIP	5962-93156 02HXX
128K x 8 SRAM	85nS	32 pin DIP	5962-93156 03HXX
128K x 8 SRAM	70nS	32 pin DIP	5962-93156 04HXX
128K x 8 SRAM	55nS	32 pin DIP	5962-93156 05HXX