DS3112-3.0

P1480

LAN CAM 1KX64-BIT CMOS CONTENT-ADDRESSABLE MEMORY

(SUPERSEDES SEPTEMBER 1993 EDITION - VERSION 2)

The P1480 LAN CAM is a 1K X 64-bit fixed-width CMOS Content-addressable Memory (CAM) aimed at address filtering applications in Local-area Network (LAN) bridges and routers. The architecture of the LAN CAM allows a network station list of any length to be searched in a single memory transaction. This device is also well-suited for other applications that require high-speed data searching such as optical and magnetic disk caches and data base accelerators.

Although the internal data path of the P1480 is 64-bits wide, the external interface is multiplexed four ways to allow communication with the device over a 16-bit bus. Vertical cascading and system flag generation require no external logic. The LAN CAM is synchronously controlled by four wires in much the same way as standard memories are controlled. A powerful instruction set increases the control flexibility and minimizes software overhead in typical systems. A data translation facility converts between IEEE 802.3 (CSMA/CD) and 802.5 (Token Ring) address formats on command. Both random access and associative operations are supported by this device. Flexible bit- and word-masking facilities enhance the associative operations. These and other features make the P1480 a powerful, yet easy to use, associative memory which drastically reduces data search delays.

FEATURES

- 1K X 64-bit CMOS Content-addressable Memory (CAM)
- 64-bit internal data path multiplexed four ways over a 16-bit I/O interface
- Simple four-wire synchronous control directly usable in conventional memory subsystems
- Extensive instruction set adds control flexibility Memory Array width can be configured as a mixture of CAM and RAM on 16-bit boundaries
- Memory operations allow random access, associative access, and write-at-next-free-address cycles
- Vertical cascading and system flag generation require no external logic
- Two Mask registers allow masking of individual bits for both writing and comparing
- Priority encoder returns highest-priority match address
- Device gives status information after each operation
- Two validity bits per location provide a word masking facility and valid or empty information

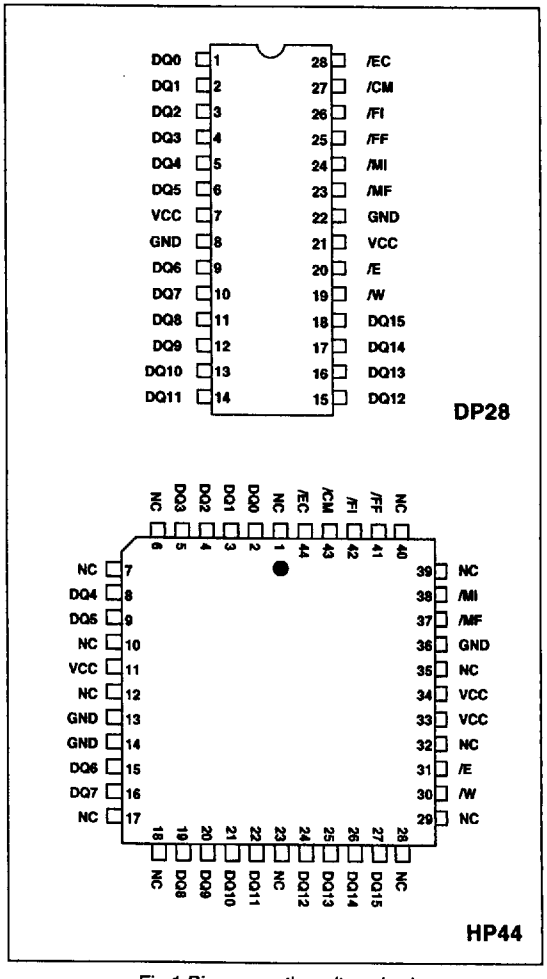


Fig.1 Pin connections (top view)

- Programmable data translation facility converts between IEEE 802.3 and 802.5 formats
- Manufactured in CMOS technology with TTL-compatible inputs and outputs
- Packaged in industry-standard 28-pin PDIP and 44-pin PLCC packages

ORDERING INFORMATION

PART NUMBER	CYCLE TIME	PACKAGE	TEMPERATURE RANGE
P1480-12CGDPAS	120ns	28-PIN PDIP	0-70°C
P1480-12CGHPAS	120ns	44-PIN PLCC	0-70°C
P1480-15CGDPAS	150ns	28-PIN PDIP	0-70°C
P1480-15CGHPAS	150ns	44-PIN PLCC	0-70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 to 7.0 Volts
Voltage on all Other Pins	–0.5 to V_{CC}+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	–40°C to +85°C
Storage Temperature	–55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Notes
1. Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.
2. All voltages are referenced to GND.

OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1"	2.0		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	see notes 2 and 3 below
T_A	Ambient Operating Temperature	0		70	°C	Still Air

Notes
1. All voltages referenced to GND at the device pin.
2. -1.0V for a duration of 10ns measured at 50% amplitude for Input-only lines (see Fig.9).
3. Common I/O lines are clamped so that signal transients cannot fall below -0.5V.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Conditions
I_{CC}	Average Power Supply Current		200	mA	
V_{OH}	Output Voltage Logic "1"	2.4		Volts	I_{OH} = -2.0 mA
V_{OL}	Output Voltage Logic "0"		0.4	Volts	I_{OL} = 4.0 mA
I_{IZ}	Input Leakage Current	-2	2	µA	$V_{SS} \leq$ VIN ≤ VCC
I_{OZ}	Output Leakage Current	-10	10	µA	$V_{SS} \leq$ VIN ≤ VCC; DQ_n = High Impedance

CAPACITANCE

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	6	pF	f=1MHz, V_{IN}=0V.
C_{OUT}	Output Capacitance	7	pF	f=1MHz, V_{IN}=0V.

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 volts
Output Timing Reference Level	0.8 to 2.4 volts

PIN DESCRIPTIONS

DQ0-DQ15 (Data Bus, Common I/O, TTL)

The DQ0-DQ15 lines convey data, commands and status to and from the P1480. The direction and nature of the information that flows to or from the device is controlled by the states of /CM and /W.

/E (Chip Enable, Input, TTL)

The /E input, the main clock control, enables the LAN CAM while LOW, latches the control signals /W, /CM, /EC on its falling edge and releases them on the rising edge, and clocks the Destination or Source Segment counter on its rising edge.

/W (Write Enable, Input, TTL)

The /W input selects the direction of data flow during a memory cycle. /W LOW selects a Write cycle, and /W HIGH selects a Read cycle.

/CM (Data/Command Select, Input, TTL)

The /CM input selects whether the inputs on the DQ0-DQ15 lines are data or commands. /CM LOW selects Command cycles and /CM HIGH Data cycles.

/EC (Enable Comparison, Input, TTL)

The /EC input enables the /MF output to show the results of a comparison. If /EC is LOW at the falling edge of /E in a given cycle, the /MF output is enabled. Otherwise, the /MF output is held HIGH.

/MF (Match Flag, Output, TTL)

The /MF output goes LOW when a valid match occurs during a Comparison cycle if the /EC line was latched LOW by the falling edge of /E at the start of the cycle.

/MI (Match Input, Input, TTL)

The /MI input is used in vertically cascaded systems to prioritize devices. In a daisy-chained system, the /MF output of one device is connected to the /MI input of the next lower-priority device in the chain.

/FF (Full Flag, Output, TTL)

The /FF output indicates that all the memory locations within the device contain valid contents. /FF LOW indicates the Full condition.

/FI (Full Input, Input, TTL)

The /FI input is used in vertically cascaded systems to generate CAM Memory System Full indication. In a daisy-chained system, the /FF output of one device is connected to the /FI input of the next-lower priority device in the chain.

V_{CC}, GND (Positive Power Supply and Ground)

These pins are the main power supply connections to the P1480. VCC must be held at +5V + 10% relative to the GND pin, which is at 0V (system reference potential), for correct operation of the device.

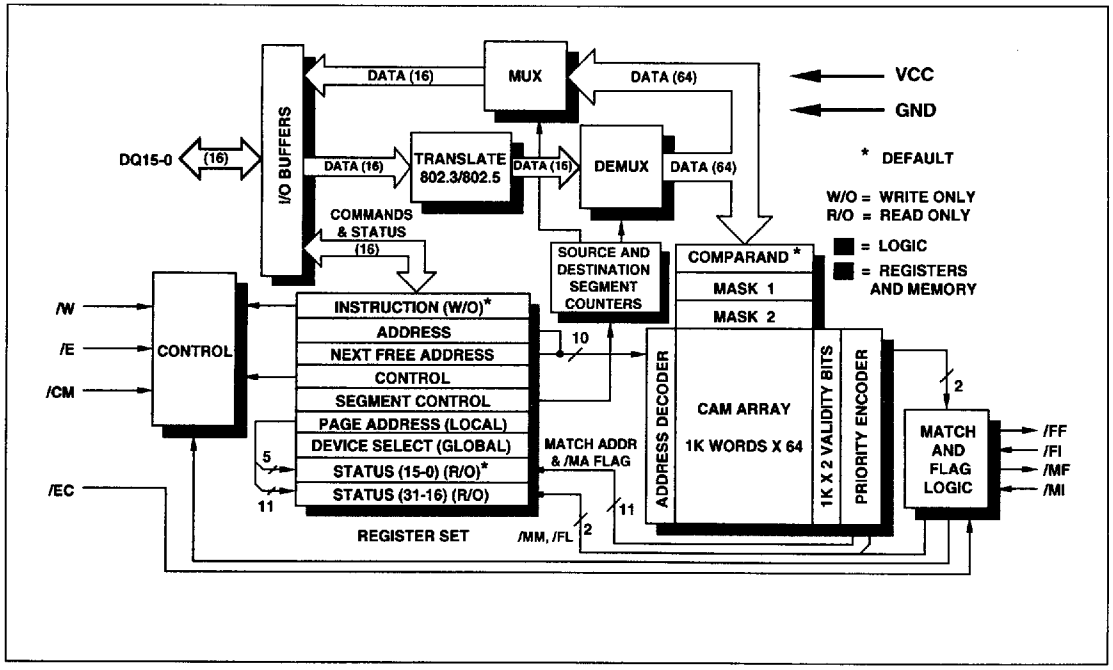


Fig.2 Block Diagram

FUNCTIONAL DESCRIPTION

The GEC Plessey Semiconductors' P1480 is a 1K x 64-bit CAM targeted at address filtering applications in Local-area Network (LAN) Bridges and Routers. The device is designed to hold the station list in the Bridge, allowing single-transaction decisions on whether to pass a data packet from one segment across the Bridge to another.

The P1480 is designed to minimize the external logic needed for expansion and control. It is controlled via four synchronous control signals and by commands loaded into an Instruction register. One of the control signals is used to indicate whether information present on the 16-bit input bus is to be interpreted as a Data or a Command field. During a Random Access cycle, the Address field is loaded into the Instruction Address register during a second Command Write cycle.

The data inputs and outputs of the P1480 are multiplexed four ways over a 16-bit I/O bus. This multiplexing increases the transaction time but allows the device to reside in a 28-pin package. The speed penalty related to the multiplexing is insignificant in the LAN Bridge environment because the address bits to be compared in the CAM are received serially from the network, so the loading is pipelined.

The P1480 contains 65,536 bits of static CAM, organized as 1024 64-bit Data fields. Each Data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. In LAN Bridges, the RAM subfield could hold port-address and time-out information, or other data associated with the Destination Address held in the CAM subfield of the location.

Appended to each 64-bit data field are two bits of CAM storage to indicate the validity of the location. These two bits are encoded to render four validity conditions: Valid data, Skip, Empty and Random access only.

The contents of the memory can be randomly accessed or associatively accessed. During a Data Comparison cycle, data is assembled in a Comparand register and is compared with the CAM section of the memory array. Only the locations whose Validity bits are set Valid will enter into comparison with the Comparand. Comparisons can also be done on the Validity bits themselves. Random access to the memory array, using an address to define a unique location, is independent of the state of the Validity bits.

The station list can be held in either the IEEE 802.3 or IEEE 802.5 format. When data is received from the network in other than the selected default storage format, the data bits can be translated during the loading process. This facility simplifies bridging between CSMA/CD and Token Ring networks.

Two Mask registers on the device can be selected to mask comparison or data writes. For comparison masking, data held in the selected Mask register determines which bits of the Comparand are compared against the valid contents. During a Write cycle, data in the designated Mask register selects which bits in the destination are written.

The Match line associated with each location is fed into a Priority encoder where multiple responses are resolved and the address of the highest-priority responder (lowest numbered physical address) is generated. In the LAN Bridge application a multiple response might indicate the existence of an error, whereas, in other applications, the existence of multiple responders may be a valid condition.

After a Comparison cycle, the Status register contains the address of the highest-priority responding location, along with flags indicating Match, Multiple Match and Full. The Match and Full flags are also available directly as output signals. These flags can be daisy-chained independently to provide system Match and Full indication without external logic.

A Page Address register simplifies vertical expansion in systems using more than one P1480. This register is loaded with upper-order address information during system initialization. During a Comparison cycle, the lower-order 10 bits of the Match address are fed to the Status register from the Priority encoder and are concatenated with the upper-order address bits from the Page Address register. The Device Select register is used to access a particular device in a vertically cascaded LAN CAM array. The address of the desired device is broadcast to all Device Select registers. Only the device whose Page Address register contains this address will respond to subsequent transactions.

A Control register sets up operating conditions within the P1480, such as Reset, enable or disable Match Flag, enable or disable Full Flag, set default data translation, CAM/RAM partitioning, disable or select masking condition, and disable or select address auto-increment or auto-decrement.

Source and Destination Segment counters within the P1480 control reading and writing 64-bit data. A Segment Control register sets the count limits for the Source and Destination Segment counters, and allows loading of values into each respective counter.

The P1480 is controlled by a combination of hardware signals and instructions loaded into the Instruction register. The instruction set offers a powerful, symmetrical control mechanism for causing the LAN CAM to perform the tasks commonly encountered in LAN Bridges and Routers. To facilitate the repetitive operations that are often desired, several instructions have persistent sources and/or destinations. In this way much of the software overhead that would otherwise be suffered is removed because operations done in a batch can be set up once and left in a given configuration until changed.

Larger LANs are commonly divided into more manageable segments that are joined by a Bridge to prevent excessive local traffic from degrading the overall network performance as shown in Fig.3 below. Segments can all be of the same protocol or can be of mixed protocols. The two major protocols of interest are IEEE 802.3 (Ethernet) and IEEE 802.5 (Token Ring).

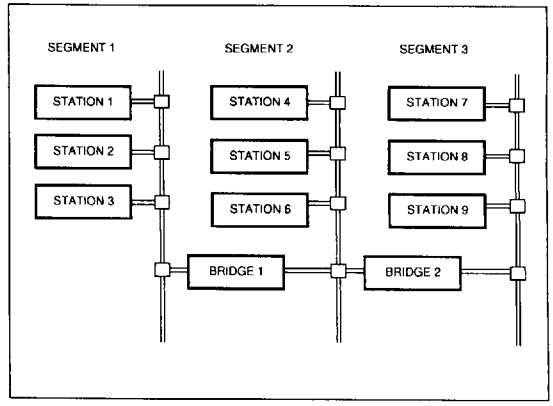


Fig.3 - LAN segments connected by bridges

The Bridge monitors the traffic on all of its segments to determine to which port a particular packet is aimed. This determination requires searching the destination address field (six bytes) in the packet and comparing it to those stored in the station list. A match provides associated information which the Bridge uses to route the packet correctly. A generic block diagram of a Bridge which would utilize one or more LAN CAMs to store and search the station list is shown in Fig.4. Using the LAN CAM radically reduces the search time and improves the Bridge's performance.

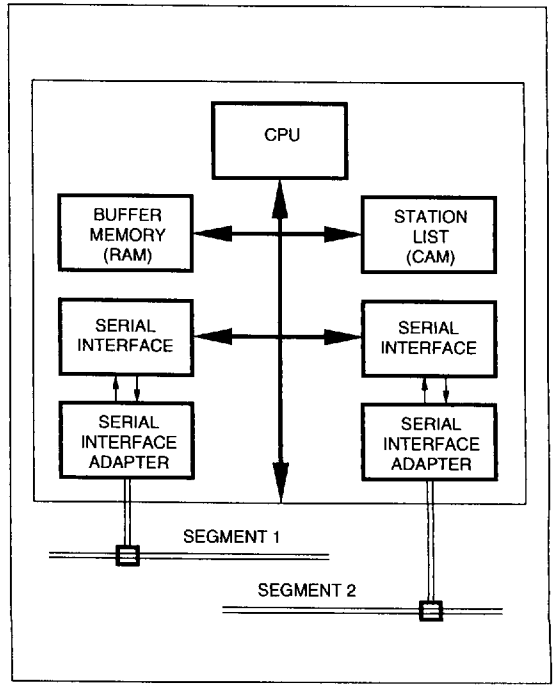


Fig.4 - Generic bridge block diagram

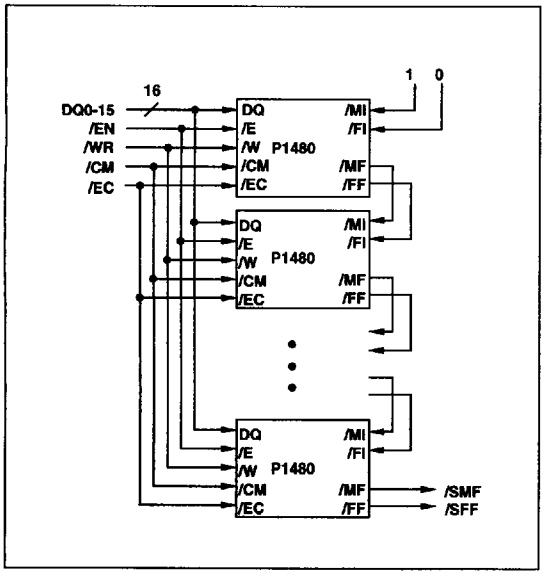


Fig.5 - Vertically cascading the LAN CAM

One P1480 can contain up to 1024 station list entries. For applications that require a larger station list, the LAN CAM is easily cascaded vertically without the need for external logic. Fig.5 below shows the connection scheme. Note that the flags are daisy-chained to generate the system flags without the need for external logic. Further, the Page register facility on the LAN CAM allows each device in the vertically cascaded chain to attach its own address in the event of a match in that device. This feature removes the need to construct an external priority encoder to calculate the complete match address. The fullness indication is also daisy-chained to permit the use of Associative writes which do not require a specific address. The P1480 can be instructed to Write at Next Free Address, even in a cascaded environment.

Table 1 illustrates the flow of a simple Compare operation assuming the LAN CAM is configured as 48 bits of CAM and 16 bits of RAM, any masking on the Compare and the Segment counters is already set up, Associated data is to be read back, and the Match address and the Match flag are to be read back through the Status register (the Associated Data and Status reads are optional and can be in either order). This search operation takes 270 ns to get a hardware flag indication and 450 ns to obtain both a Match address and Associated data, regardless of the length of the Station List. Fig.6 shows the cycle-to-cycle timing with the Match flag valid at the end of the third load cycle if /EC is LOW at the start of the third cycle. The fourth cycle reads status or associated data, depending on the state of /CM.

Duration	Operation	Controls and Flag /W	/CM	/EC	/MF
90ns	Load S1 COMPARAND	L	H	H	H
90ns	Load S2 COMPARAND	L	H	H	H
90ns	Load S3 COMPARAND	L	H	L	L
90ns	Read Associated Data*	H	H	H	H
90ns	Read Status Register*	H	L	H	H
450ns	Total	*sequence is arbitrary			

Table 1 - Station list search flow chart

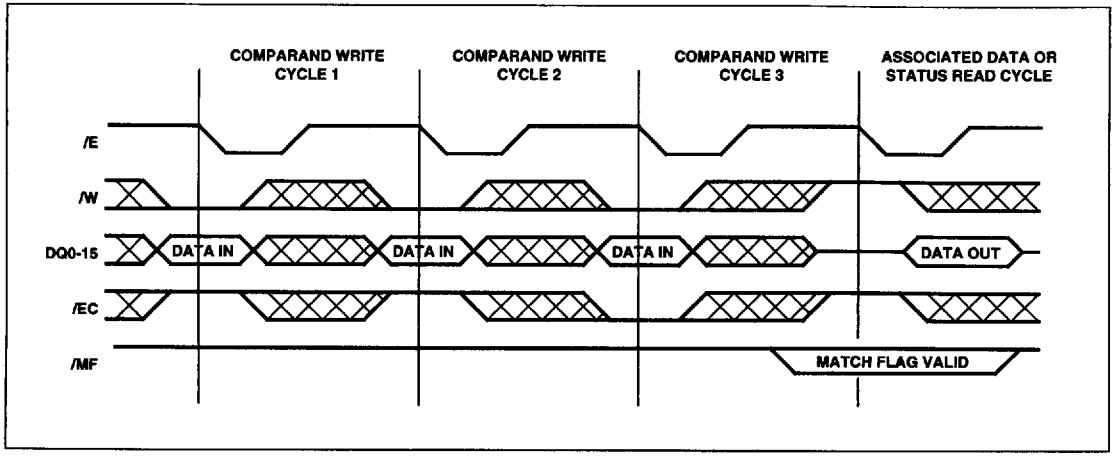


Fig.6 - Cycle-to-cycle timing

INSTRUCTION SET DESCRIPTIONS

A more complete description of the Instruction Set can be obtained in the P1480 LAN CAM Handbook (3113-1.3).

SELECT PERSISTENT SOURCE (SPS)

Binary Op Code	0000 f000 0000 0sss
f	Address Field Flag
sss	Selected Source

The SPS instruction selects a source for Data Reads. After instruction execution, the selected source persistently remains the source for Data Reads until another SPS instruction is executed or until a Reset occurs. The Comparand register is the default persistent source after power up or Reset.

SELECT PERSISTENT DESTINATION (SPD)

Binary Op Code	0000 f001 mmdd dvvv
f	Address Flag
mm	Mask Register Select
ddd	Selected Destination
vvv	Validity Setting if destination is a memory location

The SPD instruction selects a destination for Data Writes. Once this instruction is executed, the selected destination persistently remains the destination for Data Writes until another SPD instruction is executed or until a Reset. The Comparand register is the default destination for Data Writes.

When the selected destination is the Comparand register or the Memory array, the writing of data may be masked by the selected Mask register, Mask Register 1 or Mask Register 2. When the writing of data is masked, only those bits in the destination that correspond to bits containing 0's in the selected Mask register will be modified. Bits in the destination corresponding to bits containing 1's in the selected Mask register will remain unchanged.

Writing to the Comparand register or a Mask register causes a comparison to occur. Writing to the Memory array does not cause a comparison to occur. The next free address is generated when any instruction that could potentially affect the Validity bits is executed.

TEMPORARY COMMAND OVERIDE (TCO)

Binary Op-Code	0000 0010 00dd d000
ddd	Register selected as sourceor destination for only the next Command Read or Write cycle.

When a TCO instruction is executed, the temporarily selected register becomes the source or destination for only the next Command Read or Write cycle, respectively. Once either of those cycles occurs, subsequent Command Read or Write cycles revert to reading the Status register and writing the Instruction register during Command Reads or Writes. The special TCO PS or TCO PD instructions allow the user to read which persistent source or destination has been selected in the next Command Read cycle. If either of these instructions is followed by a Command Write cycle, no actionooccurs. Note that the TCO instruction permits access to the Instruction Address register for diagnostic purposes. Also, the Next Free Address register is Read Only, and Writes to the Page Address register invalidate the contents of the Status register.

DATA MOVE (MOV)

Binary Op-code	0000 f011 mmdd dsss or 0000 f011 mmdd dvss
f	Address Field Flag
mm	Mask Register select
ddd	Destination of Data
sss	Source of Data
v	Validity setting if destination is a memory location

The MOV instruction transfers the data in the selected source to the selected destination. Data transfers between the Memory array and the Comparand register may be masked by the selected Mask register, Mask Register 1 or Mask Register 2. If the transfer is masked, only those bits in the destination which correspond to bits containing 0's in the selected Mask register will be altered. Destination bits which correspond to bits containing 1's in the selected Mask register will remain unchanged.

The Validity bits of a Memory location used as a destination for a MOV instruction will be set to the Valid state or left unchanged, depending on the nature of the operation. If the source and destination are selected to be the same register in register-to-register operations, no net change to the state of the LAN CAM occurs. This operation would be equivalent to a NOOP.

VALIDITY BIT CONTROL (VBC)

Binary Op-code	0000 f100 00dd dvvv
f	Address Field Flag
ddd	Destination of data
vvv	Validity setting for Memory location

The VBC instruction sets the Validity bits to the selected state at the selected Memory location or locations. Validity bits can be accessed randomly or associatively. The VBC instruction can be used in conjunction with the appropriate Compare instruction to compare on any Validity condition. Hence, skipped locations can be returned to the Valid state after processing multiple matches by repeating the Compare operation using the Skip condition as the Validity field search criterion.

COMPARE (CMP)

Binary Op-code	0000 0101 0000 0vvv
vvv	Validity condition

The CMP instruction forces a Comparison after a cycle, such as a Memory Write cycle, which does not automatically result in a Comparison. Destinations to which Write cycles cause an automatic Comparison are the Comparand register, the Mask registers, the Control register.

The CMP E instruction forces the generation of the next free address. The Memory array at the next free address does not need to be a Persistent Destination. The CMP S instruction is used in conjunction with the VBC instruction to return all skipped locations to the Valid state after processing multiple matches. The CMP R instruction permits associative access to any Random-access-only Memory locations.

SET FULL FLAG (SFF)

Binary Op-code 0000 0111 0000 0000

The SFF instruction is a special instruction used to force the Full flag LOW for a device whose /FI input is LOW, but whose /FF output is HIGH. SFF is used in vertically cascaded systems for selecting each device in turn to initialize the Page Address register.

INSTRUCTION SET SUMMARY

MNEMONIC FORMAT: INS dst,src[msk],val

INS: Instruction mnemonic.
dst: Destination of the data.
src: Source of the data.
msk: Mask register used.
val: Validity condition set at the location written.

SELECT PERSISTANT SOURCE

Operation	Mnemonic	Op Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Address Reg	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Memory at Highest-priority Match	SPS M@HM	0005H

TEMPORARY COMMAND OVERIDE

Operation	Mnemonic	Op Code
Control Register	TCO CT	0200H
Page Address Register	TCO PA	0208H
Segment Control Register	TCO SC	0210H
Next Free Address Register	TCO NF	0218H
Instruction Address Register	TCO AR	0220H
Device Select Register	TCO DS	0228H
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

VALIDITY BIT CONTROL

Operation	Mnemonic	Op Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaaH,V	0C24H
Set Empty	VBC aaaH,E	0C25H
Set Skip	VBC aaaH,S	0C26H
Set Random Access	VBC aaaH,R	0C27H
Set Validity bits at Highest-priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

SELECT PERSISTANT DESTINATION

Operation	Mnemonic	Op Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1}	0140H
Masked by MR2	SPD CR[MR2}	0180H
Mask Register 1	SPD MR1	0108H
MaskRegister 2	SPD MR2	0110H
Memory at Address Reg set Valid	SPD M@AR,V	0124H
Masked by MR1	SPD M@AR[MR1],V	0164H
Masked by MR2	SPD M@AR[MR2],V	01A4H
Memory at Address Reg set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H
Memory at Address Reg set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Memory at Address Reg set Random	SPD M@[AR],R	0127H
Masked by MR1	SPD M@[AR][MR1],R	0167H
Masked by MR2	SPD M@[AR][MR2],R	01A7H
Memory at Address set Valid	SPD M@aaaH,V	0924H
Masked by MR1	SPD M@aaaH[MR1],V	0964H
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Address set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Memory at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Memory at Highest-prio. Match,Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH
Memory at Highest-prio. Match,Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Memory at Highest-prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH
Memory at High-prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Memory at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Memory at Next Free Addr.,Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Memory at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Memory at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

DATA MOVE

Operation	Mnemonic	Op Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Memory at Highest-prio Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Memory at Highest-prio Match	MOV MR1,HP	030DH
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Memory at Highest-prio Match	MOV MR2,HP	0315H
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaaH,CR	0B20H
Masked by MR1	MOV aaaH,CR[MR1]	0B60H
Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaaH,MR1	0B21H
Mask Register 2	MOV aaaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaaH,CR,V	0B24H
Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaaH,MR1,V	0B25H
Mask Register 2	MOV aaaH,MR2,V	0B26H

DATA MOVE (continued)

Operation	Mnemonic	Op Code
Memory at Highest-priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1]	0370H
Masked by MR2	MOV NF,CR[MR2]	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

COMPARE

Operation	Mnemonic	Op Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Compare Random Access Locations	CMP R	0507H

SPECIAL INSTRUCTIONS

Operation	Mnemonic	Op Code
Set Full Flag	SFF	0700H

SWITCHING CHARACTERISTICS

Note 4 (using AC test conditions)

No.	Symbol	Parameter	-120		-150		Units	Notes
			Min	Max	Min	Max		
1	tELE	Compare Cycle Time	120		150		ns	
2	tELEH	Chip Enable LOW Compare Pulse Width	100		120		ns	
3	tEHEL	Chip Enable High Pulse Width	20		30		ns	
4	tWHEL	Write Enable HIGH to Chip Enable LOW	0		0		ns	
5	tELWX1	Chip Enable LOW to Write Don't Care	15		15		ns	
6	tWLEL	Write LOW to Chip Enable Low	0		0		ns	
7	tELWX2	Chip Enable LOW to Write Don't Care	15		15		ns	
8	tCMVEL	Command Valid to Chip Enable LOW	0		0		ns	
9	tELCMX	Chip Enable LOW to Command Don't Care	15		15		ns	
10	tECVEL	Enable Comparison Valid to Chip Enable LOW	0		0		ns	
11	tELECX1	Chip Enable LOW to Enable Compare Don't Care	15		15		ns	
12	tELQX	Chip Enable LOW to Outputs Active	3		3		ns	2
13	tELQV	Chip Enable LOW to Data Valid		85		105	ns	2
14	tELQZ	Chip Enable HIGH to Outputs High-Z	3	20	3	25	ns	3
15	tDVEL	Data Valid to Chip Enable LOW	0		0		ns	
16	tELDX	Chip Enable LOW to Data Don't Care	15		15		ns	
17	tELFFV	Chip Enable LOW to Full Flag Valid		90		110	ns	
18	tFIVFFV	Full Input Valid to Full Flag Valid		7		7	ns	
19	tWVEL	Write Valid to Chip Enable LOW	0		0		ns	
20	tELWX3	Chip Enable LOW to Write Don't Care	15		15		ns	
21	tECLEL	Comparison Enable LOW to Chip Enable LOW	0		0		ns	
22	tELECX2	Chip Enable LOW to Enable Compare Don't Care	15		15		ns	
23	tEHMFV	Chip Enable HIGH to Match Flag Valid		30		35	ns	
24	tMIVMFV	Match in Valid to Match Flag Valid		7		7	ns	
25	tEHMFX	Chip Enable HIGH to Match Flag Invalid	0		0		ns	
26	tELELRW	Read/Write Cycle Time	95		105		ns	
27	tELEHRW	Chip Enable LOW Read/Write Pulse Width LOW	75		75		ns	

Notes:
1. Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
2. With load specified in Fig.7.
3. With load specified in Fig.8.
4. Over the operating temperature and voltage ranges.

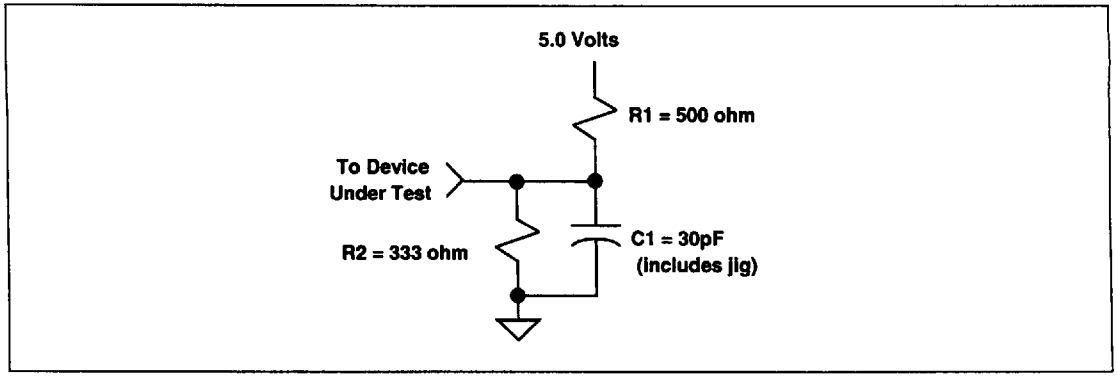


Fig.7 - AC test load

Test	Waveform - measurement level
Delay from output high to output high impedance	V_H 0.2V
Delay from output low to output high impedance	V_L 0.2V
Delay from output high impedance to Output low	1.5V 0.2V
Delay from output high impedance to Output high	1.5V 0.2V

V_H - Voltage reached when output driven high
V_L - Voltage reached when output driven low

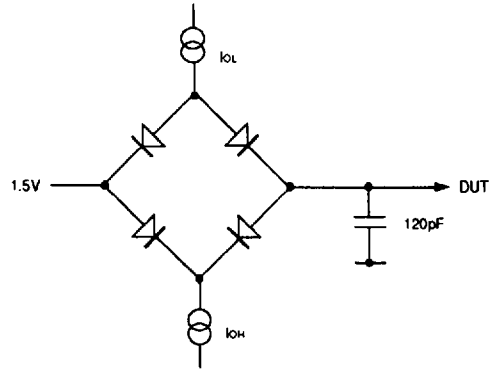


Fig.8 - Three state delay measurement

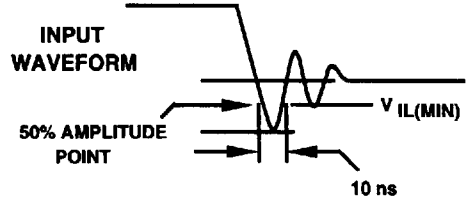


Fig.9 - Input signal waveform

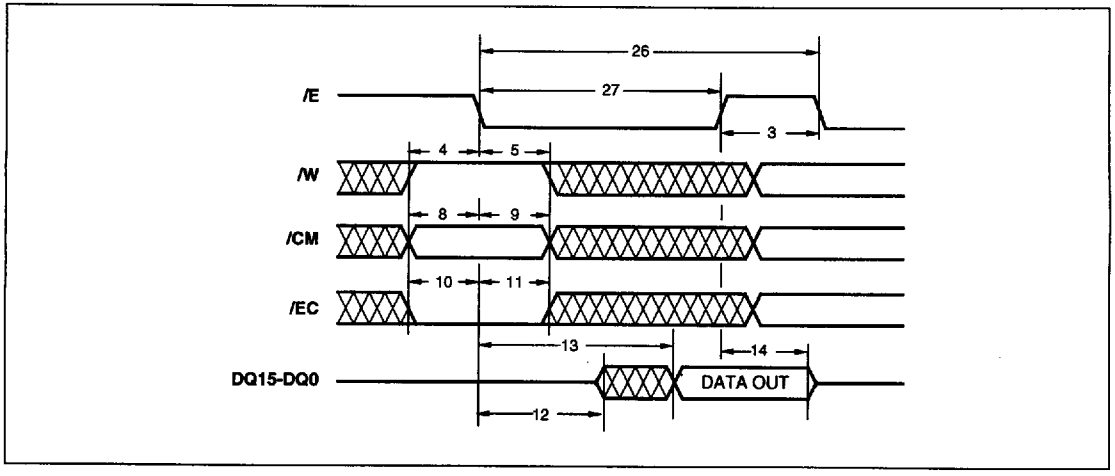


Fig.10 P1480 read cycle

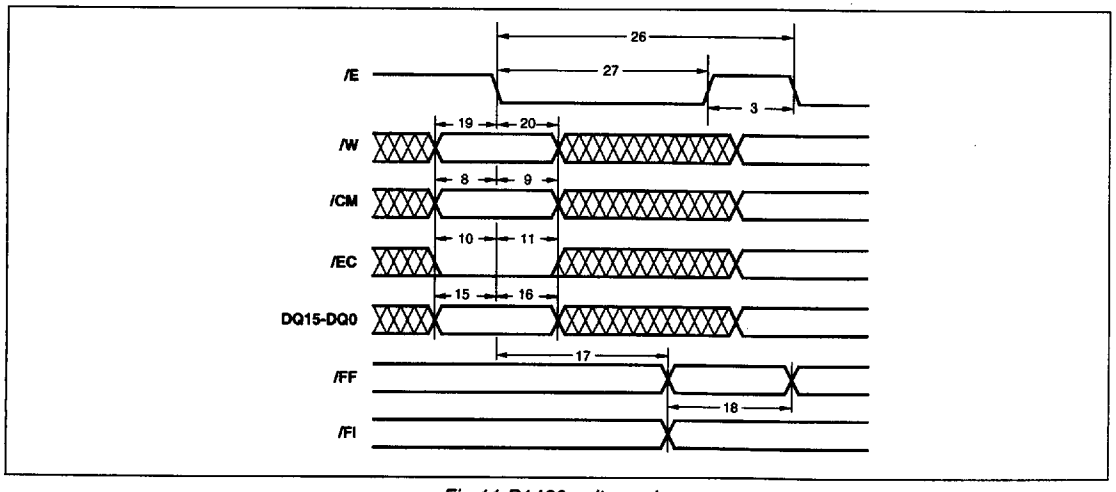


Fig.11 P1480 write cycle

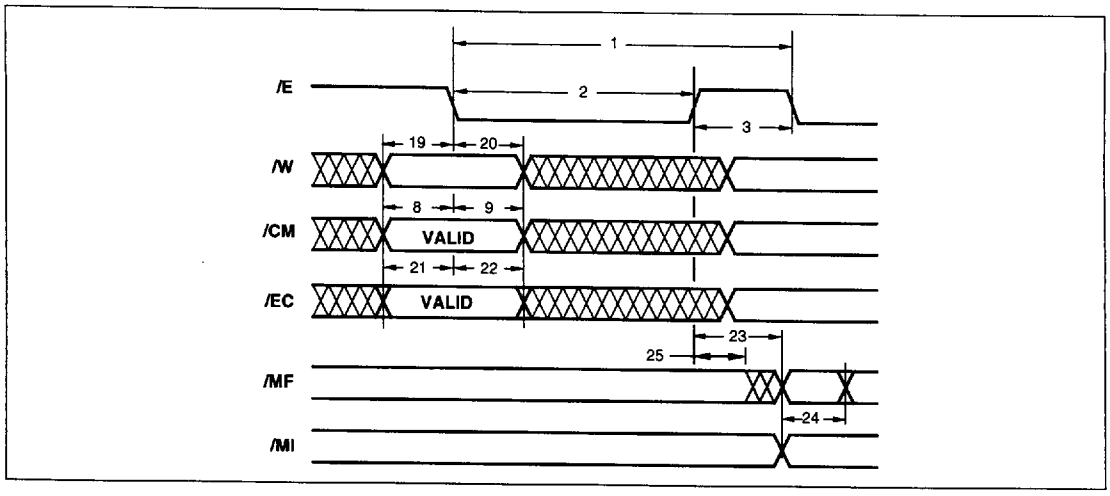


Fig. 12 P1480 match flag response

P1480 LAN CAM

1KX64-BIT CMOS CONTENT-ADDRESSABLE MEMORY HANDBOOK

CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The P1480 LAN CAM is a 1K x 64-bit Content-addressable Memory (CAM) which is targeted at address filtering applications in Local Area Network (LAN) Bridges. Although some of the aspects of this device are tuned specifically to the LAN Bridge environment, additional features are included to broaden its applicability. The P1480 could be applied in a wide range of systems where associativity is advantageous, such as LAN Routers, optical and magnetic disk cache memories and data base systems.

The data inputs and outputs of the P1480 are multiplexed four ways over a 16-bit I/O bus. Although this multiplexing increases the effective transaction time, the device can reside in relatively low-pin-count packages (28-pin PDIP and 44-pin PLDCC packages). The speed penalty related to the multiplexing is insignificant in the LAN Bridge environment because the search time using this device is many times faster than for other approaches. In other applications, the multiplexing may be seen as a drawback, but the performance advantage over conventional sequential search methods is so significant that the P1480 will still be applicable in such systems until other more tailored CAM devices become available.

The P1480 contains 65,536 bits of static CAM organized as 1,024 64-bit data fields plus 2048 CAM bits used as validity or status bits organized as 1024 two-bit fields (one two-bit status field for each 64-bit data field). Each data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. In other words, the memory array can be configured as 64 bits of CAM (default); 48 bits of CAM, 16 bits of RAM; 32 bits of CAM, 32 bits of RAM; 16 bits of CAM, 48 bits of RAM; or 64 bits of RAM. The CAM subfield contains the Associative data, while the RAM subfield contains the Associated data. In LAN Bridges, the RAM subfield could hold, for example, port-address and aging information related to the destination-address or source-address information held in the CAM subfield of a given location.

Appended to each 64-bit data field are two bits of CAM storage to indicate the validity of the location. These bits are referred to as the Empty and Skip bits. The Empty bit is used to indicate whether or not the location contains valid data, while the Skip bit is used to withdraw a valid content from comparison on a temporary basis. These two bits are encoded to render four validity conditions: Valid data, Skip, Empty, and Random access only.

The contents of the memory can be randomly accessed or associatively accessed. During a Comparison cycle, data is assembled in a Comparand register and is compared with all valid entries in the CAM section of the memory array simultaneously. Only the locations with their Validity bits set to the valid condition will enter into comparison with the Comparand. Random access to the memory array, using an address to define a unique location, is independent of the setting of the Validity bits.

When bridging between an Ethernet network and a Token Ring network, the station list can be held in either the IEEE 802.3 (Ethernet) or IEEE 802.5 (Token Ring) format. The data can be written into the Comparand register in either a transformed or non-transformed way. The bit transformation corresponds to the destination-address bit translation between IEEE 802.3 and IEEE 802.5 formats. This facility simplifies bridging between CSMA/CD and Token Ring networks. When an address is received from the network that does not correspond to the selected default storage format, the address bits can be transformed during the loading of the Comparand register. The address can then be compared and/or stored in the default format without any external logic.

Two Mask registers exist on the chip that can be selected to mask comparison or data writes. For comparison masking, data held in the selected Mask register determines which bits of the Comparand are compared against the valid contents. If a bit is set HIGH in the Mask register, the corresponding bit position in all locations is forced to a true comparison condition. During a Write cycle, data in the selected Mask register determines which bits in the destination are updated. If a bit is HIGH in the Mask register, the corresponding bit of the destination remains unchanged during the Write cycle.

The Match line associated with each location is fed into a Priority encoder where multiple responses are resolved and the address of the highest-priority responder is generated. In the LAN Bridge application, a multiple response can indicate the existence of an error, whereas, in other applications, the existence of multiple responders may be a valid condition.

The P1480 is controlled via four input control signals and by commands loaded into an Instruction register. One of the four input control signals is used to indicate whether information present on the 16-bit input bus is a data input or output or a command input or status output. During a random access cycle, the address field is loaded into the Instruction Address register during a second of two consecutive Command Write cycles. A Status register provides access to the resultsoof an associative cycle.

After a Comparison cycle, the Status register contains the address of the highest-priority responding location, along with flags indicating Match, Multiple Match and Full. The Match and Full flags are also available directly as output signals. These hardware flags can be daisy-chained independently to provide System Match and System Full indications in vertically cascaded LAN CAM arrays. In such arrays, if no match is found after a comparison, access to the Status register is denied, so the hardware flag must be used to check for the no-match condition.

A Page Address register is provided to simplify vertical expansion in systems using more than one P1480. This register is loaded with upper-order address information during system initialization. During a Comparison cycle, the 10 bits of the Match address in a given device are fed to the Status register from the Priority encoder and are appended to the upper-order address bits from the Page Address register.

A Device Select register allows the user to target a specific device within a vertically cascaded system. This register also simplifies system initialization and permits context-specific processing in the CAM memory system.

A Control register is used to set up persistent operating conditions within the P1480. Conditions set by the contents of this register are Reset, enable or disable Match Flag, enable or disable Full Flag, set default address format, CAM/RAM organization select, enable or disable or select masking conditions, enable or disable or select address autoincrement or autodecrement operations.

Two Segment counters are present in the P1480, one to control the writing of 64-bit data to the device (Destination Segment counter), and one to control the reading of 64-bit data from the device (Source Segment counter). A Segment Counter Control register sets the count limits for the Destination and Source Segment counters and can load preset values into each respective counter.

1.2 DISTINCTIVE CHARACTERISTICS

- 1K X 64-bit CMOS Content-addressable Memory (CAM)
- 64-bit internal data path multiplexed four ways over a 16-bit I/O interface
- Simple four-wire synchronous control directly usable in conventional memory subsystems
- Extensive instruction set for added control
- Memory Array width can be configured as a mixture of CAM and RAM on 16-bit boundaries
- Memory operations allow random access, associative access, and write-at-next-free-address cycles
- Vertical cascading and system flag generation require no external logic
- Two Mask registers allow masking of individual bits for both writing and comparing
- Priority encoder returns highest-priority match address
- Device gives status information after each operation
- Two validity bits per location provide a word masking facility and valid or empty status
- Programmable data translation facility converts between IEEE 802.3 and 802.5 formats
- Manufactured in CMOS technology with TTL-compatible inputs and outputs
- Packaged in industry-standard 28-pin DIP and 44-pin PLCC Packages

1.3 INTRODUCTION TO CAMS

Content-addressable Memories (CAMs), also known as Associative Memories, operate in the converse way to their counterparts, Random Access Memories (RAMs). In a RAM an address is presented to the device, and the unique location pointed to by the address is accessed; data may be read from or written to the selected location according to the logical state of the control inputs.

In a CAM, data is presented at the inputs and the address where that data resides is generated and appears at the outputs in a single transaction. A flag is also generated to indicate whether that data was present amongst the values stored in memory. Data values stored in a CAM are referred to as the Contents. Alternatively, Associated data may be accessed instead of the matching address value. Under this circumstance, the incoming data, referred to as the Comparand, can be thought of as an address field representing a noncontiguous address space. In this mode of operation, CAMs are ideally suited to Cache memory applications.

The CAM can act as a search engine. The same task can be performed in a RAM under software control, but with reduced performance. In a RAM, each location must be searched sequentially, the data must be read into the CPU where it is compared against the value being searched; if the accessed value does not match with the template, the next address must be accessed. This process continues either until a match is found, or until a search boundary is reached. On average, half the memory locations of the search list will be accessed per sequential search task. This algorithm is not only time consuming, but the time needed to generate a result is also unpredictable. The CAM will generate a result in a single transaction regardless of the length of the list being searched.

Although the associative operation of a CAM is very different from operations in a RAM, CAMs can also be randomly accessed, a useful characteristic for reading or writing the Contents to the CAM. The CAM Contents can be read and written as a function of address or of associativity. Writing can also be done to the next free address.

Because associative access is to all addresses, there is a potential for more than one location to respond at a time. Multiple Responders, or Ambiguity, is unique to CAMs; in a RAM only a single location is accessed per transaction, as defined by the input address. In a CAM, a mechanism called the Priority Encoder must be included to resolve multiple responses. The Priority Encoder generates the address of the highest-priority responding location.

The concept of Content-addressable Memories was first described in a paper by A.E. Slade and H.O. McMahon in 1956, 'A Cryotron Catalog Memory System.' Since then there has been little commercial exploitation of the technique. Many applications have been suggested for CAMs in the literature, including: data base acceleration, sonar and radar processing, cache memories and artificial intelligence.

With the market drive towards Memories, and with the advent of dense CMOS manufacturing processes, CAMs have become economically feasible for specific applications. The P1480 targets the specific application of destination address recognition in local area network Bridges and Routers, although it is suitable for a wide range of other applications where data searching is a bottleneck to system throughput.

1.4 THE LOCAL AREA NETWORK BRIDGE

Local Area Networks (LANs) have become a popular way of connecting computers together so that they can share and exchange data. There are a number of well established LAN standards, most notably Ethernet (IEEE 802.3), and Token Ring (IEEE 802.5).

High levels of traffic on networks can greatly diminish the efficiency of their operation. One way to keep traffic levels down is to limit the number of nodes on the network. Clearly, this solution imposes an unacceptable restriction. An improved solution is to divide the network into segments with a small number of nodes on each segment. These segments can then be connected to form the complete network.

A network may be divided into segments for reasons of convenience, as in the case of one office being on one segment with many offices in the building, all interconnected on the network. Alternatively, the network may be segmented because of physical constraints, such as the distance between groups of stations, or the number of stations in the overall network. Also, the performance of individual segments of the network can be improved if the majority of the traffic is local to each segment, as in intra-office communication with only the occasional inter-office data transfer. The response time of one single large network would be worse than the segmented network in this case.

A large network comprising smaller segments is desirable if the segment interconnection can be efficiently done. The nature of the communication channel between networks is succinctly described by the Extended Network ISO (International Standards Organization) Model. Fig. 1-1 shows the layers at which communication takes place between networks.

At the highest level of the ISO model, the Application layer, the Gateway provides communication that is independent of the physical nature of the network. At a lower level, the Router determines which of a number of possible routes through the network a particular packet takes. Therefore, the Router must have knowledge of the topology of the network, and that topology may change as a function of time. The P1480 can be used in the Router to hold routing strategies as well as destination- and source-address information.

At the Data Link layer, the Bridge handles inter-network communication between segments. At the lowest level, the Repeater serves simply to amplify signals along signal paths that are longer than those prescribed in the standard specification of that particular network.

A LAN Bridge connects two or more segments and decides to which segment to send a data packet based on the destination address. Fig. 1-2 shows three network segments linked by two bridges, each segment having three stations.

When one station wants to communicate with another, it sends a data packet using a protocol specific to the particular network. For example, an Ethernet frame consists of a six-byte destination address, followed by a six-byte source address, followed by a two-byte type field which specifies the higher-level protocol to be used to interpret the frame contents, followed by 46 to 1500 bytes of data, followed by a four-byte frame check sequence.

The Bridge recognizes the data transmission on one of its segments and captures and compares the destination address with its stored station list. If the destination station is found to reside on the other segment, the Bridge passes the packet across. The Bridge learns the network by comparing Source addresses with its station list.

In Bridge designs to date, the station list has been searched sequentially for the destination address. This operation is a time consuming operation where the response time varies according to where the target address resides in the station list and how long the station list is. The length of the station list is a measure of the size of the overall network and can be quite large (16K or more entries). Moreover, during network initialization when the bridge is 'learning' the station addresses from the source addresses and creating the station list, the entire list must be searched before establishing the absence of the incoming address. Therefore, the response time of the network is even more adversely affected by the sequential search during initialization.

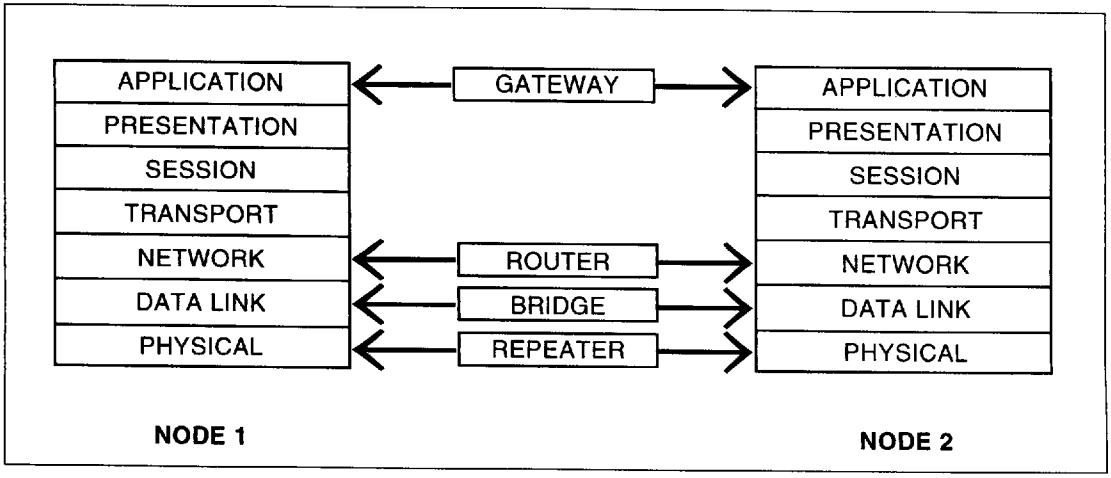


Fig. 1-1 - Extended Network ISO Model

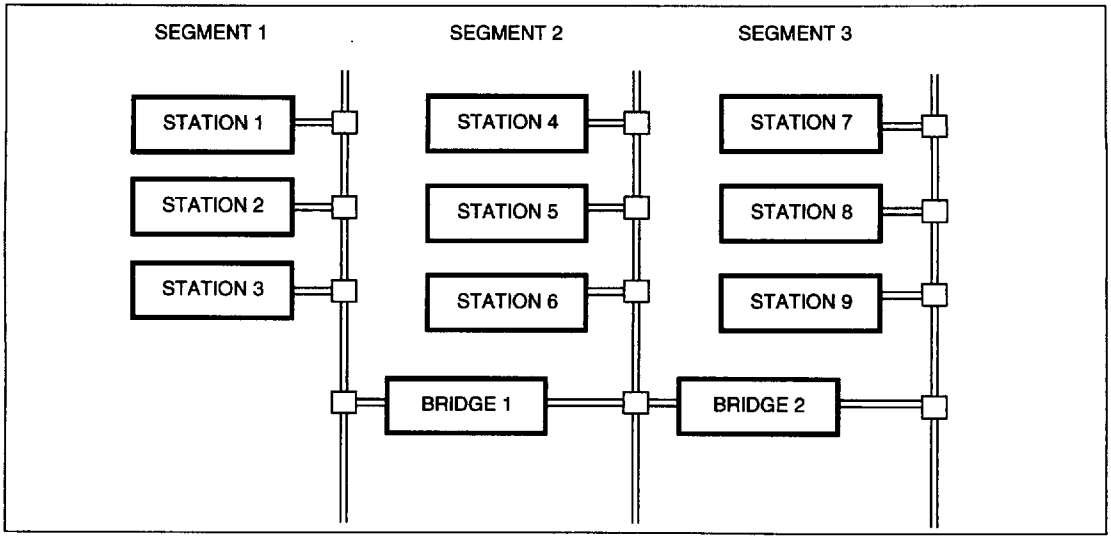


Fig. 1-2 - LAN Segments Connected by Bridges

Clearly, the sequential station-list search operation represents a severe bottleneck both during initialization and during normal operation of the network. Some improvement can be realized if the list is pre-sorted. In this approach, the search time becomes logarithmic as a function of list length. However, many search transactions are required, and the search time still varies with list length. The P1480 is designed to perform the station-list search in a single transaction. Not only does this device speed up the search operation dramatically, but it also responds in a predictable time. The station list is written into the CAM array. The destination address of the packet being transferred forms the Comparand. The Comparand is compared simultaneously with all destination addresses held in the CAM, and a match or no-match result is found in one such Comparison transaction.

The architecture of the P1480 is tailored to the LAN Bridge application. The 64-bit field width of the P1480 can be configured as an area of CAM and an area of RAM on 16-bit boundaries. In the LAN Bridges, an organization of 48 bits of CAM and 16 bits of RAM is selected. The RAM bits are accessed as a function of the Matching location in the CAM field. This associated data could hold, for example, the Bridge Port address, Segment status, Access conditions, and Station aging data. Thus, the Bridge can decide whether and where to send the data packet based on this data.

The simplest Bridge designs have two ports and link only between two segments; but a trend towards multi-port bridges with dissimilar segments has begun. By ascribing a number of bits of the associated data field to a Bridge Port address, the P1480 can support future-generation Bridge design philosophy.

Fig. 1-3 shows a simplified block diagram of a LAN Bridge. The Serial Interface adapters drive the coaxial cable links with the defined signal levels, while the Serial interface assembles parallel data to and from serial bit streams. If the Bridge cannot gain immediate access to the destination segment, the buffer memory allows the entire frame to be captured and held until the destination segment becomes available.

When destination-address recognition is fast enough, little or no data buffering may be necessary. This desirable situation is referred to as 'cut-through', and allows the bridge to route the data packet directly from one segment to the otherwwithout the need for temporary data storage, provided that no collision is detected on the destination segment. The P1480 LAN CAM makes cut-through feasible. The station list is held in one or more vertically cascaded P1480s. The operation of the bridge is controlled by the CPU.

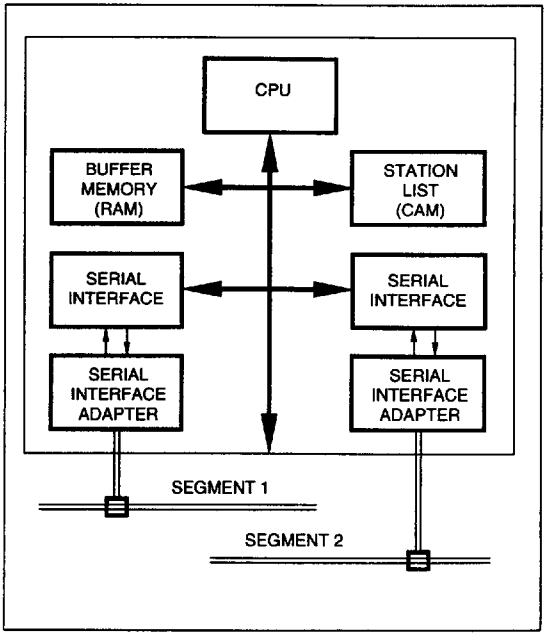


Fig. 1-3 - Generic Bridge Block Diagram

CHAPTER 2
HARDWARE INTERFACE

2.1 PIN DESCRIPTIONS

The LAN CAM pin assignments for the 28-pin DIP and for the 44-pin PLCC are shown in Fig. 2-1. In the following description of the pin functions of the P1480, the positive logic convention is observed. Specifically, a logic LOW corresponds to a Boolean logic "0", and is represented by a voltage level between VIL(min) and VIL(max) for an input, and between VOL(min) and VOL(max) for an output. Conversely, a logic HIGH corresponds to a Boolean "1", and is represented by a voltage level between VIH(min) and VIH(max) for an input, and between VOH(min) and VOH(max) for an output. All voltages are referenced to GND at the device pins.

DQ0-DQ15 (Data/Command Bus, Three-state Common Input/Output, TTL)

The DQ0-DQ15 lines convey data, commands, and status to and from the P1480. The state of the /W input determines whether data flow into or out of the device, while the /CM input determines whether the information on the DQ0-DQ15 lines is interpreted as data or a command or status. Several sources of data and destinations for data exist within the P1480.

In the Command mode (/CM is LOW), the default destination of the information input on the DQ0-DQ15 lines during a Command Write cycle (/W is LOW) is the Instruction register; during a Command Read cycle (/W is HIGH), the default source of the data output on the DQ0-DQ15 lines is the Status register. These default conditions can be overridden by an instruction in favor of the Instruction Address register, the Control register, the Page Address register, the Device Select register, the Next-free-address register, and the Segment Control register.

For Data cycles (/CM is HIGH) the destination of the data input on DQ0-DQ15 during a Data Write cycle (/W is LOW) is the persistently selected one of the following: the Comparand register (default), Mask Register 1, Mask Register 2, or the Memory array. During a Data Read cycle (/W is HIGH) the source of the information output on DQ0-DQ15 is the persistently selected one of the following: the Comparand register, Mask Register 1, Mask Register 2, or the Memory array.

/E (Chip Enable, Input, TTL)

The /E input is the main clock control input of the P1480. It enables the P1480 while LOW, registers the control signals on its falling edge, and clocks the Destination or Source Segment counter on its rising edge.

/E is also used in timing the locking and unlocking of the daisy chain in vertically cascaded systems. The daisy chain is locked on the rising edge of /E during the cycle in which /EC is LOW at the falling edge of /E; correspondingly, the daisy chain is unlocked on the rising edge of /E during the cycle in which /EC is HIGH at the falling edge of /E.

When /E is HIGH, the device is disabled and standby power is consumed, the output buffers are in their high-impedance state, and neither data nor commands can be written to the device, regardless of the state of /W. When the /E input is LOW, the device is enabled for normal operation and active power is consumed.

/W (Write Enable, Input, TTL)

The /W input selects the direction of data transfer during a memory cycle. The state of the /W input is registered on the falling edge of /E. When /W is registered HIGH, data are output from the selected source within the P1480. When the /W input is registered LOW, data are written into the selected destination within the device. When /W is registered LOW, the output buffers remain in the high-impedance state.

/CM (Data/Command Select, Input, TTL)

The /CM input selects whether the information on the DQ0-DQ15 lines is interpreted as data or as a command or status. The state of the /CM input is registered on the falling edge of /E. When /CM is HIGH, the data present on the DQ0-DQ15 lines are written into the persistently selected destination during a Data Write cycle (/W is LOW) or is read from the persistently selected source during a Data Read cycle (/W is HIGH).

When /CM is LOW, the data present on the DQ0-DQ15 lines are written by default into the Instruction register during a Command Write cycle (/W is LOW) or is read by default from the Status register during a Command Read cycle (/W is HIGH). These default conditions can be overridden by an instruction in favor of the Instruction Address register, the Control register, the Page Address register, the Device Select register, the Next-free-address register, or the Segment Control register.

/EC (Enable Comparison, Input, TTL)

The /EC input locks and unlocks the daisy chain in a vertically cascaded system. It is registered internally by the falling edge of /E, and is synchronized with the rising edge of /E. If /EC is LOW at the falling edge of /E, the results of a comparison are conveyed via the /MF output. While /EC is HIGH on consecutive cycles, the /MF flag will remain HIGH regardless of the results of the comparison. While /EC is LOW on consecutive cycles, the /MF output will go LOW if enabled in the Control register, and if the /MI input is LOW, or a true comparison results between the value held in this particular Comparand register and one or more of the contents of the CAM section. When the state of /EC changes from LOW to HIGH at the start of a cycle, the /MF output will go HIGH after the rising edge of /E of that cycle.

/MF (Match Flag, Output, TTL)

The /MF output is the Match flag which indicates whether a valid match has occurred during a Comparison cycle. The /MF output is only active when enabled in the Control register in a cycle when the /EC line was LOW at the falling edge of /E at the beginning of that cycle; the /MF output will not go LOW until after the rising edge of /E during that cycle.

Similarly, when /EC was HIGH at the falling edge of /E at the beginning of a subsequent cycle, the /MF output will go HIGH after the rising edge of /E during that cycle.

If the /MF output is enabled by the Control register, /EC, and /E and is HIGH at the end of a Comparison cycle, there was no match between the unmasked portion of the value held in the Comparand register and any of the valid contents of the CAM array. If the /MF output is LOW, there was at least one match between the unmasked portion of the value held in the Comparand register and the valid contents of the CAM array in this or an up-stream device.

The /MF output can be deactivated by the Flag Disable state in the Control register. The /MF output will remain HIGH even if there is a valid match during a Compare cycle. When active, the /MF output will also go LOW if the /MI input goes LOW, even with no Match in that specific device.

/MI (Match Input, Input, TTL)

The /MI input is used in daisy-chained, vertically cascaded systems to prioritize devices within the CAM memory system. When the /MI input is HIGH, the /MF output state is determined by the state of /EC and by the internal Match condition. When /MI is LOW, the /MF output will be forced LOW whenever /EC was LOW at the start of the cycle. In a daisy-chained system, the /MF output of one device is connected to /MI input of the next-lower-priority device.

/FF (Full Flag, Output, TTL)

The /FF output is the Full flag which indicates when none of the memory locations are Empty. When the /FF output is HIGH, there is at least one empty location, or the /FI input is HIGH. When the /FF output is LOW, no locations are empty. The /FF output can be deactivated by the Control register in which case the /FF output will remain HIGH even if no locations are empty.

/FI (Full Input, Input, TTL)

The /FI input is used in daisy-chained, vertically cascaded systems to generate a CAM Memory System Full indication. When the /FI input is HIGH, the /FF output is forced HIGH. When /FI is LOW, the /FF output will be HIGH if that device is not full, and will be LOW if that device is full. In a daisy-chained system, the /FF output of one device is connected to /FI input of the next-lower-priority device.

VCC, GND (Positive Power Supply, Ground)

These pins are the main power supply connections to the P1480. VCC must be held at +5V +10% relative to the GND pin, which is at 0V (system reference potential), for correct operation of the device.

2.2 BLOCK DIAGRAM DESCRIPTION

Referring to the block diagram of the P1480 shown in Fig. 2-2, the DQ0-DQ15 Data I/O bus enters the device via an I/O buffer. A Control bus comprising Chip Enable (/E), Write Enable (/W), Command Enable (/CM) and Enable Comparison (/EC) inputs controls the operation of the device, along with instructions loaded into an Instruction register.

The Control bus and the Instruction register are fed to the Control block and Flag Logic Block which control the internal functions of the device. The Source and Destination Segment counters control the multiplexing and demultiplexing of the 16-bit I/O data to and from the 64-bit internal bus. The Segment Control register allows the count limits of the two Segment counters to be set independently, and preset values to be loaded into or read from the counters.

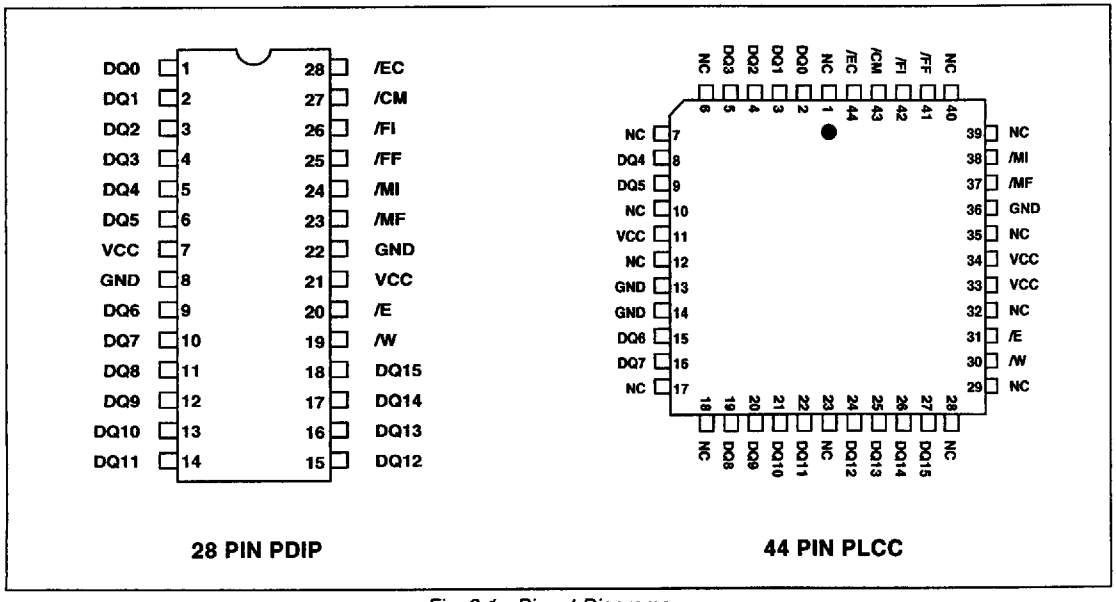


Fig. 2-1 - Pinout Diagrams

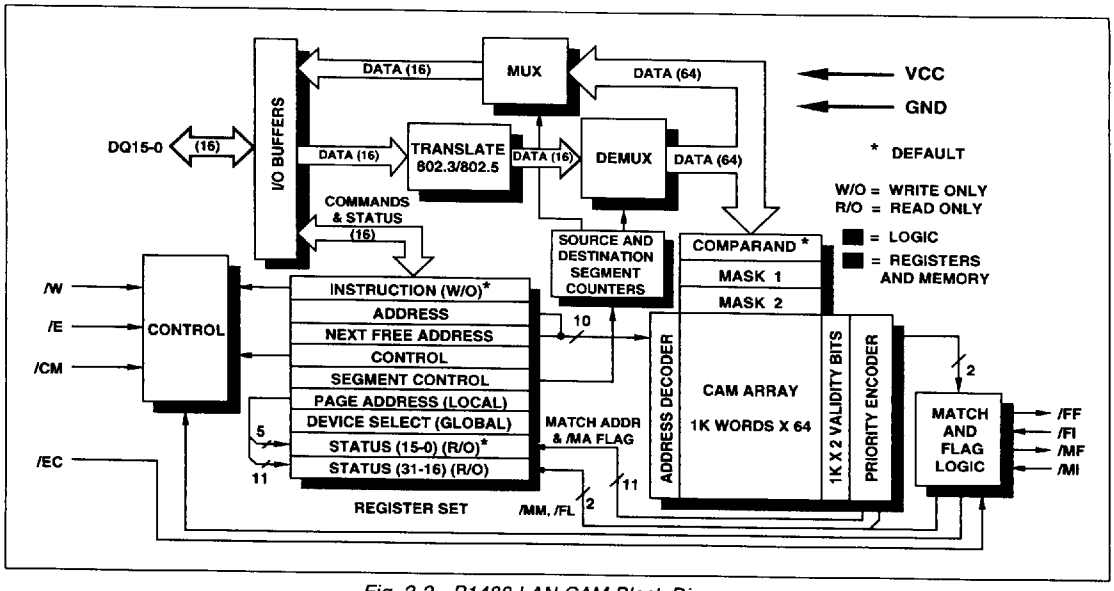


Fig. 2-2 - P1480 LAN CAM Block Diagram

Two flags are outputs: the Match flag (/MF) indicates if a valid match has occurred during a Comparison cycle between the contents of the Comparand register and one or more of the unmasked portion of the contents of the CAM array; and the Full flag (/FF) indicates if all the CAM locations are filled with data. These active-LOW flags can be deactivated independently through the executionoof an instruction, causing them to remain HIGH regardless of the internal state of the P1480.

The output flags are also affected by the /MI and the /FI inputs. These two inputs are used to daisy chain multiple LAN CAM devices in a vertically cascaded system. If the /MI input is LOW, a higher-priority device in the chain has a valid match. If the /FI input is LOW, all the devices in the chain above are full. The daisy chain allows the highest-priority responding P1480 in the system to be accessed.

The internal 16-bit data bus is connected to the I/O buffer, the Instruction register, the Instruction Address register, the Page Address register, the Device Select register, the Control register, the Segment Control register, the Status registers, the Next-free-address register, the 802.3/802.5 Format translator, and the Output multiplexer. Internal 64-bit data are multiplexed and de- multiplexed between the 16-bit and 64-bit buses.

During a Command Write cycle (/CM is LOW, and /W is LOW), the data on the 16-bit data bus are written into the Instruction register to control subsequent operation of the device. Should the instruction dictate access to a specific location in the Memory array, the address is loaded into the Instruction Address register during the next cycle which must also be a Command Write cycle.

The loading of the Instruction register can be temporarily overridden for one Command Write cycle by loading a Temporary Command Override (TCO) instruction into the Instruction register. The next cycle must be a Command Write cycle which will load the Control register, the Page Address register, the Device Select register, the Instruction Address register, the Next-free-address register, or the Segment Control register, depending on which was selected by the TCO instruction. Subsequent Command Write cycles will revert to loading the Instruction register, until again overridden for one cycle by a TCO instruction.

During a Command Read cycle (/CM is LOW, and /W is HIGH), the lower-order 16 bits of the Status register are placed onto the internal 16-bit data bus and are sent to the DQ0-DQ15 bus via the I/O buffer. If the upper-order 16-bits of the Status register are required, they are accessed if the next cycle is also a Command Read cycle. If the next cycle is not a Command Read cycle, a later Command Read cycle will again access the lower-order 16 bits of the Status register.

Access to the Status register can be temporarily overridden for one Command Read cycle by loading a TCO instruction into the Instruction register. The next cycle must be a Command Read cycle which will access the Control register, the Page Address register, the Device Select register, the Instruction Address register, the Next-free-address register or the Segment Control register, depending on which was selected by the TCO instruction. Subsequent Command Read cycles will revert to accessing the Status register, until again overridden for one cycle by a TCO instruction.

During a Data Write cycle (/CM is HIGH, and /W is LOW), data are transferred to one of a number of destinations from the DQ0-DQ15 lines. The default destination of the data is the Comparand register. The other data destinations that can be selected by executing a Select Persistent Destination instruction are Mask Register 1, Mask Register 2, or the Memory array.

The Comparand register, the two Mask registers and each location in the Memory array hold 64 bits of data and are loaded via the Demultiplexer over one, two, three, or four cycles, depending on the start-count and end-count values set for the Destination Segment counter. During loading from the I/O port, the data can be translated between IEEE 802.3 and IEEE 802.5 formats.

During a Data Read cycle (/CM is HIGH, and /W is HIGH), data are transferred from one of a number of sources to the DQ0-DQ15 lines. The default source of the data is the Comparand register. The other sources of the data that can be selected by executing a Persistent Source Select instruction are Mask Register 1, Mask Register 2, or the Memory array. The Comparand register, the two Mask registers and the Memory are read via the Multiplexer over one, two, three, or four cycles, depending on the start-count and end-count values set for the Source Segment counter.

On the 64-bit bus, instructions allow moving data among the Comparand register, Mask Register 1, Mask Register 2, and the Memory array. The data transfers between the Comparand register and the Memory array can be masked by the contents of either Mask register as can the Memory Write operation.

The Memory array comprises a 1K x 64-bit CAM array and a 1K x two-bit Validity bit array. The Memory array is configurable as a CAM field and a RAM field on 16-bit boundaries. During a Compare cycle, the value held in the Comparand register corresponding to the unmasked bits of the CAM field is compared simultaneously with all valid locations in the CAM field.

The bits of the selected Mask register control which corresponding bits of the Comparand are used in the comparison with the contents of the CAM field. If a bit is set HIGH in the Mask register, the corresponding bit in the CAM field is forced to a true comparison at all locations, regardless of the value of that bit in the Comparand. During a compare, the RAM field of the Memory array is automatically excluded from the comparison.

Each memory location has a two-bit field that indicates the validity of the location. The two validity bits are designated the Empty bit and the Skip bit and are encoded to give four validity conditions shown in Table 2-1. The unmasked portion of locations with their Validity bits set to Valid will enter into a comparison with the Comparand during Compare cycles, and can be accessed randomly (Read and Write at Address). Locations set Empty will not enter into a comparison; they are eligible to be randomly accessed, and can be overwritten by Write-at-Next-Free-Address cycles. Locations set to Skip will not enter into a comparison; they are eligible to be randomly accessed for Read or Write cycles, but are considered to contain valid data, and will not be overwritten by Write-at- next-free-address cycles. The Skip state is used to process multiple responders. Locations set to Random Access will not enter into a comparison; these locations can be accessed by random access cycles or associative cycles that search the validity bit field for the Random-access status indication. They are considered to contain valid data and will not be overwritten by Write-at-next-free-address cycles. The Random Access condition defines locations that contain data only, such as a buffer area for storing mask values and other nonassociative information. Such information is protected and will not be modified along with associative data. The Skip and Empty bits can be manipulated by instructions both as a function of address and content.

Skip	Empty	Condition
LOW	LOW	Valid Location
LOW	HIGH	Empty Location
HIGH	LOW	Temporarily Withdrawn from Comparison (Skip)
HIGH	HIGH	Random Access Only

Table 2-1 - Validity Bit Encoding

Each of the 1,024 64-bit content fields in the Memory array has a Match line connected to the Priority encoder. All the cells of a content are wire-ANDed onto the Match line. If any one or more of the non-masked CAM cells of a valid content differ from the corresponding bit of the Comparand (a mismatch), that or those cells pull the Match line of that content LOW.

The Priority encoder generates the address of the highest-priority content whose Match line remains HIGH during a Comparison cycle. The prioritization scheme is hard-wired such that the address 000H is the highest priority, and the address 3FFH is the lowest. The Match address generated by the Priority encoder is fed to the Status register, where it can be read out on the DQ0-DQ15 bus during a Command Read cycle.

The Match lines are also fed to the Match and Flag logic block which generates the Match flag signal (/MF), and the internal Match flag (/MA) and Multiple match flag (/MM), which are sent to the Status register. The Match flag is affected by the Match Input signal, /MI, in vertically cascaded systems, and is further affected by the /EC input. The internal /MA and /MM flags are NOT affected by the flag enable bits in the Control register or the /MI or /EC inputs.

The Empty bits in the array are connected to the Priority encoder to generate the next free address for Associative write cycles. The Empty bits are also connected to the Match and Flag logic block which generates the Full Flag signal (/FF) and the internal Full flag (/FL) in the Status register. The Full flag is affected by the Full Input signal, /FI, in vertically cascaded systems. The internal /FL flag is NOT affected by the /FI input or the flag enable bits in the Control register.

The output flags, /MF and /FF, can be enabled and disabled independently by loading certain values into the Control register. Since the internal flags, /MA, /MM, and /FL, are not controlled by external conditions, local conditions within a single P1480 in a multi-device system can be determined from the Status register.

CHAPTER 3
OPERATIONAL CHARACTERISTICS

3.1 THE CONTROL BUS

Throughout the following text aaaH represents a general three-bit hexadecimal number aaa where each letter corresponds to a four-bit binary field. Similarly, bbB represents a two-bit binary field bb.

Refer to the Block Diagram (Fig. 2-2) for the following discussion. The primary control mechanism of the PNC1480 is the Control bus which comprises the Chip Enable (/E), the Write Enable (/W), and the Command Enable (/CM) inputs. The Enable Comparison (/EC) input of the Control bus is responsible for enabling the Match flag output when LOW, but does not influence comparisonsoor the flow of data into or out of the device. The secondary control mechanism of the P1480 is via the instructions which are loaded into the Instruction register. Logical combinations of the Control Bus inputs, coupled with the execution of Select Persistent Source (SPS), Select Persistent Destination (SPD), and Temporary Command Override (TCO) instructions, allow the I/O operations to and from the DQ0-DQ15 lines shown in Table 3-1.

The default source and destination for Data Read and Write cycles is the Comparand register. This default state can be overridden independently by executing a Select Persistent Source or Select Persistent Destination instruction. If a particular source or destination is selected, subsequent Data Read or Write cycles will access that source or destination until another such instruction is executed. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand register, Mask Register 1, Mask Register 2, and the Memory array.

Access to the Control register, the Page Address register, the Segment Control register, the Address register, and Device Select Register is by Temporary Command Override (TCO) instructions which are only active for one Command Read or Write cycle after being loaded into the Instruction register. In other words, the override instructions are not persistent. The currently selected persistent source or destination can be read back via a TCO PS (or PD) instruction. Each control state has alternative functions, dependent on the selected temporary and permanent operating conditions.

The data and control interfaces to the P1480 are synchronous. During a Write cycle, the Control and Data inputs are registered by the falling edge of /E. When writing to the persistently selected data destination, the Destination Segment counter is clocked by the rising edge of /E. During a Read cycle, the Control inputs are registered by the falling edge of /E, and the Data outputs are enabled while /E is LOW. When reading from the persistently selected data source, the Source Segment counter is clocked by the rising edge of /E.

3.2 THE REGISTER SET

Instruction and Address Registers

The nature of ensuing operations within the device is selected by loading the Instruction register. Only one Command Write cycle is required if the instruction does not define a specific address. A second Command Write cycle, during which the Address is presented on the DQ0-DQ15 lines and is loaded into the Address register, is required if the instruction does require a specific address, as indicated by the Address Field flag in the instruction. If the instruction normally requires an address, but the Address Field flag is not set, then the instruction executes at the address currently pointed to by the contents of the Address register.

The lower-order twelve bits of the Instruction register comprise the instruction. Details of the bit allocations within this subfield are given in Section 4.2. The upper-order four bits of the Instruction register hold the upper-order four bits of the address for a random access instruction. The sixteen bits of the Address register hold the lower-order sixteen bits of the address. In the P1480 only the lower-order ten bits of this twenty-bit address field are used. The additional address space allows for future expansion.

Writing to the Instruction register can be suspend for one Command Write cycle by loading a Temporary Command Override (TCO) instruction into the Instruction register. The next cycle must be a Command Write cycle and will load the Control register, the Page Address register, the Segment Control register, the Device Select register, or the Address register, depending on the destination selected by the TCO instruction. After loading the register selected by the TCO instruction, subsequent Command Write cycles are again directed to the Instruction register until another TCO instruction is executed. Details of the Instruction set are given in Chapter 4. The bit assignments for the Instruction word and the Address are shown in Table 3-2.

Status Register

The internal status of the P1480 is read from the Status register, which is the default register for Command Read cycles. In the first Command Read cycle, bits 0-15 of the Status register are available on DQ0-DQ15. If the next cycle is also a Command Read, bits 16-31 of this register are available on DQ0-DQ15. If the next cycle is not a Command Read, on a subsequent such cycle bits 0-15 of this register will again be accessed.

Status register bits ST0-ST15 contain the Match flag / MA, the 10-bit Match address from the Priority encoder, AM0-AM9, and the lower-order five bits of the Page Address register, PA0-PA4. Bits ST16-ST31 contain the remaining eleven bits of the Page Address register, PA5-PA15, the Full flag, /FL, and the Multiple Match flag, /MM.

/E	/CM	/W	I/O Status	SPS	SPD	TCO	Operation	Notes
L	L	L	IN				Load Instruction register	1
			IN			√	Load Address register	2,3
			IN			√	Load Control register	3
			IN			√	Load Page Address register	3
			IN			√	Load Segment Control register	3
			IN			√	Load Device Select register	3
L	L	H	OUT			√	Read Next Free Address register	3
			OUT			√	Read Instruction Address register	3
			OUT				Read Status Register bits 0-15	4
			OUT				Read Status Register bits 16-31	5
			OUT			√	Read Control Register	3
			OUT			√	Read Page Address Register	3
			OUT			√	Read Segment Control Register	3
			OUT			√	Read Device Select Register	3
			OUT			√	Read Current Persistent Source or Destination	3,11
L	H	L	IN		√		Load Comparand Register	6,9
			IN		√		Load Mask Register 1	7,9
			IN		√		Load Mask Register 2	7,9
			IN		√		Write Memory Array at Address	7,9
			IN		√		Write Memory Array at Next Free Address	7,9
			IN		√		Write Memory Array at Highest-priority Match	7,9
L	H	H	OUT	√			Read Comparand Register	6,9
			OUT	√			Read Mask Register 1	8,9
			OUT	√			Read Mask Register 2	8,9
			OUT	√			Read Memory Array at Address	8,9
			OUT	√			Read Memory Array at Highest-priority Match	8,9
H	X	X	HIGH-Z				Deselected	
L	L	L	IN			√	Deselected	10

Notes:

1. Default Command Write cycle destination.
2. Command Write cycle destination on the consecutive Command Write cycle if Address flag was set in bit IR11 of the instruction loaded in the previous cycle.
3. Loaded or read on the consecutive Command Write or Read cycle after a TCO instruction has been loaded. Active for one Command Write or Read cycle only. NFA register cannot be loaded this way.
4. Default Command Read cycle source.
5. Command Read cycle source on the consecutive Command Read cycle. If next cycle is not a Command Read cycle, it accesses the Status register low-order 16-bits.
6. Default persistent source and destination on power-up and after Reset. If other resources were selected as sources or destinations, SPD CR or SPS CR restores the Comparand register as the destination or source.
7. Selected by executing a Select Persistent Destination.
8. Selected by executing a Select Persistent Source Instruction.
9. May require multiple 16-bit Read or Write cycles. Segment Control register used to control selection of desired 16-bit segment(s) by establishing Segment counters' limits and start values.
10. Device is also deselected if contents of Device Select register do not match contents of Page Address register except when Device Select register contains all 1's (0FFFFH). All Device Select registers in a vertically cascaded device array are written in a Command Write cycle immediately following a TCO with the Device Select register as the destination.
11. TCO PS or TCO PD read back the Instruction register bits that were last set to select a source or destination on the next cycle which must be a Command Read cycle.

Table 3-1 - Input/Output Operations

IR15	IR14	IR13	IR12	IR11	IR10	IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
\AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

BIT	FUNCTION
IR15-1R12	Address bits, A19-A16
IR11-IR0	Instruction bits, I11-!0
AR15-AR0	Address bits, A15-A0

Table 3-2 - Instruction Register and Instruction Address Register Bit Assignments

Access to the Status register can be overridden for one Command Read cycle by loading a TCO instruction into the Instruction register. The next cycle must be a Command Read cycle and will access the Control register, the Page Address register, the Segment Control register, the Device Select register, the Next Free Address register, or the Address register, depending on the source selected by the TCO instruction. After reading the register selected by the TCO instruction, subsequent Command Read cycles again access the Status register until another TCO instruction is executed. Table 3-3 lists the bit assignments for the Status register.

The Control Register

The Control register can be written to or read from by executing a TCO instruction, specifying in the instruction the Control register as the destination or source for the next Command Write or Read cycle, respectively. The next cycle must be a Command Write or Read cycle. Subsequent Command cycles again access the Instruction register (Write) or the Status register (Read) until another TCO instruction is executed.

The most-significant bit of the Control register, CT15, controls the software resetting of the device. If CT15 is LOW, the device is reset, and all lower-order bits, CT14-CT0, are ignored. The reset operation sets all locations to the Empty condition (Skip is LOW, Empty is HIGH); the Match and Full flag outputs are enabled; the input is not translated according to the mapping between IEEE 802.3 and IEEE 802.5; the CAM/RAM partitioning is set to 64 bits CAM, 0 bits RAM; the Comparison masking is disabled; the Address autoincrement/autodecrement mode is disabled; the default sources and destinations are restored (Status register and Instruction register for Command Reads and Writes and Comparand register for Data Reads and Writes); the Source and Destination Segment counters are set to count from 00 to 11, and are loaded with 00 (this state is reflected by the value forced into the Segment Control register); the Address register is loaded with all zeros; the Page Address and Device Select registers are left unchanged; and the value 0008H is loaded into the Control register. The Page Address and Device Select registers contain all 0's after a power-on reset. See Table 3-4 for the device control state after a Reset Command.

If a value is loaded into the Control register with CT15 set HIGH, then no reset occurs and the lower order 15 bits persistently determine the settings of the device. All the control fields have an enable state, so each can be independently set , although the Reset function overrides all the other control bits. The bit assignments for the Control register are shown in Table 3-5.

ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16

BIT	FUNCTION
ST31	Full flag, /FL
ST30	Multiple Match flag, /MM
ST29-ST27	Reserved (LOW)
ST26-ST16	Concatenated Page Address bits, PA15-PA5
ST15-ST11	Concatenated Page Address bits, PA4-PA0
ST10-ST1	Match address from Priority Encoder, AM9-AM0
ST0	Match flag, /MA

Table 3-3 - Status Register Bit Assignments

Page Address Register

The Page Address register can be written to or read from by executing a TCO instruction, specifying in the instruction the Page Address register to be the destination or source for the next Command Write or Read cycle. The next cycle must be a Command Write or Read cycle. Subsequent Command Write or Read cycles access the Instruction register or the Status register, respectively, until another TCO instruction is executed.

In a vertically cascaded system, access to individual Page Address registers is controlled through the Full-flag daisy chain. The loading of each Page Address register is always local, never global. Each device is selected in turn to have its Page address written and is then forced full in turn using the Set Full Flag instruction.

The value written into the Page Address register is appended to the Match Address which results from a Compare cycle, and can be read in the combined form from the Status register. The Page Address register bit assignments are shown in Table 3-6.

Device Select Register

The Device Select register can be written to or read from by executing a TCO instruction, specifying in the instruction the Device Select register to be the destination or source for the next Command Write or Read cycle. The next cycle must be a Command Write or Read cycle. Subsequent Command Write or Read cycles access the Instruction register or the Status register, respectively, until another TCO instruction is executed.

In a vertically cascaded system, the Device Select register allows a particular device to be selected for access without the need for any external decoding. A value is broadcast to all Device Select registers via a TCO DS instruction, and only the device whose Page Address value matches the Device Select value will respond to further transactions. Device selection is overridden when the value FFFFH is written into the Device Select registers of all devices in the array. The loading of the Device Select registers is always global, never local. The Device Select register bit assignments are shown in Table 3-7.

Segment Control Register

The Segment Control register can be written to or read from by executing a TCO instruction, specifying in the instruction the Segment Control register to be the destination or source for the next Command Write or Read cycle. The next cycle must be a Command Write or Read cycle. Subsequent Command Write or Read cycles access the Instruction register or the Status register, respectively, until another TCO instruction is executed.

The Segment Control register bits SC14-SC11 set the Destination Segment counter limits. SC15 enables the loading of these bits. SC9-SC6 set the Source Segment counter limits. SC10 enables the loading of these bits. SC4 and SC3 are loaded into the Destination Segment counter. SC5 enables the loading of these bits. SC1 and SC0 are loaded into the Source Segment counter. SC2 enables the loading of these bits. When the Segment Control register is read, SC4 and SC3 contain the current value of the Destination Segment counter, and SC1 and SC0 contain the current value of the Source Segment counter. All the control fields have an enable bit so that each can be set independently.

If the Source or Destination Segment counter load values are outside the count limits, the value is loaded into the counter which then increments, once per Read or Write cycle on the rising edge of /E, until the End Count value is reached. On the next clock cycle, the counter returns to the Start Count value. On subsequent cycles the count is from Start Count to End Count. The bit assignments for the Segment Control register are shown in Table 3-8.

Control Register Resource	After Reset, Set to
Validity bits at all memory location	Skip = 0, Empty = 1
Match and Full Flag outputs	Enabled
IEEE 802.3-802.5 Input Translation	Not translated
CAM/RAM Partitioning	64 bits CAM, 0 bits RAM
Comparison masking	Disabled
Address register autoincrement and autodecrement	Disabled
Source and Destination Segment counters count ranges	00B to 11B; loaded with 00B
Address register	Contains all 0's
Page Address and Device Select registers	Unchanged
Control register after Reset (including CT15)	Contains 0008H
Persistent Destination for Command Writes	Instruction register
Persistent Source for Command Reads	Status register (bits 0-15)
Persistent Source and Destination for Data Reads and Writes	Comparand register

Table 3-4 - Device Control State after Reset Command

CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CONTROL REGISTER BIT			FUNCTION
CT15			
0			Reset
1			Do Not Reset
CT14	**CT13**		
0	0		Enable Match flag
0	1		Disable Match flag
1	0		Reserved
1	1		No Change to Match Flag State
CT12	**CT11**		
0	0		Enable Full flag
0	1		Disable Full flag
1	0		Reserved
1	1		No Change to Full flag State
CT10	**CT9**		
0	0		Input Not Scrambled
0	1		Input Scrambled
1	0		Reserved
1	1		No Change to Scramble State
CT8	**CT7**	**CT6**	
0	0	0	64 CAM bits, 0 RAM bits
0	0	1	48 CAM bits, 16 RAM bits
0	1	0	32 CAM bits, 32 RAM bits
0	1	1	16 CAM bits, 48 RAM bits
1	0	0	0 CAM bits, 64 RAM bits
1	0	1	Reserved
1	1	0	Reserved
1	1	1	No Change to partitioning
CT5	**CT4**		
0	0		Disable Comparison Masking
0	1		Mask Comparison with Mask Register 1
1	0		Mask Comparison with Mask Register 2
1	1		No Change to Masking Condition
CT3	**CT2**		
0	0		Enable Address Increment
0	1		Enable Address Decrement
1	0		Diasable Address Increment/Decrement
1	1		No Change to Address Increment/Decrement
CT1	**CT0**		
X	X		Reserved

Table 3-5 - Control Register Bit Assignments

PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

BIT	FUNCTION
PA15-PA0	Page Address

Table 3-6 - Page Address Register Bit Assignments

DS15	DS14	DS13	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0

BIT	FUNCTION
DS15-DS0	Device Select Value

Table 3-7 - Device Select Register Bit Assignments

Comparand Register

The default source and destination for Data Read and Write cycles is the Comparand register. During a Data Write cycle, the Comparand register is loaded in one, two, three, or four cycles, depending on the start-count and end-count values of the Destination Segment counter. Each falling edge of /E registers a 16-bit segment of data from DQ0-DQ15 into the Comparand register. Each rising edge of /E increments the Destination Segment counter. During a Data Read cycle, the Comparand register is accessed in one, two, three, or four cycles, depending on the start-count and end-count values of the Source Segment counter. Each falling edge of /E enables the DQ0-DQ15 outputs while each rising edge of /E increments the Source Segment Counter and turns off the DQ0-DQ15 outputs.

Default read or write access to the Comparand register can be overridden by executing a Select Persistent Source (SPS) or Select Persistent Destination (SPD) instruction. The persistent source and destination of data during a Data Read or Data Write cycle can be selected independently. The sources and destinations that can be selected on a persistent basis for data during a Data Read or Write cycle are either of the Mask registers and the Memory array with various combinations of status conditioning or addressing. The bit assignments for the Comparand register are shown in Table 3-9.

Mask Register 1 and Mask Register 2

Mask Register 1 and/or 2 can be chosen as the persistent source and/or destination for Data Read or Write cycles by executing a SPS Mask Register 1 (or 2) or SPD Mask Register 1 (or 2) instruction. Once chosen, the Mask register remains the source or destination for subsequent Data Read or Write cycles until another source or destination is chosen via an SPS or SPD instruction, or a Reset occurs.

Mask Register 1 or 2 is selected to mask Compare cycles through bits CT5 and CT4 in the Control register. Masking of Data Write and Data Move operations is controlled by instruction. In a Compare operation, if a Mask register has been enabled, bits set LOW in the Mask register cause corresponding bits throughout the Memory array to be compared with Comparand bits. Bits set HIGH in the Mask register force a match between corresponding bits in the Memory array and Comparand bits. During masked Data Write and Move cycles, destination bits corresponding to LOW values in the selected Mask register are updated, while bits corresponding to HIGH values in the selected Mask register remain unchanged. The bit assignments for Mask Registers 1 and 2 are shown in Table 3-10.

3.3 THE MEMORY ARRAY

The Memory array is organized as 1024 64-bit locations, each having two Validity bits, the Skip bit and Empty bit. By default each location comprises 64 CAM cells. However, the array can be reconfigured by writing to the Control register, to divide each location into a CAM field and a RAM field. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selections of 64 CAM bits, 0 RAM bits; 48 CAM bits, 16 RAM bits; 32 CAM bits, 32 RAM bits; 16 CAM bits, 48 RAM bits; 0 CAM bits, 64 RAM bits. Memory Array bits designated to be RAM bits can be used to store and retrieve Associated data (data associated with a CAM content). The bit assignments for the Memory array are shown in Table 3-11.

Read Memory at Address

The Memory array can be selected as the persistent source for Data Read cycles as a function of a specified address by executing a Select Persistent Source Memory Array at Address instruction. Once selected in this way, the Memory array remains the source for subsequent Data Read cycles until another source is selected by executing another Select Persistent Source instruction.

SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

SEGMENT CONTROL REGISTER BIT				FUNCTION
SC15				
0				Set Destination Segment Counter Limits
1				No Change to Destination Segment Counter Limits
SC14	**SC13**	**SC12**	**SC11**	
0	0	0	0	Destination Count Start 00, End 00
0	0	0	1	Destination Count Start 00, End 01
0	0	1	0	Destination Count Start 00, End 10
0	0	1	1	Destination Count Start 00, End 11
0	1	0	0	Reserved
0	1	0	1	Destination Count Start 01, End 01
0	1	1	0	Destination Count Start 01, End 10
0	1	1	1	Destination Count Start 01, End 11
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Destination Count Start 10, End 10
1	0	1	1	Destination Count Start 10, End 11
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Destination Count Start 11, End 11
SC10				
0				Set Source Segment Counter Limits
1				No Change to Source Segment Counter Limits
SC9	**SC8**	**SC7**	**SC6**	
0	0	0	0	Source Count Start 00, End 00
0	0	0	1	Source Count Start 00, End 01
0	0	1	0	Source Count Start 00, End 10
0	0	1	1	Source Count Start 00, End 11
0	1	0	0	Reserved
0	1	0	1	Source Count Start 01, End 01
0	1	1	0	Source Count Start 01, End 10
0	1	1	1	Source Count Start 01, End 11
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Source Count Start 10, End 10
1	0	1	1	Source Count Start 10, End 11
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Source Count Start 11, End 11
SC5				
0				Load Destination Segment Counter
1				No Change to Destination Segment Counter

Table 3-8 - Segment Control Register Bit Assignments (Continued opposite)

SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

SEGMENT CONTROL REGISTER BIT		FUNCTION
SC4	**SC3**	
0	0	Load Destination Segment Counter with 00
0	1	Load Destination Segment Counter with 01
1	0	Load Destination Segment Counter with 10
1	1	Load Destination Segment Counter with 11
SC2		
0		Load Source Segment Counter
1		No Change to Source Segment Counter
SC1	**SC0**	
0	0	Load Source Segment Counter with 00
0	1	Load Source Segment Counter with 01
1	0	Load Source Segment Counter with 10
1	1	Load Source Segment Counter with 11

Table 3-8 - Segment Control Register Bit Assignments (Continued)

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
CR47	CR46	CR45	CR44	CR43	CR42	CR41	CR40	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
CR63	CR62	CR61	CR60	CR59	CR58	CR57	CR56	CR55	CR54	CR53	CR52	CR51	CR50	CR49	CR48

BIT	FUNCTION
CR15-CR0	Comparand Register Segment 1
CR31-CR16	Comparand Register Segment 2
CR47-CR32	Comparand Register Segment 3
CR63-CR48	Comparand Register Segment 4

Table 3-9 - Comparand Register Bit Assignments

If the Address flag is set in the instruction, the address at which the Memory is to be accessed is loaded by a second Command Write cycle after the Select Persistent Source Memory Array at Address instruction. If the Address flag is not set, the memory access occurs at the address currently contained in the Address register.

Subsequent addresses can be generated in one of two ways. A new address can be forced into the Address register by executing a TCO instruction to direct the next Command Write cycle to the Address register. Alternatively, by the appropriate setting of the Control register bits CT3 and CT2, the Address register will increment or decrement automatically when the Source or Destination Segment counter reaches its end count. Automatic incrementing or decrementing provides support for DMA transfers to and from the memory. Note that the incrementing or decrementing involves Memory-at-Address functions and does not occur for operations with the other sources or destinations, regardless of the setting of CT3 and CT2.

MXI5	MX14	MX13	MX12	MX11	MX10	MX9	MX8	MX7	MX6	MX5	MX4	MX3	MX2	MX1	MX0
MX31	MX30	MX29	MX28	MX27	MX26	MX25	MX24	MX23	MX22	MX21	MX20	MXI9	MX18	MX17	MX16
MX47	MX46	MX45	MX44	MX43	MX42	MX41	MX40	MX39	MX38	MX37	MX36	MX35	MX34	MX33	MX32
MX63	MX62	MX61	MX60	MX59	MX58	MX57	MX56	MX55	MX54	MX53	MX52	MX51	MX50	MX49	MX48

BIT	FUNCTION
MXI5-MX0	Mask Register 1 or 2 Segment 1
MX31-MX16	Mask Register 1 or 2 Segment 2
MX47-MX32	Mask Register 1 or 2 Segment 3
MX63-MX48	Mask Register 1 or 2 Segment 4

Table 3-10 - Mask Register 1 and 2 Bit Assignments

Read Memory at Highest-priority Match Address

The Memory array can be selected as the persistent source for Data Read cycles as a function of the highest-priority match address by executing a Select Persistent Source Memory Array at Highest-priority Match Address. Once selected to be accessed at the highest-priority match address, the Memory array remains the source for subsequent Data Read cycles until another source is selected by executing another Select Persistent Source instruction.

No explicit address field is required to access the memory during these Associative Read cycles. Instead, the memory is addressed as a function of the highest-priority location whose contents match with the contents of the Comparand register taking the selected Mask register, if any, into account. The comparison may or may not be masked by the contents of Mask Register 1 or Mask Register 2, depending on what comparison conditions have been selected by earlier instructions written to the device.

If no match exists between the contents of the Comparand register and the contents of the CAM section of the memory array, the DQ0-DQ15 bus remains in the high-impedance state to facilitate the daisy chain operation. If enabled, /MF will indicate whether or not a match has occurred. In a daisy-chained system, only the highest-priority responding device, if any, will be accessed by the Data Read cycle. For this reason, the /MF line can be enabled and checked by the system to determine the no-match condition in vertically cascaded systems. If the daisy-chain feature is not used, individual devices can still be accessed if the contents of their Page Address register matches those of their Device Select register.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
D47	D46	D45	D44	D43	D42	D41	D40	D39	D38	D37	D36	D35	D34	D33	D32
D63	D62	D61	D60	D59	D58	D57	D56	D55	D54	D53	D52	D51	D50	D49	D48

BIT	FUNCTION
D15-D0	Memory Array Segment 1
D31-D16	Memory Array Segment 2
D47-D32	Memory Array Segment 3
D63-D48	Memory Array Segment 4

Table 3-11 - Memory Array Bit Assignments

If a context-specific operation is desired where a particular device's Status register is to be queried, the DQ0-DQ15 lines of that device will be enabled for one or more Command Read cycles if its Device Select register's contents match its Page Address register's contents. In this case, the selected device's /MA, /MM, and other Status register bits can be used to reflect a match or no-match condition.

Write Memory at Address

The Memory array can be selected as the persistent destination for Data Write cycles as a function of a specified address by executing a Select Persistent Destination Memory Array at Address instruction. Once selected to be written at a specified address, the Memory array remains the destination of subsequent Data Write cycles until another destination is selected by executing another Select Persistent Destination instruction.

If the Address flag is set in the instruction, the address at which the Memory is to be accessed is loaded as the secondwword in a Command Write cycle after the instruction to Select Persistent Source Memory Array at Address. If the Address flag is not set, the memory write occurs at the address currently contained in the Address register.

Subsequent addresses can be generated in one of two ways. A new address can be forced into the Address register by executing a Temporary Command Override instruction to direct the next Command Write cycle to the Address register. Alternatively, by the appropriate setting of the Control register bits CT3 and CT2, the Address can be set to increment or decrement automatically when the Source or Destination Segment counter reaches its end count. This feature provides support for DMA transfers to and from the memory. Note that the incrementing or decrementing only occurs for Data Read and Write Memory-at-address cycles; incrementing or decrementing does not occur when the other persistent sources or destinations are selected, regardless of the setting of CT3 and CT2.

The Write to the Memory array may be masked by either Mask Register 1 or Mask Register 2, depending on the conditions set up by the Select Persistent Destination (SPD) instruction. During the cycle in which the last 16-bit segment of the current data word is written into the Memory array, the validity of the addressed location will be set according to the condition specified by the SPD instruction most recently executed.

Write Memory at Highest-priority Match Address

The Memory array can be selected as the persistent destination for Data Write cycles as a function of the highest-priority match address by executing a Select Persistent Destination Memory Array at Highest-priority Match Address instruction. Once selected, the Memory array at the highest-priority match address remains the destination for subsequent Data Write cycles until another destination is selected by executing a different Select Persistent Destination instruction.

No explicit address field is required to write the memory during these Associative Write cycles. Instead, the memory is addressed as a function of the highest-priority locationwwhose contents match with the contents of the Comparand register taking the selected Mask register, if any, into account. The comparison could be masked by the contents of Mask Register 1 or 2, depending on what comparison conditions have been selected by previous instructions.

The Write to Memory Array operations may be masked by either Mask Register 1 or Mask Register 2, depending on the conditions set up by the Select Persistent Destination instruction. During the cycle in which the last 16-bit segment of the current data word is written into the Memory array, the validity of the addressed location will be set according to the condition specified by the Select Persistent Destination instruction most recently executed.

Write Memory at Next Free Address

The Memory array can be selected as the persistent destination for Data Write cycles as a function of the next free address by executing a Select Persistent Destination (SPD) Memory at Next Free Address instruction. Once selected to be written at the next free address, the Memory array remains the destination for subsequent Data Write cycles until another destination is selected by executing another SPD instruction.

No explicit address field is required to write the memory during these Associative Write cycles. Instead, the memory is addressed as a function of the next free location. The LAN CAM generates this address automatically by internally feeding the Validity bits to the Priority encoder. The next free address is contained in the Next Free Address register which can be read (but not written) using the TCO instruction.

The Write at Next Free Address cycle can be used in a vertically cascaded system when the Full flags are daisy-chained. When a Write at Next Free Address cycle is broadcast, only the device which is not full and whose /FI input is LOW will respond to the Write cycle.

The Write to the Memory array may be masked by either Mask Register 1 or 2, depending on the conditions set up when loading the Select Persistent Destination instruction. During the cycle in which the last segment of the current data word is written into the Memory array, the validity bits of the addressed location are set according to the condition specified by the Select Persistent Destination instruction most recently executed. Data Move instructions from the Comparand register and the two Mask registers to the Memory array either set the location Valid, or leave the Validity bits unchanged, depending on the instruction.

3.4 I/O CYCLES

The P1480 supports four basic I/O cycles: Data Read, Data Write, Command Read, and Command Write. The nature of a particular cycle is determined by the states of the /W and /CM control inputs. These signals are registered at the beginning of a cycle by the falling edge of /E. Table 3-12, a summary of Table 3-1, shows how the /W and /CM lines select the cycle type.

/W	/CM	Cycle Type
LOW	LOW	Command Write Cycle
LOW	HIGH	Data Write Cycle
HIGH	LOW	Command Read Cycle
HIGH	HIGH	Data Read Cycle

Table 3-12 - Summary of I/O Cycles

During Read cycle, the outputs are enabled when /E is LOW. During Write cycles, the data or command to be written is captured at the beginning of the cycle by the falling edge of /E. Figs. 3-1 and 3-2 show Read and Write cycles respectively. Fig. 3-3 shows the cycle-to-cycle timing of three Comparand loads followed by a Status register or Memory array Read.

Because the P1480 does not have a conventional address bus, the device should be memory mapped in a system, which sees the device as four locations: reading and writing command and data resources. The four locations correspond to the logical combinations of the /CM and the /W control inputs. The /EC control input enables the comparison flag, /MF, provided CT13 and CT14 are appropriately set, and activates the daisy chain in a vertically cascaded system.

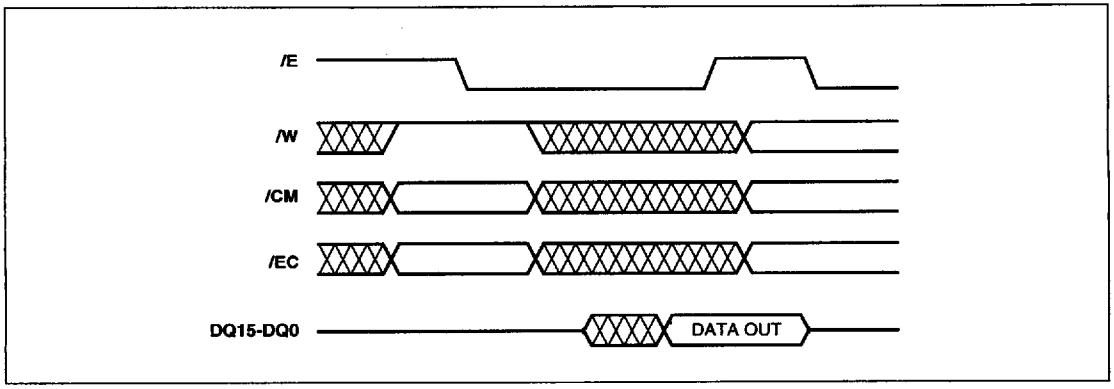


Fig. 3-1 - Read Cycle

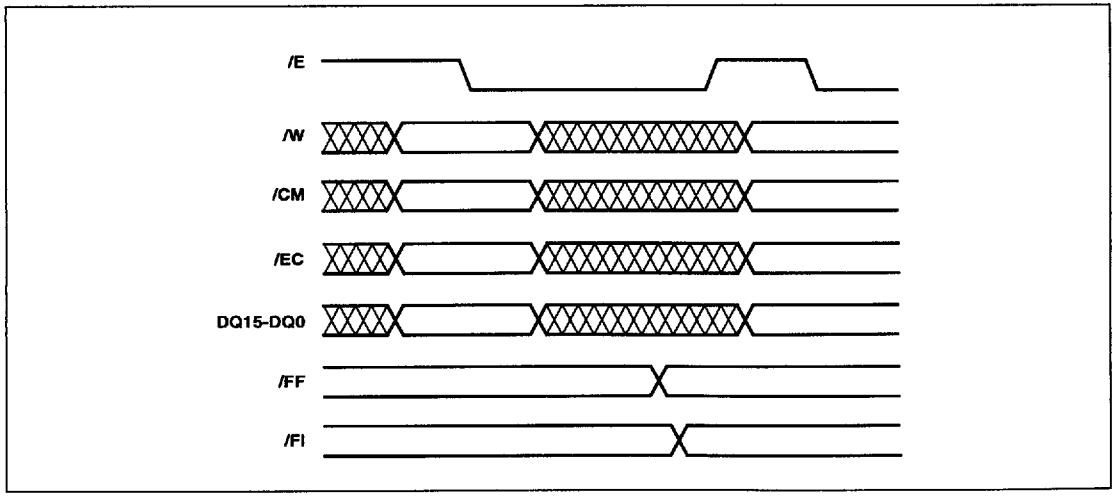


Fig. 3-2 - Write Cycle

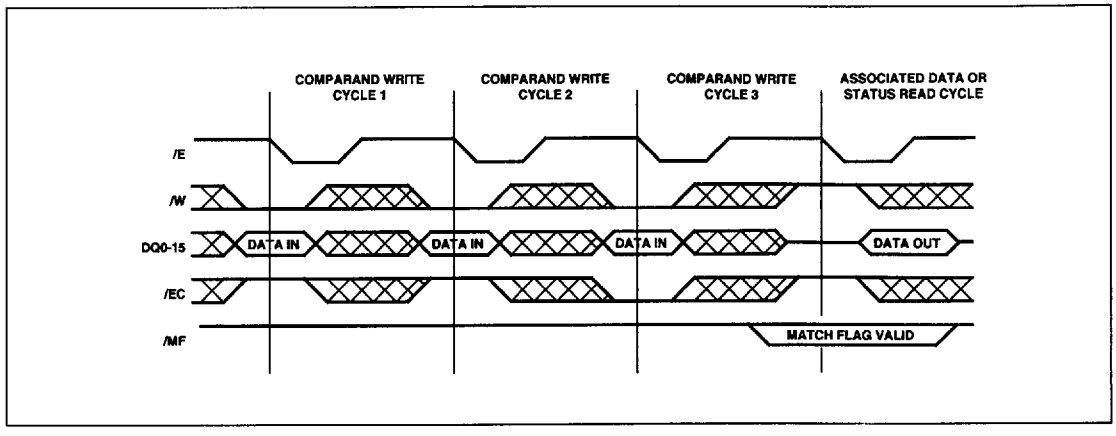


Fig. 3-3 - Cycle to Cycle Timing

3.5 VERTICAL CASCADING

The P1480 can be vertically cascaded in a system to increase its depth. The vertical cascading uses a daisy-chaining technique which allows system prioritizing of the Match response and control of the Memory-full status. The 5 ns (worst case) serial delay per device in the daisy-chained vertical cascading can easily be handled in the system. Should this delay be too long, the daisy chaining need not be used, and system match ordering can be done with external logic.

Daisy-chaining is achieved through the /FI and /FF flags for the Full indication, and the /MI and /MF flags, controlled by the /EC input, for the Match indication. The two cascading processes can be used independently. In other words, the Full flag cascading can be used, and the Match flags can be prioritized externally, or both cascading schemes can be used together. A system in which four P1480s are vertically cascaded using daisy-chaining for both the Full and Match flags is shown in Fig. 3-4.

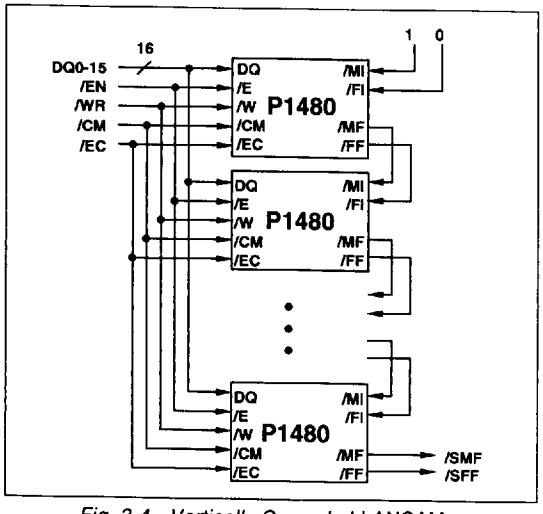


Fig. 3-4 - Vertically Cascaded LANCAMs

Full Flag Cascading

Referring to Fig. 3-4, the condition that the Full flag is set LOW in a particular device is that the /FI input is LOW, and that device is full. If the /FI input is HIGH, one (or more) location(s) are free above that device. Under this circumstance, whether or not that particular device is full, its /FF flag will remain HIGH. In this way, system-full indication takes into account free locations in devices higher up in the daisy chain.

The daisy chain also allows Write-at-Next- Free-Address cycles to operate globally over the entire system, and not just locally in a device. All devices in the system can be set to have Memory-at-Next-Free-Address selected as their persistent destination for Data Write cycles. Data Write cycles can then be broadcast to all devices. Only the device in which /FI input is LOW, and which is not full, will respond to the Write cycle. This scheme allows deletions and insertions to take place in the memory automatically, without the need to keep track of addresses.

The daisy chaining also gives a system-full indication. When the device at the end of the chain has its /FF LOW, the system must be full. The first device in the chain must have its /FI input tied LOW. The truth table for the Full flag cascading is shown in Table 3-13.

/FI	Device Full	/FF	Write @ Next Free Address
LOW	NO	HIGH	YES
LOW	YES	LOW	NO
HIGH	NO	HIGH	NO
HIGH	YES	LOW	NO

Table 3-13 - Full Flag Cascading Logic

Match Flag Cascading

Referring to Fig. 3-4, the Match flag will be LOW in a particular device if its /MI input is LOW, or there is a match in that device and the Match flag is enabled in the Control registers of all devices in the daisy chain. If the /MI input is LOW, there is one (or more) matching location(s) above that device. Under this circumstance, whether or not that particular device has a match, its /MF flag will be forced LOW. In this way, the system-match indication flags matching locations in devices higher up in the daisy chain.

The daisy chain also controls access to the highest-priority Status register, and allows Data Reads from and Writes to the highest-priority matching address to operate over the entire system, and not just in a device. When a Command Read cycle is broadcast to the CAM system, access is gained to the Status register of the device which has its /MI input HIGH and has a match. Similarly, all devices in the system can be set to have Memory at Highest-priority Match as their persistent source or destination for Data Read or Write cycles. Data Read or Write cycles can then be broadcast to all devices. Only the device in which the /MI input is HIGH and which has a match will respond to the Read or Write cycle. This scheme automatically prioritizes a system of vertically cascaded devices, the highest up in the chain has the highest priority.

The daisy chaining also gives a system-match indication. When the end device of the chain has its /MF LOW, the system has a match in one or more devices. The /MI input of the first device in the chain is tied HIGH. The truth table for the Match flag cascading is shown in Table 3-14.

/MI	Match?	/MF	Access Status Reg. ?
LOW	NO	HIGH	NO
LOW	YES	LOW	NO
HIGH	NO	HIGH	NO
HIGH	YES	LOW	YES

Table 3-14 - Match Flag Cascading Logic

Clearly, indication of the match condition within the system takes some time to establish itself once a Comparand is loaded. The Compare time in each device operating in parallell is added to the ripple delay through the daisy chain. Before reading the results of a comparison, either through the Status register or the System Match flag, the daisy chain must be given time to settle to a valid state. If there are N devices vertically cascaded in a system, and the time to get a valid output on /MF is t(MF), and the time for the flag to ripple through one device from /MI valid to /MF valid is t(MI-to-MF), then the time t(DC) for the daisy chain to develop a valid output condition is

$$t(DC) = t(MF) + (N-1) * t(MI\text{-}to\text{-}MF).$$

This period of time must elapse before the results of the comparison are available.

To assist in accessing the results of a daisy-chained comparison, and overriding the control the daisy chain exerts on the system, the /EC control input enables and disables the /MF outputs in a special way. When /EC is HIGH at the falling edge of /E at the beginning of any cycle, the /MF output is forced HIGH, regardless of the match conditions in the device. When /EC is LOW at the beginning of a cycle, it enables the /MF output to respond to the /MI input, the /MF enable/disable control, and the match conditions in the device. The captured state of the /EC input remains in effect after the end of the cycle until it changes to another state at the beginning of a subsequent cycle. The /EC timing ensures that there are no false transitions on the /MF line prior to establishing local match conditions.

/EC allows the comparison and daisy-chain rippling to take place between device cycles. If, for example, a 48-bit Comparand is broadcast to all the P1480s in a daisy-chained system, the /EC line is driven HIGH during the writing of the first two segments. During the writing of the third segment, the /EC line is driven LOW. The comparison is active throughout all of the Comparand Write cycles, but the flags are only enabled at the end of the last load. Now the Associated data or Status register can be read as a function of the highest-priority match within the system, as long as sufficient time is allowed for the daisy-chain ripple to complete. The /EC line is captured internally on each CAM device, enabling the daisy chain to remain locked while the devices are not being accessed.

Vertically Cascaded System Initialization

In a vertically cascaded system, the user can set the contents of individual Page Address registers for subsequent local access by using the Page Address initialization mechanism. This process obviates the need for external decoding.

The Page Address register initialization works through the Full Flag cascading feature. The /FF output of one device is connected to the /FI input of the next-lower-priority device in the daisy chain. The highest-priority device has its /FI input tied LOW. While a device's /FI input is LOW, and the device is not full (/FF is HIGH), it responds to Write-at-next-free-address cycles. Once full, the /FF flag goes LOW, pulling /FI of the next-lower priority device LOW, thereby allowing that device to respond to Write-at-next-free-address cycles.

The instruction Set Full Flag forces the /FF output LOW in the currently writing device. The Page Address register of the first device can be loaded, its /FF can then be forced LOW by this instruction, and the Page Address register of the next-lower-priority device can be loaded. This process continues until all of the Page Address registers have been loaded. Note that the writes to the Page Address register are never broadcast. They only take place in the device whose /FI input is LOW, and whose /FF output is HIGH. Once all Page Address registers are initialized, a Reset command is issued which forces all the /FF outputs HIGH. Note that the Reset command does not alter the contents of the Page Address register. (See Table 3-4.)

Random Access for Vertically Cascaded Systems

The Device Select register allows random access to a single device in the daisy chain once the Page Address registers have been initialized. Random access into a daisy-chained system works by sending a Device Select value to all the Device Select registers which corresponds to the Page Address of the target device using the Temporary Command Override instruction.

Access to all resources of a given device is conditioned by the Device Select register of that device. Only the device which has a match between its Page Address register and its Device Select register will respond to access cycles.

The effects of the Device Select register can be switched off by loading a special value, FFFFH. When this value is loaded into the Device Select register, the comparison with the contents of the Page Address register is inhibited. Write cycles to the registers and memory of devices within a daisy-chained system are then broadcast, and all devices receive the data, such as when an instruction is sent to the CAM array.

When access to a specific device is required, the page address of that device is broadcast to all the Device Select registers using a TCO DS, Command Write instruction sequence. Now only the device with a match between the contents of the Page Address and Device Select registers will respond to subsequent Command and Data Read and Write cycles, until the value FFFFH is broadcast to the Device Select registers of all the devices in the system. This ability to switch on and off the Device Select function allows local or global transactions within the system.

All random access and register reads are inhibited for Data and Command Read cycles when global access is enabled (by loading the Device Select registers with the value FFFFH) to prevent bus contention from multiple devices' presenting the requested data simultaneously. All associative reads are allowed because the internal priority encoders and the daisy chaining only allow access to a single device at a time.

The Page Address registers must be correctly loaded. If equal values are loaded into two or more Page Address registers, there is the potential for bus contention. This software situation is analogous to the hardware condition where more than one /E line is activated in a RAM system, and such an error should be removed in the design debugging stages. An application programmer should not have access to such low-level system functions as the loading of the Page Address registers. That task will be implemented in or controlled by the firmware.

The implications to the user of being able to select between local and global access are far-reaching. This facility makes possible run-time switching into a context-specific mode.

3.6 IEEE 802.3/802.5 FORMAT MAPPING

To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the P1480 provides a bit translation facility in the Control space. Formally expressed, the nth input bit, D(n), maps to the xth output bit, Q(x), through the following expression:

$$D(n) = Q(7-n) \quad \text{for} \quad 0 < n < 7, \text{ and}$$

$$D(n) = Q(23-n) \quad \text{for} \quad 8 < n < 15.$$

Loading the appropriate value into the Control register persistently selects the condition either to translate, or not, the data written onto the 64-bit internal bus. The default condition on power-up and after a Reset command is not to translate the incoming data. Fig. 3-5 shows the bit mapping between the two formats.

3.7 INITIALIZING THE LAN CAM

Since the P1480 is controlled by a combination of input signals and instructions, some initialization is required to configure the device. Every effort has been made to make the default states of the device on power up and after a Reset operation as useful as possible. However, since applications for this device vary widely, the default states will not be suitable for all applications. Refer back to Table 3-4 for the device's control states after a Reset operation. The following code sequences are illustrative and may not represent the most efficient way to perform an initialization. Each system designer should plan his own routine to initialize the device based on his particular application. The example shown in Table 3-15 initializes LAN CAM devices that are vertically cascaded. Code is included to set the Page Address registers of each of the devices in the chain.

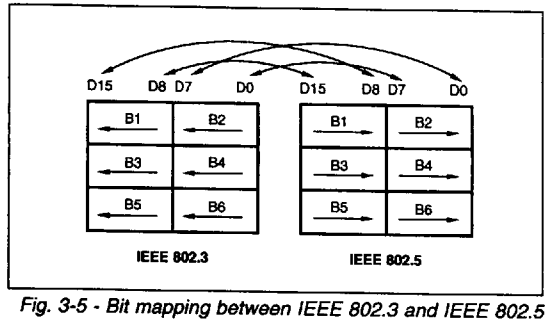


Fig. 3-5 - Bit mapping between IEEE 802.3 and IEEE 802.5

Cycle Type	Opcode or Data on Data Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Command Write	TCO DS	L	L	L	H	Target Device Select register to disable local device selection	
Command Write	FFFFH	L	L	L	H	Disables Device Select feature	
Command Write	TCO CT	L	L	L	H	Target Control register for reset	1
Command Write	0000H	L	L	L	H	Causes reset	1
Command Write	TCO PA	L	L	L	H	Target Page Address register to set page for cascaded operation	2
Command Write	xxxxH	L	L	L	H	Page Address value	2
Command Write	SFF	L	L	L	H	Set Full flag; allows access to next device (repeat previous 2 instructions for each device in chain)	2
Command Write	TCO CT	L	L	L	H	Target Control register for reset of Full flags, but not Page Address.	1
Command Write	0000H	L	L	L	H	Causes Reset	1
Command Write	TCO CT	L	L	L	H	Target Control register for initial values	3
Command Write	8040H	L	L	L	H	Control register value	3
Command Write	TCO SC	L	L	L	H	Target Segment Counter Control register	
Command Write	1080H	L	L	L	H	Both Segment counters = 0 and set to load 48-bits (3 segments)	4

Notes:

1. The TCO CT immediate field bit assignments translate to 0000H for the Reset operation. The default power-up condition generates the same effect, but good programming practice dictates a software reset for initialization to account for all possible conditions.
2. These instructions may be omitted for a single P1480 application.
3. Typical LAN CAM control environment:

   Enable match flag
   Enable full flag
   Input not scrambled
   48 CAM bits, 16 RAM bits
   Disable comparison masking (can be changed as required)
   Enable address increment

   This example translates to 8040H. See Table 3-5 for Control register bit assignments.
4. The Segment Control register value is 1080H for this example (see Table 3-8).

Table 3-15 - Example Initialization Routine

CHAPTER 4
INSTRUCTION SET

4.1 INSTRUCTION FORMAT

The I/O operations of the P1480 are controlled primarily by the Control bus (/E, /CM, /W, and /EC). The secondary control mechanism of the device is via instructions loaded into the Instruction register which set up persistent and temporary operation states within the device and control internal data moves. The desired instruction is loaded from the DQ0-DQ15 bus into the Instruction register during a Command Write cycle (/CM and /W are LOW). The instruction is captured on the falling edge of /E.

The Instruction word is subdivided into fields which define the operation to be performed. The upper four Instruction register bits, IR15-IR12, are reserved for future Address field expansion, and are ignored in the P1480; they are assumed to be set LOW in the following Instruction set description. Instruction register bit IR11 is the Address flag which indicates whether or not the instruction has an Address field to be loaded on the next cycle. Instruction register bits IR10-IR8 define the Instruction type: Select Persistent Source, Select Persistent Destination, Temporary Command Override, Move, Validity Bit Control,Compare, and Special Instructions. Instruction register bits IR7 and IR6 define the masking condition, IR5-IR3 define the destination for data transfer, and IR2-IR0 define the source of a data transfer or the validity condition to be set when writing to a memory location. The instruction format is shown below. Using these field and bit definitions, the Instruction word has the following structure:

a : a : a : a : f : i : i : i : m : m : d : d : d : s : s : s where

a : a : a : a	represents upper-order address bits for future expansion;
f	represents the address flag indicating whether or not the instruction has an appended address field;
i : i : i	represents the instruction type;
m : m	represents the mask register select for data writes and moves;
d : d : d	represents the destination for data transfers; and
s : s : s	represents the source of data transfers or the validity bit setting for data transfers to memory.

Throughout the following description of the instructions, mnemonics are defined in an assembly language format. All the instructions have a common structure:

INS dst, src[msk], val

INS:	Instruction mnemonic.
dst:	Destination of the data.
src:	Source of the data.
msk:	Mask register used.
val:	Validity condition set at the location written.

4.2 INSTRUCTION SET DESCRIPTION

Instruction: Select Persistent Source (SPS)

Binary Op Code:	**0000 f000 0000 0sss**
f	**Address Field Flag**
sss	**Selected Source**

Description: The SPS instruction selects a source for Data Reads. After instruction execution, the selected source persistently remains the source for Data Reads until another SPS instruction is executed or until a Reset occurs. The Comparand register is the default persistent source after power up or Reset.

Condition	Operation	Mnemonic	Op Code
f			
0	if source is not Memory at Address, or is at Address Reg		
1	if source is Memory at Address		
sss			
000	Comparand Register	SPS CR	0000H
001	Mask Register 1	SPS MR1	0001H
010	Mask Register 2	SPS MR2	0002H
011	Reserved		
100	Memory Array at Address Register	SPS M@[AR]	0004H
100 (f=1)	Memory Array at Address	SPS M@aaaH	0804H
101	Memory at Highest-priority Match	SPS M@HM	0005H

Instruction: Select Persistent Destination (SPD)

Binary Op Code:	**0000 f001 mmdd dvvv**
f	**Address Flag**
mm	**Mask Register Select**
ddd	**Selected Destination**
vvv	**Validity Setting (if destination is a memory location)**

Description: The SPD instruction selects a destination for Data Writes. Upon execution, this instruction persistently selects the destination for Data Writes until another SPD instruction is executed or until a Reset. The Comparand register is the default destination for Data Writes.

When the selected destination is the Comparand register or the Memory array, the Data Writes may be masked by the selected Mask register, MR1 or MR2. When Data Writes are masked, only those bits in the destination that correspond to bits containing 0's in the selected Mask register will be modified. Bits in the destination corresponding to bits containing 1's in the selected Mask register will remain unchanged.

Writing to the Comparand register or a Mask register causes a comparison to occur. Writing to the Memory array does not cause a comparison to occur. The next free address is generated when any instruction that could potentially affect the Validity bits is executed.

Instruction: Select Persistent Destination (SPD) (Continued)

Condition	Operation	Mnemonic	Op Code
f			
0	if destination is not Memory at Address, or is at Address Reg		
1	if destination is Memory at Address		
mm			
00	No Mask		
01	Mask Write with Mask Register 1		
10	Mask Write with Mask Register 2		
11	Reserved		
vvv			
100	Set Valid		
101	Set Empty		
110	Set Skip		

Instruction: Select Persistent Destination (Continued)

Condition	Operation	Mnemonic	Op Code
111	Set Random Access Location		
ddd			
000	Comparand Register	SPD CR	0100H
	Masked by MR1	SPD CR[MR1]	0140H
	Masked by MR2	SPD CR[MR2]	0180H
001	Mask Register 1	SPD MR1	0108H
010	MaskRegister 2	SPD MR2	0110H
011	Reserved		
100	Memory at Address Reg set Valid	SPD M@AR,V	0124H
	Masked by MR1	SPD M@AR[MR1],V	0164H
	Masked by MR2	SPD M@AR[MR2],V	01A4H
100	Memory at Address Reg set Empty	SPD M@[AR],E	0125H
	Masked by MR1	SPD M@[AR][MR1],E	0165H
	Masked by MR2	SPD M@[AR][MR2],E	01A5H
100	Memory at Address Reg set Skip	SPD M@[AR],S	0126H
	Masked by MR1	SPD M@[AR][MR1],S	0166H
	Masked by MR2	SPD M@[AR][MR2],S	01A6H
100	Memory at Address Reg set Random	SPD M@[AR],R	0127H
	Masked by MR1	SPD M@[AR][MR1],R	0167H
	Masked by MR2	SPD M@[AR][MR2],R	01A7H
100	Memory at Address set Valid	SPD M@aaaH,V	0924H
	Masked by MR1	SPD M@aaaH[MR1],V	0964H
	Masked by MR2	SPD M@aaaH[MR2],V	09A4H
100	Memory at Address set Empty	SPD M@aaaH,E	0925H
	Masked by MR1	SPD M@aaaH[MR1],E	0965H
	Masked by MR2	SPD M@aaaH[MR2],E	09A5H
100	Memory at Address set Skip	SPD M@aaaH,S	0926H
	Masked by MR1	SPD M@aaaH[MR1],S	0966H
	Masked by MR2	SPD M@aaaH[MR2],S	09A6H
100	Memory at Address set Random Access	SPD M@aaaH,R	0927H
	Masked by MR1	SPD M@aaaH[MR1],R	0967H
	Masked by MR2	SPD M@aaaH[MR2],R	09A7H
101	Memory at Highest-priority Match,Valid	SPD M@HM,V	012CH
	Masked by MR1	SPD M@HM[MR1],V	016CH
	Masked by MR2	SPD M@HM[MR2],V	01ACH
101	Memory at Highest-priority Match,Empty	SPD M@HM,E	012DH
	Masked by MR1	SPD M@HM[MR1],E	016DH
	Masked by MR2	SPD M@HM[MR2],E	01ADH
101	Memory at Highest-priority Match, Skip	SPD M@HM,S	012EH
	Masked by MR1	SPD M@HM[MR1],S	016EH
	Masked by MR2	SPD M@HM[MR2],S	01AEH
101	Memory at High-priority Match, Random	SPD M@HM,R	012FH
	Masked by MR1	SPD M@HM[MR1],R	016FH
	Masked by MR2	SPD M@HM[MR2],R	01AFH
110	Memory at Next Free Address, Valid	SPD M@NF,V	0134H
	Masked by MR1	SPD M@NF[MR1],V	0174H
	Masked by MR2	SPD M@NF[MR2],V	01B4H
110	Memory at Next Free Address,Empty	SPD M@NF,E	0135H
	Masked by MR1	SPD M@NF[MR1],E	0175H
	Masked by MR2	SPD M@NF[MR2],E	01B5H
110	Memory at Next Free Address, Skip	SPD M@NF,S	0136H
	Masked by MR1	SPD M@NF[MR1],S	0176H
	Masked by MR2	SPD M@NF[MR2],S	01B6H
110	Memory at Next Free Address, Random	SPD M@NF,R	0137H
	Masked by MR1	SPD M@NF[MR1],R	0177H
	Masked by MR2	SPD M@NF[MR2],R	01B7H
111	Reserved		

Instruction: Temporary Command Override (TCO)

Binary Op-Code: **0000 0010 00dd d000**
ddd **Register selected as source or destination for only the next Command Read or Write cycle.**

Description: When a TCO instruction is executed, the temporarily selected register becomes the source or destination for only the next Command Read or Write cycle, respectively. Once either of those cycles occurs, subsequent Command Read or Write cycles revert to reading the Status register and writing the Instruction register during Command Reads or Writes. The special TCO PS or TCO PD instructions allow the user to read which persistent source or destination has been selected in the next Command Read cycle. Loading either of these instructions causes the subsequent Command Read cycle to access the "sss" value of the last SPS instruction loaded or the "ddd" value of the last SPD instruction loaded. If either of these instructions is followed by a Command Write cycle, no action occurs. The TCO instruction permits access to the Instruction Address register for diagnostic purposes. Also, the Next Free Address register is Read Only, and Writes to the Page Address register invalidate the contents of the Status register.

Instruction: Temporary Command Override (Continued)

Condition	Operation	Mnemonic	Op Code
sss			
000	Control Register	TCO CT	0200H
001	Page Address Register	TCO PA	0208H
010	Segment Control Register	TCO SC	0210H
011	Next Free Adress Register	TCO NF	0218H
100	Instruction Address Register	TCO AR	0220H
101	Device Select Register	TCO DS	0228H
110	Read Persistent Source	TCO PS	0230H
111	Read Persistent Destination	TCO PD	0238H

Instruction: Data Move (MOV)

Binary Op-code: **0000 f011 mmdd dsss or 0000 f011 mmdd dvss**
f **Address Field Flag**
mm **Mask Register select**
ddd **Destination of Data**
sss **Source of Data**
v **Validity setting if destination is a memory location**

Description: The MOV instruction transfers the data in the selected source to the selected destination. Data transfers between the Memory array and the Comparand register may be masked by the selected Mask register, MR1 or MR2. If the transfer is masked, only those bits in the destination which correspond to bits containing 0's in the selected Mask register will be altered. Destination bits which correspond to bits containing 1's in the selected Mask register will remain unchanged.

The Validity bits of a Memory location used as a destination for a MOV instruction will be set to the Valid state or left unchanged, depending on the nature of the operation. If the source and destination are selected to be the same register in register-to-register operations, no net change to the state of the LAN CAM occurs. This operation would be equivalent to a NOP.

Condition	Operation	Mnemonic	Op Code
f			
0	if source or destination is not Memory at Address, or is at Address Register		
1	if source or destination is Memory at Address		
mm			
00	No Mask		
01	Mask Write with Mask Register 1		
10	Mask Write with Mask Register 2		
11	Reserved		
v			
0	No change to Validity Condition		
1	Set Valid: SKIP=0, EMPTY=0		

Instruction: Data Move (Continued)

Condition		Operation	Mnemonic	Op Code
ddd	sss			
000		Comparand Register from:		
	000	No Operation	NOP	0300H
	001	Mask Register 1	MOV CR,MR1	0301H
	010	Mask Register 2	MOV CR,MR2	0302H
	011	Reserved		
	100	Memory at Address Register	MOV CR,[AR]	0304H
		Masked by MR1	MOV CR,[AR][MR1]	0344H
		Masked by MR2	MOV CR,[AR][MR2]	0384H
		Memory at Address	MOV CR,aaaH	0B04H
		Masked by MR1	MOV CR,aaaH[MR1]	0B44H
		Masked by MR2	MOV CR,aaaH[MR2]	0B84H
	101	Memory at Highest-priority Match	MOV CR,HM	0305H
		Masked by MR1	MOV CR,HM[MR1]	0345H
		Masked by MR2	MOV CR,HM[MR2]	0385H
	110	Reserved		
	111	Reserved		
001		Mask Register 1 from:		
	000	Comparand Register	MOV MR1,CR	0308H
	001	No Operation	NOP	0309H
	010	Mask Register 2	MOV MR1,MR2	030AH
	011	Reserved		
	100	Memory at Address Register	MOV MR1,[AR]	030CH
	100 (f=1)	Memory at Address	MOV MR1,aaaH	0B0CH
	101	Memory at Highest-priority Match	MOV MR1,HP	030DH
	110	Reserved		
	111	Reserved		
010		Mask Register 2 from:		
	000	Comparand Register	MOV MR2,CR	0310H
	001	Mask Register 1	MOV MR2,MR1	0311H
	010	No Operation	NOP	0312H
	011	Reserved		
	100	Memory at Address Register	MOV MR2,[AR]	0314H
	100 (f=1)	Memory at Address	MOV MR2,aaaH	0B14H
	101	Memory at Highest-priority Match	MOV MR2,HP	0315H
	110	Reserved		
	111	Reserved		
011		Reserved		
100		Memory at Address Register, No Change to Validity bits, from:		
	000	Comparand Register	MOV [AR],CR	0320H
		Masked by MR1	MOV [AR],CR[MR1]	0360H
		Masked by MR2	MOV [AR],CR[MR2]	03A0H
	001	Mask Register 1	MOV [AR],MR1	0321H
	010	Mask Register 2	MOV [AR],MR2	0322H
	011	Reserved		
100		Memory at Address Register, Location set Valid, from:		
	100	Comparand Register	MOV [AR],CR,V	0324H
		Masked by MR1	MOV [AR],CR[MR1],V	0364H
		Masked by MR2	MOV [AR],CR[MR2],V	03A4H
	101	Mask Register 1	MOV [AR],MR1,V	0325H
	110	Mask Register 2	MOV [AR],MR2,V	0326H

Instruction: Data Move (Continued)

Condition		Operation	Mnemonic	Op Code
ddd	sss			
	111	Reserved		
100	(f=1)	Memory at Address, No Change to Validity bits, from:		
	000	Comparand Register	MOV aaaH,CR	0B20H
		Masked by MR1	MOV aaaH,CR[MR1]	0B60H
		Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
	001	Mask Register 1	MOV aaaH,MR1	0B21H
	010	Mask Register 2	MOV aaaH,MR2	0B22H
	011	Reserved		
100	(f=1)	Memory at Address, Location set Valid, from:		
	100	Comparand Register	MOV aaaH,CR,V	0B24H
		Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
		Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
	101	Mask Register 1	MOV aaaH,MR1,V	0B25H
	110	Mask Register 2	MOV aaaH, MR2,V	0B26H
	111	Reserved		
101		Memory at Highest-priority Match, No Change to Validity bits, from:		
	000	Comparand Register	MOV HM,CR	0328H
		Masked by MR1	MOV HM,CR[MR1]	0368H
		Masked by MR2	MOV HM,CR[MR2]	03A8H
	001	Mask Register 1	MOV HM,MR1	0329H
	010	Mask Register 2	MOV HM,MR2	032AH
	011		Reserved	
101		Memory at Highest-priority Match, Location set Valid, from:		
	100	Comparand Register	MOV HM,CR,V	032CH
		Masked by MR1	MOV HM,CR[MR1],V	036CH
		Masked by MR2	MOV HM,CR[MR2],V	03ACH
	101	Mask Register 1	MOV HM,MR1,V	032DH
	110	Mask Register 2	MOV HM,MR2,V	032EH
	111	Reserved		
110		Memory at Next Free Address, No Change to Validity bits, from:		
	000	Comparand Register	MOV NF,CR	0330H
		Masked by MR1	MOV NF,CR[MR1]	0370H
		Masked by MR2	MOV NF,CR[MR2]	03B0H
	001	Mask Register 1	MOV NF,MR1	0331H
	010	Mask Register 2	MOV NF,MR2	0332H
	011		Reserved	
110		Memory at Next Free Address, Location set Valid, from:		
	100	Comparand Register	MOV NF,CR,V	0334H
		Masked by MR1	MOV NF,CR[MR1],V	0374H
		Masked by MR2	MOV NF,CR[MR2],V	03B4H
	101	Mask Register 1	MOV NF,MR1,V	0335H
	110	Mask Register 2	MOV NF,MR2,V	0336H
	111	Reserved		
111		Reserved		

Instruction: Validity Bit Control (VBC)

Binary Op-code: 0000 f100 00dd dvvv
f Address Field Flag
ddd Destination of data
vvv Validity setting for Memory location

Description: The VBC instruction sets the Validity bits to the selected state at the selected Memory location or locations. Validity bits can be accessed randomly or associatively. The VBC instruction can be used in conjunction with the appropriate Compare instruction to compare on any Validity condition.

Condition		Operation	Mnemonic	Op Code
f				
0		if source or destination is not Memory at Address, or is at Address register		
1		if source or destination is Memory at Address		
ddd	vvv			
000		Reserved		
001		Reserved		
010		Reserved		
011		Reserved		
	000	Reserved for all ddd		
	001	Reserved for all ddd		
	010	Reserved for all ddd		
	011	Reserved for all ddd		
100		Set Validity bits at Address Register		
	100	Set Valid	VBC [AR],V	0424H
	101	Set Empty	VBC [AR],E	0425H
	110	Set Skip	VBC [AR],S	0426H
	111	Set Random Access	VBC [AR],R	0427H
100	(f=1)	Set Validity bits at Address		
	100	Set Valid	VBC aaaH,V	0C24H
	101	Set Empty	VBC aaaH,E	0C25H
	110	Set Skip	VBC aaaH,S	0C26H
	111	Set Random Access	VBC aaaH,R	0C27H
101		Set Validity bits at Highest-priority Match		
	100	Set Valid	VBC HM,V	042CH
	101	Set Empty	VBC HM,E	042DH
	110	Set Skip	VBC HM,S	042EH
	111	Set Random Access	VBC HM,R	042FH
110		Reserved		
111		Set Validity bits at All Matching Locations		
	100	Set Valid	VBC ALM,V	043CH
	101	Set Empty	VBC ALM,E	043DH
	110	Set Skip	VBC ALM,S	043EH
	111	Set Random Access	VBC ALM,R	043FH

Instruction: Compare (CMP)

Binary Op-code: 0000 0101 0000 0vvv
vvv Validity condition

Description: The CMP instruction forces a Comparison after a cycle, such as a Memory Write cycle, which does not automatically result in a Comparison. Destinations to which Write cycles cause an automatic Comparison are the Comparand register, the Mask registers, and the Control register.

The CMP E instruction forces the generation of the next free address. The Memory array at the next free address does not need to be a Persistent Destination. The CMP S instruction is used with the VBC instruction to return all skipped locations to the Valid state after processing multiple matches. The CMP R instruction permits associative access to any Random-access-only Memory locations.

Condition	Operation	Mnemonic	Op Code
vvv			
000	Reserved		
001	Reserved		
010	Reserved		
011	Reserved		
100	Compare Valid Locations	CMP V	0504H
101	Compare Empty Locations	CMP E	0505H
110	Compare Skipped Locations	CMP S	0506H
111	Compare Random Access Locations	CMP R	0507H

INSTRUCTION: SET FULL FLAG (SFF)

Binary Op-code: 0000 0111 0000 0000

Description: The SFF instruction is a special instruction used to force the Full flag LOW for a device whose /FI input is LOW, but whose /FF output is HIGH. SFF is used in vertically cascaded systems for selecting each device in turn to initialize its Page Address register.

Condition	Operation	Mnemonic	Op Code
	Set Full Flag	SFF	0700H

CHAPTER 5
SYSTEM CONSIDERATIONS

5.1 P1480 BUS INTERFACE

Although the P1480 is a memory device, it does not have conventional address inputs. Therefore, the system should treat the device as a memory-mapped or I/O-mapped peripheral.

The Data bus to and from the P1480 (DQ15-DQ0) is connected to the system Data bus via any necessary buffers. The Chip Enable (/E) can be generated in the system by decoding the upper-order address bits, and Write Enable (/W) can be connected to the CPU Control bus. Using the Associative access facilities on the chip may remove the need for external decoding.

The four logical combinations of the Command (/CM) and Enable Comparison (/EC) inputs can be generated through the memory mapping scheme. Address bits A15 and A14 are used to drive /CM and /EC, respectively, while the remaining address bits are fed to decoder logic to map the P1480 into some predefined address space, as shown in Table 5-1.

The following design example uses this type of memory mapping scheme. This technique allows the LAN CAM to be incorporated easily into conventional memory designs. The simplest example was used to illustrate the concept. No provisions were made for the hardware Match or Full indications nor the vertical expansion of a CAM array. Although the device operates synchronously, the timing fits in with conventional microprocessor bus requirements. This example is not intended to be used directly by a prospective user.

Note: System designers are cautioned to verify their own designs while using this example solely as a general guide.

5.2 DESIGN CONSIDERATIONS

When designing the printed circuit layout for a system that incorporates the P1480, high-speed memory design practice must be applied to the power supply, circuit board, and associated wiring, particularly where multiple CAMs are used in the system. The parallel operation of the LAN CAM causes transient currents whose influence must be filtered out from the power supply to maintain data intergity.

The system design must incorporate low-impedence power planes, decoupled with bulk capacitance at the power entry point, and as close to each device as possible, a low-inductance, high-frequency capacitor whose nominal value is 0.1uF. Printed circuit traces must be as short and straight as possible to reduce inductance and signal-to-signal coupling.

5.3 HARDWARE DESIGN EXAMPLE

Having outlined the application of the P1480 in the LAN Bridge in earlier discussions, a more detailed discussion follows which describes the interface between an Intel™ 80286™ microprocessor and the P1480. This circuit configuration would be suitable for the LAN bridge application, as well as for a wide range of other applications where associative memory access is beneficial. Although only one P1480 is incorporated in the described memory array, the interfacing principles can be extended to larger CAM capacities for storing larger station lists using the techniques for vertical cascading described in Chapter 3.

Fig. 5-1 shows a circuit diagram of a rudimentary 80286-based CPU. No interrupt, DMA or I/O facilities are shown so as to highlight the memory interface. In real systems, these and other facilities will be added as needed. The circuit of Fig. 5-1 does show the Data, Address and Control buses which interface to the memory system shown in Fig. 5-2. Table 5-1 shows a possible Memory map for the system.

The CPU shown in Fig. 5-1 follows Intel™ design recommendations. No further details of the circuit will be given here; if more information is required, refer to the appropriate literature, such as one of the many independently published books on the iAPX86™ microprocessor family.

The Memory system shown in Fig. 5-2 comprises 512K bytes of SRAM, 4K words of CAM and 128K bytes of EPROM. The memory is addressable as words, high-order bytes or low-order bytes. In the SRAM portion of the memory there are four 64Kx16 banks, each holding two 64K-byte segments. In the EPROM portion of the memory there is one 64Kx16 memory bank which holds two 64K-byte segments. Although the P1480 has 1K 64-bit locations, these are not directly accessable via the system address bus in this approach. There are only four directly addressable facilities in the device. As shown in the System memory map, the first such facility is the Command structure of the device which is accessed at any memory system location between 0C0000H and 0C7FFFH. A Command Write cycle or a Command Read cycle to an address between 0C0000H and 0C3FFFH enables the Match flag, while one between 0C4000H and 0C7FFFH does not. The second address-accessible resource within the device is the Data I/O which is accessed at any memory system location between addresses 0C8000H and 0CFFFFH. A Data Read or Write cycle to an address between 0C8000H and 0CBFFFH enables the Match flag, while one between 0CC000H and 0CFFFFH does not. Random access into theP1480 Memory array is done by selecting the Memory array at address as the persistent source or destination for Data Read or Write cycles.

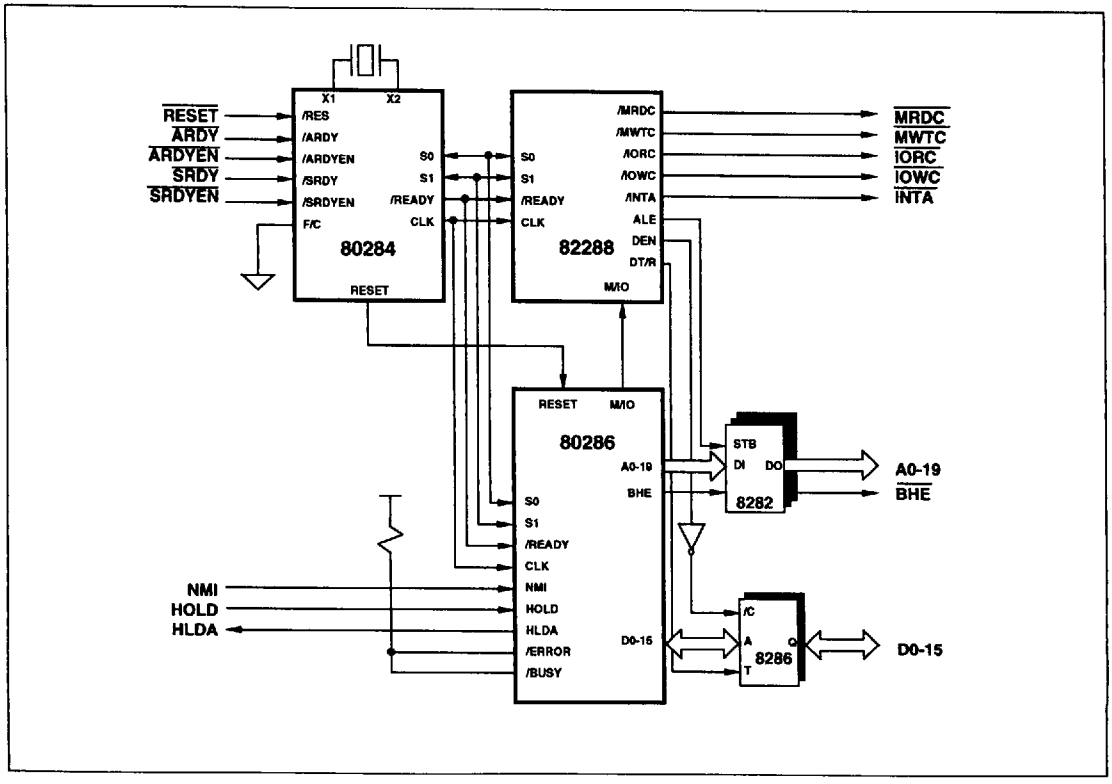


Fig. 5-1 - An 80286-based CPU

BYTE ADDRESS	MEMORY ALLOCATION	
	D15 D8	D7 D0
00000H-0FFFFH	RAM SEGMENT 0(H)	RAM SEGMENT 0(L)
10000H-1FFFFH	RAM SEGMENT 1(H)	RAM SEGMENT 1(L)
20000H-2FFFFH	RAM SEGMENT 2(H)	RAM SEGMENT 2(L)
30000H-3FFFFH	RAM SEGMENT 3(H)	RAM SEGMENT 3(L)
40000H-4FFFFH	RAM SEGMENT 4(H)	RAM SEGMENT 4(L)
50000H-5FFFFH	RAM SEGMENT 5(H)	RAM SEGMENT 5(L)
60000H-6FFFFH	RAM SEGMENT 6(H)	RAM SEGMENT 6(L)
70000H-7FFFFH	RAM SEGMENT 7(H)	RAM SEGMENT 7(L)
80000H-BFFFFH	UNUSED	
C0000H-C3FFFH	CAM COMMAND AND ENABLE MATCH FLAG	
C4000H-C7FFFH	CAM COMMAND AND DISABLE MATCH FLAG	
C8000H-CBFFFH	CAM DATA AND ENABLE MATCH FLAG	
CC000H-CFFFFH	CAM DATA AND DISABLE MATCH FLAG	
D0000H-DFFFFH	UNUSED	
E0000H-EFFFFH	EPROM SEGMENT 0 (H)	EPROM SEGMENT 0 (L)
F0000H-FFFFFH	EPROM SEGMENT 1 (H)	EPROM SEGMENT 1 (L)

Table 5-1 - An Example Memory Map

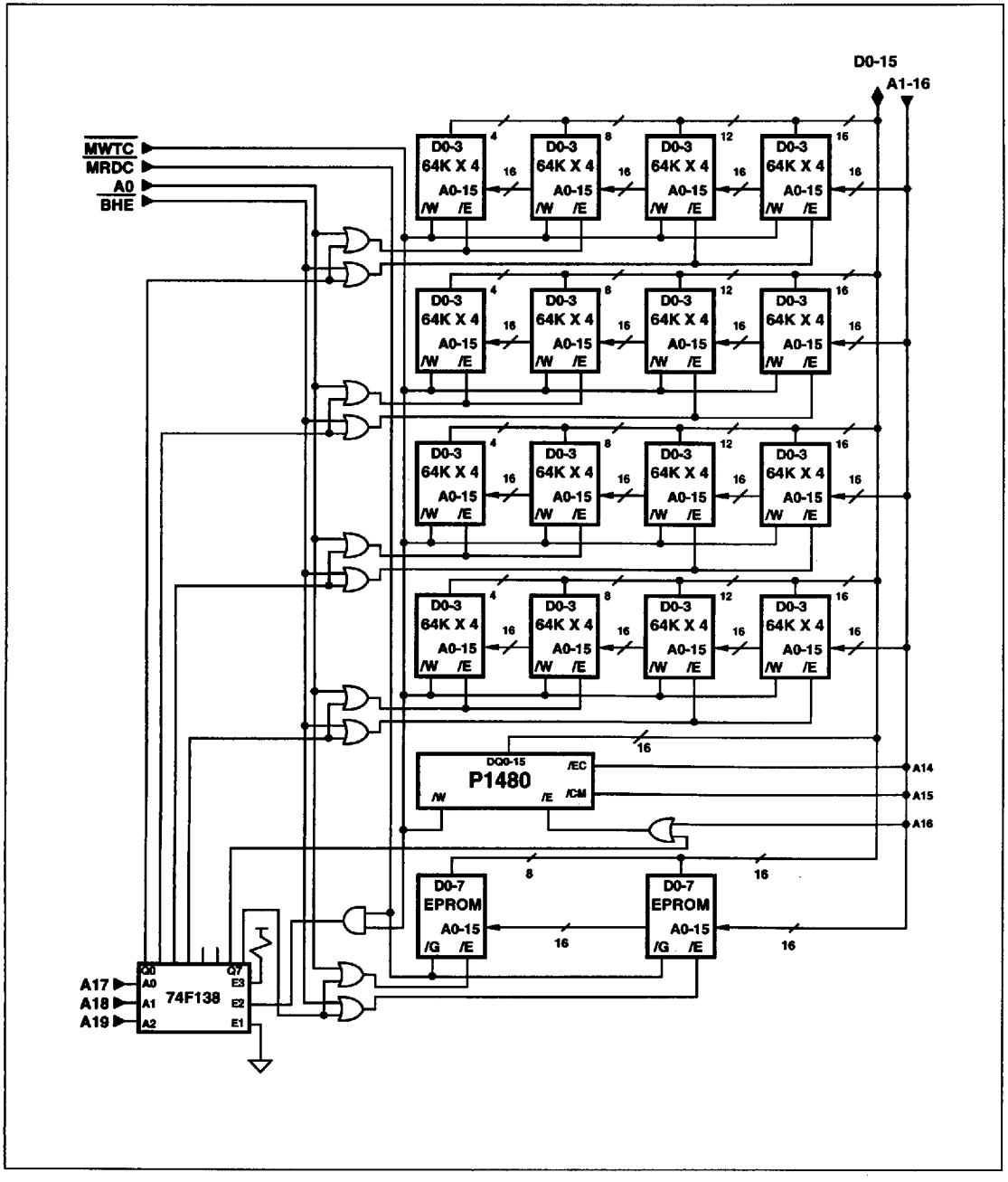


Fig. 5-2 - A Memory System Using the LAN CAM

Selection of the address-accessible resources within the P1480 is done through the control of the /CM and /EC inputs. If the /CM line is LOW, the Command structure is accessed; if the /CM line is HIGH, the Data I/O is accessed; if the /EC line is LOW, /MF is enabled; if the /EC line is HIGH, /MF is disabled. In the Memory system shown in Fig. 26, the /CM line is controlled by the A15 line and the /EC line is controlled by the A14 line from the system address bus. The CAM is enabled between addresses 0C0000H and 0CFFFFH by the decoding of the system address lines A16-A19. This coarse decoding produces address aliasing, where the four accessable resources of the CAM are each accessible in a 16 Kbyte block. In a system where more memory space is needed, a more efficient decoding scheme could be used to reduce the memory space taken by the CAM's four facilities.

5.4 SOFTWARE DESIGN EXAMPLE

Having described the hardware interface for the P1480 to an Intel™ 80286™ micro- processor, this Subsection references the CPU circuit diagram shown in Fig. 5-1, the Memory system circuit diagram shown in Fig. 5-2 and the System memory map shown in Table 5-1.

Although the program segments contained in this section are extensively commented, familiarity with iAPX86 assembly language is assumed. These code segments are not intended to be stand-alone programs, but rather to act as general examples to help the user to understand the software implications of having the P1480 resident in the system memory. Although some programming overhead is shown in the foregoing code, it has been provided only as necessary for the example program segments; complete system software will need substantially more overhead which may require changes in the structure of the code described here.

The following code uses the iAPX86 Real Address mode for simplicity and clarity. The use of this mode means that the 80286 can address a 1M-byte memory space; the physical address comprises a Segment address added to an Offset address. The Segment address is a 16-bit word, but it is shifted four bits left with zeros in the least-significant four bits prior to being added to the Offset address, giving a 20-bit byte- address field. Four Segment counters in the microprocessor, the CS register for the Code Segment address, the DS register for the Data Segment address, the ES register for the Extra Segment address, and the SS register for the Stack Segment address. Code, Data, and Stack accesses default to their respective registers. The Segments can overlap, and Segment addresses can be changed or overridden for any of the Segments by using an instruction.

The code contained in this section is designed to be relocatable. Absolute addresses have to be provided to the linker after the assembler has generated relocatable object code. However, the assembly-level code has to take into account some aspects of the physical memory mapping. Specifically, the P1480 resides in Segment 0C0000H in the memory, the Instruction register and Status register are at an offset of 0H with /MF enabled and 4000H with /MF disabled, while the Data I/O is at an offset of 8000H with /MF enable and 0C000H with /MF disabled.

The following program segment performs various data-initialization tasks: reserves 512 bytes of Stack storage space, and initializes each location to zero; sets the PNC1480 Segment address to 0C000H; sets the Instruction register and Status register Offset Address with /MF enabled or disabled to 0H and 4000H, respectively; sets the Data I/O bus Offset Address with /MF enabled or disabled to 8000H and C000H, respectively; reserves 4K of memory storage to buffer 1K of 64-bit contents which will be loaded *into* the CAM during initialization; reserves 0.75K of memory to store 256 48-bit comparands; reserves 48 words of memory storage to buffer 16 48-bit Mask values; reserves 1K of memory storage to hold a look-up table which can be pointed to by Match addresses for applications which need more Associated data space than the 16 bits for each entry already provided on the chip; and sets values for various P1480 instructions and control words. Clearly, this data definition section will vary from system to system and should be used only as a guide. Further, system data will also be included in this section of the program.

Note: Use this code solely as a guide and example.

AN EXAMPLE PROGRAM

```
;SAMPLE PROGRAM SEGMENTS TO DEMONSTRATE THE SOFTWARE INTERFACE BETWEEN AN 80286
;MICROPROCESSOR AND THE PNC1480 LAN CAM CONTENT-ADDRESSABLE MEMORY.

  STACK          SEGMENT PARA 'STACK'

;DEFINE STACK STORAGE AREA IN RAM
                 DB 512 DUP 0H          ;RESERVE 512 BYTES FOR STACK
  STACK          ENDS

  DATA           SEGMENT PARA 'DATA'

;DEFINE CAM SEGMENT AND OFFSET ADDRESSES
  CAM_SEG        EQU 0C000H             ;DEFINE CAM SEGMENT ADDRESS
  CAM_CMD_EN     EQU 0H                 ;DEFINE CAM COMMAND WITH /MF-ENABLE OFFSET
  CAM_CMD_DIS    EQU 04000H             ;DEFINE CAM COMMAND WITH /MF-DISABLE OFFSET
  CAM_DATA_EN    EQU 08000H             ;DEFINE CAM DATA WITH /MF-ENABLE OFFSET
  CAM_DATA_DIS   EQU 0C000H             ;DEFINE CAM DATA WITH /MF-DISABLE OFFSET

;DEFINE STORAGE AREAS IN RAM
  CONTENTS       DW 4096 DUP 0H         ;RESERVE 4096 WORDS FOR 1K CAM ENTRIES IN RAM
  COMPARANDS     DW 768 DUP 0H          ;RESERVE 768 WORDS FOR 256 COMPARANDS IN RAM
```

```
   MASKS          DW 48 DUP 0H          ;RESERVE 48 WORDS FOR 16 MASK VALUES IN RAM
   L_TABLE        DW 1024 DUP 0H        ;RESERVE 1024 WORDS TO HOLD 1K-ENTRY LIST

;DEFINE LENGTHS OF STORAGE AREAS
   CONT_BUF_SIZE  EQU 01000H            ;DEFINE SIZE OF CONTENTS BUFFER
   COMP_BUF_SIZE  EQU 0300H             ;DEFINE SIZE OF COMPARAND BUFFER
   MASK_BUF_SIZE  EQU 010H              ;DEFINE SIZE OF MASK BUFFER
   TABLE_SIZE     EQU 0400H             ;DEFINE SIZE OF LOOK-UP TABLE
;DEFINE VALUES FOR CAM INSTRUCTIONS AND CONTROL
   PAGE_ADDR      EQU 0H                ;CAM PAGE ADDRESS
   CAM_RESET      EQU 0000H             ;RESET CAM
   CAM_INT        EQU 08060H            ;CONTROL REGISTER VALUE FOR LAN BRIDGE
   LAN_SEG_ORG1   EQU 013C3H            ;SEGMENT CONTROL REGISTER VALUE FOR LAN
   LAN_SEG_ORG2   EQU 01FC7H            ;  BRIDGE SRC AND DST SEGMENT COUNTER LIMITS
   SPD_M@NF,V     EQU 0134H             ;SELECT PERSISTENT DESTINATION MEMORY AT NEXT
                                        ;     FREE ADDR,SET VALID
SPD_CR            EQU 0100H             ;SELECT PERSISTENT DESTINATION COMPARAND
                                        ;     REGISTER
SPS_M@HM          EQU 0005H             ;SELECT PERSISTENT SOURCE MEMORY AT HIGHEST
                                        ;     PRIORITY MATCH ADDRESS
SPD_M@NF[MR1],V   EQU 0174H             ;SELECT PERSISTENT DESTINATION MEMORY AT NEXT ;
FREE ADDR MASKED BY MR1, SET VALID
   TCO_CT         EQU 0200H             ;TEMPORARY COMMAND OVERRIDE IN FAVOR OF
                                        ;     CONTROL REGISTER
TCO_PA            EQU 0208H             ;TEMPORARY COMMAND OVERRIDE IN FAVOR OF
                                        ;     PAGE ADDRESS REGISTER
TCO_SC            EQU 0210H             ;TEMPORARY COMMAND OVERRIDE IN FAVOR OF
                                        ;     SEGMENT CONTROL REGISTER
NOP               EQU 0300H             ;NO OPERATION COMMAND
SFF               EQU 0700H             ;SET FULL FLAG INSTRUCTION
TCO_DS            EQU 0228H             ;TEMPORARY COMMAND OVERRIDE IN FAVOR OF
                                        ;     DEVICE SELECT REGISTER
DEV_DIS           EQU FFFFH             ;CAM DEVICE DESELECT IMMEDIATE FIELD
DATA              ENDS
```

The next segment assumes that the Contents, Comparands and Look-up table buffers have been filled during the System initialization. This section initializes the CAM, loads the Page Address register, loads the Memory array with 1K 64-bit values from the Contents buffer using Direct Index addressing in the RAM and Write-at-next-free-address addressing in the CAM. This routine assumes that only one CAM device is used in the system. Extending the initialization to a vertically cascaded array is very easy. See Chapter 3 for this initialization technique. Insert that instruction flow after the SFF instruction and iterate the Page Address register loading operation as many times as there are cascaded devices.

```
   CODE           SEGMENT PARA 'CODE'
                  ASSUME CS: CODE, DS:DATA, ES: DATA, SS: STACK

;INITIALIZE THE CAM
   INIT_CAM       MOV DI, CAM_SEG       ;GET CAM SEGMENT ADDRESS
                  MOV DS, DI            ;LOAD IT INTO DS REGISTER
                  MOV DI, CAM_CMD_DIS   ;GET INSTRUCTION REGISTER OFFSET WITH /MF
                                        ;     DISABLE (COMMAND WRITE CYCLE)
                  MOV [DI],TCO_CT       ;LOAD TEMPORARY COMMAND OVERRIDE IN FAVOR
                                        ;     OF CONTROL REGISTER
                  MOV [DI],CAM_RESET    ;RESET THE CAM(S)
                  MOV [DI], TCO_DS      ;LOAD TCO IN FAVOR OF DEVICE SELECT REGISTER
                  MOV [DI], DEV_DIS     ;DISABLE DS REGISTER FUNCTION
                  MOV [DI],TCO_PA       ;LOAD TEMPORARY COMMAND OVERRIDE IN FAVOR
                                        ;     OF PAGE ADDRESS REGISTER
                  MOV [DI],PAGE_ADDR    ;PUT PAGE ADDRESS IN PAGE ADDRESS REGISTER
                  MOV [DI], SFF         ;EXECUTE SET FULL FLAG INSTRUCTION
                  MOV [DI], TCO_CT      ;LOAD TCO IN FAVOR OF CONTROL REGISTER
                  MOV [DI], CAM_RESET   ;RESET CAM TO RESET FULL FLAG
                  MOV [DI], TCO_CT      ;LOAD TCO IN FAVOR OF CONTROL REGISTER
                  MOV [DI],CAM_INT      ;LOAD INITIAL CONFIGURATION INTO CAM
                  MOV [DI], SPS_M@HM    ;LOAD SELECT PERSISTENT SOURCE MEMORY
                                        ;     ARRAY AT HIGHEST-PRIORITY MATCH ADDRESS
                  MOV [DI], TCO_SC      ;LOAD TCO IN FAVOR OF SEGMENT CONTROL REG.
                  MOV [DI], LAN_SEG_ORG1 ;LOAD SEGMENT CONTROL VALUE
```

```
;PUT EACH 64-BIT CONTENT FROM THE CONTENT BUFFER IN SYSTEM RAM INTO THE AX, BX, CX AND DX
;REGISTERS (LOWER-ORDER WORD IN AX REGISTER)

                MOV SI, 0H              ;INITIALIZE SOURCE INDEX REGISTER
CAM_LOAD        MOV DI,DATA             ;GET DATA SEGMENT ADDRESS
                MOV DS,DI               ;LOAD DATA SEGMENT ADDRESS
                MOV AX,CONTENTS[SI]     ;GET FIRST WORD OF CONTENT
                INC SI                  ;INCREMENT SOURCE INDEX
                MOV BX,CONTENTS[SI]     ;GET SECOND WORD OF CONTENT
                INC SI                  ;INCREMENT SOURCE INDEX
                MOV CX,CONTENTS[SI]     ;GET THIRD WORD OF CONTENT
                INC SI                  ;INCREMENT SOURCE INDEX
                MOV DX,CONTENTS[SI]     ;GET FOURTH WORD OF CONTENT
                INC SI                  ;POINT TO NEXT CONTENT

;PUT  THE NEXT CONTENT IN THE NEXT FREE CAM LOCATION.  REPEAT UNTIL ALL LOCATIONS ARE  FULL

                MOV DI,CAM_SEG          ;GET CAM SEGMENT ADDRESS
                MOV DS,DI               ;LOAD CAM SEGMENT ADDRESS
                MOV DI, CAM_CMD_DIS     ;GET INSTRUCTION REGISTER OFFSET WITH /MF
                                        ;     DISABLE (COMMAND WRITE CYCLE)
                MOV [DI], SPD_M@NF, V   ;LOAD SELECT PERSISTENT DESTINATION MEMORY
                                        ;     ARRAY AT NEXT FREE ADDRESS COMMAND
                MOV [DI], TCO_SC        ;LOAD TCO IN FAVOR OF SEGMENT CONTROL REG.
                MOV [DI], LAN_SEG_ORG2  ;LOAD DESTINATION SEGMENT CONTROL VALUE
                MOV DI, CAM_DATA_DIS    ;GET CAM DATA SEGMENT ADDRESS (DISABLE /MF)
                MOV [DI],AX             ;LOAD FIRST WORD OF CONTENT
                MOV [DI],BX             ;LOAD SECOND WORD OF CONTENT
                MOV [DI],CX             ;LOAD THIRD WORD OF CONTENT
                MOV [DI],DX             ;LOAD FOURTH WORD OF CONTENT
                CMP SI,CONT_BUF_SIZE    ;CHECK FOR LAST CONTENT
                JL CAM_LOAD             ;REPEAT LOAD IF NOT LAST CONTENT
                MOV DI, CAM_CMD_DIS     ;GET INSTRUCTION REGISTER OFFSET WITH /MF
                                        ;     DISABLE (COMMAND WRITE CYCLE)
                MOV [DI], TCO_SC        ;LOAD TCO IN FAVOR OF SEGMENT CONTROL REG.
                MOV [DI], LAN_SEG_ORG1  ;RELOAD DESTINATION SEGMENT CONTROL VALUE
                                        ;     SUITABLE FOR ADDRESS FILTERING
                MOV [DI], SPD_CR        ;LOAD SELECT PERSISTENT DESTINATION
                                        ;     COMPARAND REGISTER COMMAND
```

The next program segment selects a Comparand from the Comparand buffer in RAM, and loads it into the Comparand register.

```
;MOVE THE SELECTED 48-BIT COMPARAND VALUE INTO THE AX, BX, AND CX REGISTERS (LOWER-ORDER
;WORD IN THE AX REGISTER). A COMPARE CYCLE OCCURS ONCE THE WHOLE COMPARAND IS LOADED

                MOV DI,DATA             ;GET DATA SEGMENT ADDRESS
                MOV DS,DI               ;LOAD DATA SEGMENT ADDRESS
                MOV SI,10H              ;INITIALIZE SOURCE INDEX REGISTER TO POINT TO
                                        ;     SELECTED COMPARAND
                MOV AX,COMPARANDS[SI]   ;GET FIRST WORD OF COMPARAND
                INC SI                  ;INCREMENT SOURCE INDEX
                MOV BX,COMPARANDS[SI]   ;GET SECOND WORD OF COMPRAND
                INC SI                  ;INCREMENT SOURCE INDEX
                MOV CX,COMPARANDS[SI]   ;GET THIRD WORD OF COMPARAND
                INC SI                  ;INCREMENT SOURCE INDEX
                MOV DI,CAM_SEG          ;GET CAM SEGMENT ADDRESS
                MOV DS,DI               ;LOAD CAM SEGMENT ADDRESS
                MOV DI,CAM_DATA_DIS     ;GET CAM DATA OFFSET WITH /MF-DISABLE
                MOV [DI],AX             ;LOAD FIRST WORD OF COMPARAND
                MOV [DI],BX             ;LOAD SECOND WORD OF COMPRAND
                MOV DI,CAM_DATA_EN      ;GET CAM DATA OFFSET WITH /MF-ENABLE
                MOV [DI],CX             ;LOAD THIRD WORD OF COMPARAND
```

The next segment reads the associated data from the RAM field of the highest-priority matching location into the AX register of the CPU.

```
;READ THE CONTENTS OF THE 16-BIT RAM DATA FIELD AT THE MATCH ADDRESS
                MOV AX, [DI]            ;READ DATA FROM MEMORY ARRAY AT H-P MATCH
```

The next program segment reads the Status register in the CAM, checks the /MA flag for a match, and if there is a match, generates a pointer into the look-up table from the Match address.

```
;TEST /MA FLAG FOR VALID MATCH. IF VALID, GENERATE POINTER INTO LOOK-UP TABLE AND LOAD ;ACCESSED
VALUE INTO AX REGISTER

                MOV DI, CAM_CMD_EN      ;GET STATUS REGISTER OFFSET WITH /MF-ENABLE
                MOV BX, [DI]            ;READ STATUS REGISTER INTO BX REGISTER
                MOV SI, BX              ;SAVE STATUS REG IN SI REG
                AND BX, 01H             ;TEST MATCH FLAG
                JZ MATCH                ;JUMP IF MATCH VALID

                ;Do 'No Match' action

                MP CONTINUE             ;JUMP TO NEXT ACTION
MATCH           AND SI, 03H             ;MASK OUT MATCH FLAGS
                SHR SI, 01H             ;GENERATE BYTE ADDRESS
                MOV AX, L_TABLE [SI]    ;LOAD AX REG WITH VALUE FROM LOOK-UP TABLE

CONTINUE        ;Next Action
```

In the code given above, each time the CAM Data segment is accessed, the CPU DS register must be loaded with the CAM Segment address. Also, when the Data segment is accessed after a CAM access, the DS register must be reloaded, causing software overhead that can be avoided with a simple architectural expedient. Since the CAM need only reside in two memory locations, one for the Command/Status registers' buffer and one for the Comparand register/Data output, an area of RAM can be mapped into the same segment as the CAM to act as local data storage for CAM-related values.

5.5 SYSTEM TIMING ISSUES

Unlike random access memories, the P1480 is controlled by commands written into the device on the data inputs. An extra input on the Control bus selects between data and commands on the data bus. In random access mode the address is contained within the instruction. These major differences between the P1480 and RAM interfaces force a change in system design.

The simplicity of a standard microprocessor control bus reflects the simplicity of the SRAM interface. When designing a microprocessor interface to the P1480, the simple control bus must be supplemented to provide the necessary signals. The best design strategy is to use memory or I/O mapping techniques, so that each data source and destination within the P1480 is seen as a memory location from the point of view of the microprocessor. In this respect, the P1480 will be regarded by the system designer more as a peripheral than a memory device.

The synchronous interface to the P1480 requires that the data and control interfaces to the P1480 be stable at the time that /E goes LOW. This requirement can be met in a memory- mapped system by enabling the decoder with control signals that become active when the data and address lines from the microprocessor are valid. In the case of the 80286 system, the /MRDC and /MWTC controls go LOW when the address and data (in the case of /MWTC) are stable. So, these signals are used to enable the address decoder and ensure sufficient set-up time before /E is generated. For systems not using an external decoder, but rather the vertical cascading facilities offered on the LAN CAM, a similar approach to timing can be used to generate the /E signal at the appropriate time by simply gating the /E clock by the LOW state of both /MRDC and /MWTC (for write cycles).

CHAPTER 6
ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 to 7.0 Volts
Voltage on all Other Pins	–0.5 to V_{CC}+0.5 Volts (-2.0 Volts for 10ns, measured at the 50% point)
Temperature Under Bias	–40°C to +85°C
Storage Temperature	–55°C to +125°C
DC Output Current	20mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND.

OPERATING CONDITIONS (VOLTAGES REFERENCED TO GND AT THE DEVICE PIN)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1"	2.0		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	1, 2
T_A	Ambient Operating Temperature	0		70	°C	Still Air

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_{CC}	Power Supply Current			200	mA	tELEL=tELEL (min.)
$I_{CC(SB)}$	Stand-by Power Supply Current		TBD		mA	/E= HIGH
V_{OH}	Output Voltage Logic "1"	2.4			Volts	I_{OH} = -2.0 mA
V_{OL}	Output Voltage Logic "0"			0.4	Volts	I_{OL} = 4.0 mA
I_{IZ}	Input Leakage Current	-2		2	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{OZ}	Output Leakage Current	-10		10	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$; DQ_n = High Impedance

CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C_{IN}	Input Capacitance	6	pF	f=1MHz, V_{IN}=0 V.
C_{OUT}	Output Capacitance	7	pF	f=1MHz, V_{IN}=0 V.

AC TEST CONDITIONS

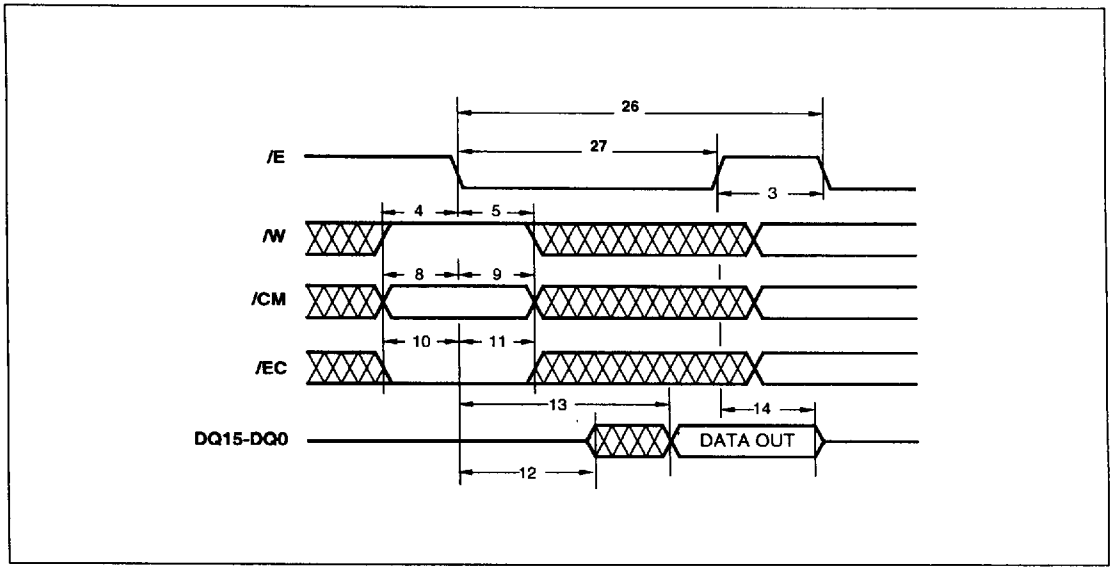
Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 volts
Output Timing Reference Level	0.8 to 2.4 volts

NOTES:
1. -1.0V for a duration of 10ns measured at the 50% amplitude points for Input-only lines (Fig. 6-3).
2. Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
3. See data sheet 3112

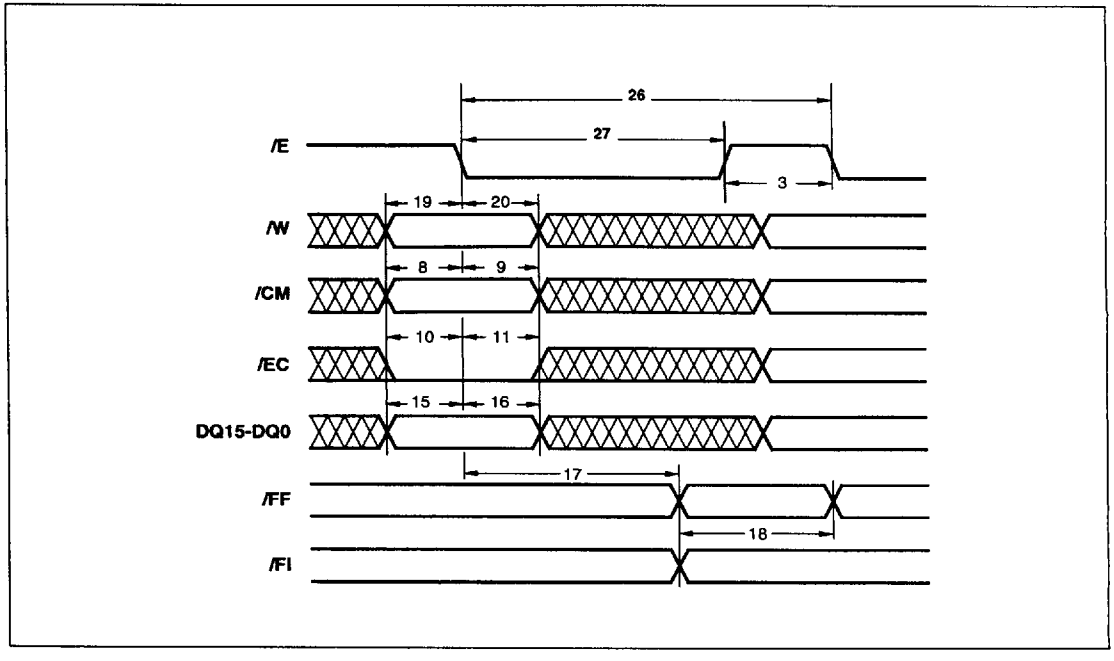
SWITCHING CHARACTERISTICS (NOTE 3)

No.	Symbol	Parameter
1	tELEL	Compare Cycle Time
2	tELEH	Chip Enable LOW Pulse Width
3	tEHEL	Chip Enable High Pulse Width
4	tWHEL	Write Enable HIGH to Chip Enable LOW
5	tELWX1	Chip Enable LOW to Write Don't Care
6	tWLEL	Write LOW to Chip Enable Low
7	tELWX2	Chip Enable LOW to Write Don't Care
8	tCMVEL	Command Valid to Chip Enable LOW
9	tELCMX	Chip Enable LOW to Command Don't Care
10	tECVEL	Enable Comparison Valid to Chip Enable LOW
11	tELECX1	Chip Enable LOW to Enable Compare Don't Care
12	tELQX	Chip Enable LOW to Outputs Active
13	tELQV	Chip Enable LOW to Data Valid
14	tELQZ	Chip Enable HIGH to Outputs High-Z
15	tDVEL	Data Valid to Chip Enable LOW
16	tELDX	Chip Enable LOW to Data Don't Care
17	tELFFV	Chip Enable LOW to Full Flag Valid
18	tFIVFFV	Full Input Valid to Full Flag Valid
19	tWVEL	Write Valid to Chip Enable LOW
20	tELWX3	Chip Enable LOW to Write Don't Care
21	tECLEL	Comparison Enable LOW to Chip Enable LOW
22	tELECX2	Chip Enable LOW to Enable Compare Don't Care
23	tEHMFV	Chip Enable HIGH to Match Flag Valid
24	tMIVMFV	Match in Valid to Match Flag Valid
25	tEHMFX	Chip Enable HIGH to Match Flag Invalid
26	tELELRW	Read/Write Cycle Time
27	tELEHRW	Chip Enable LOW Read/Write Pulse Width LOW

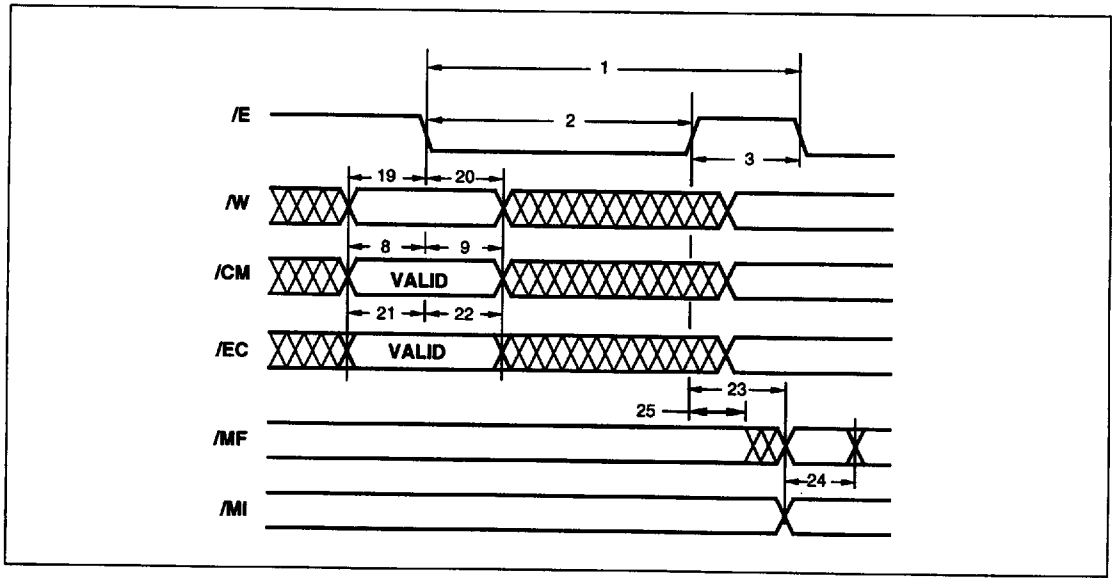
TIMING DIAGRAMS



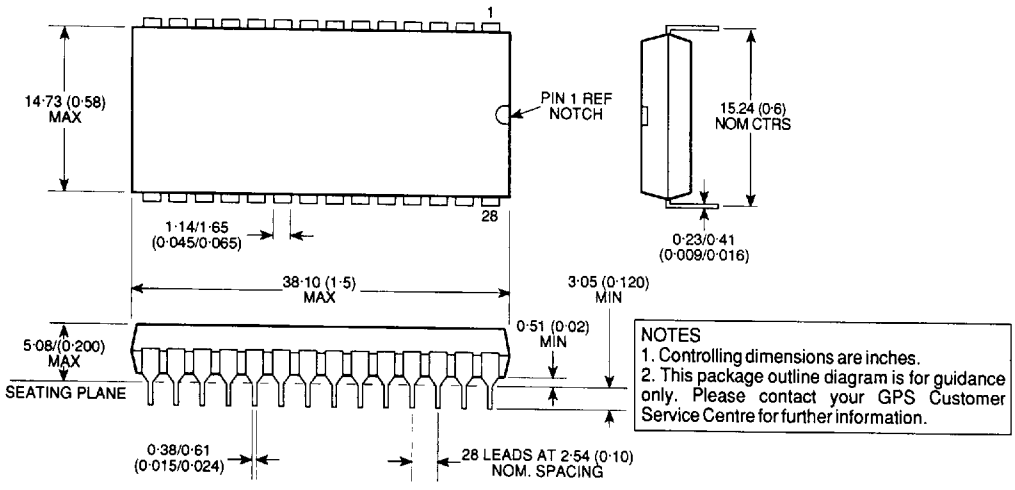
P1480 Read Cycle



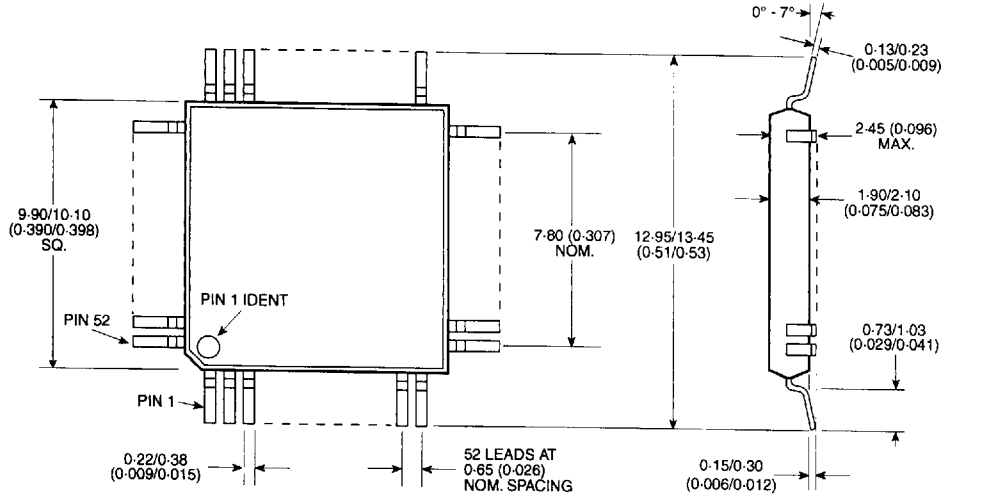
P1480 Write Cycle



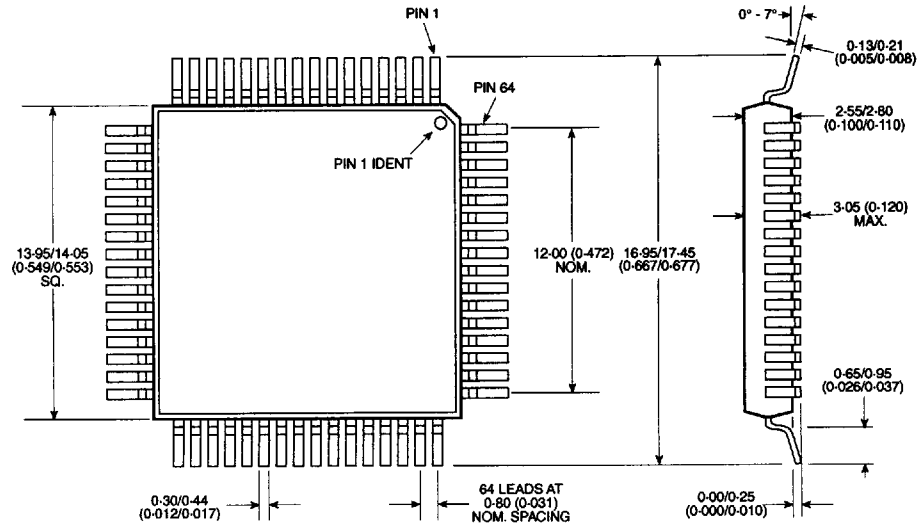
P1480 Match Flag Response



28-LEAD PLASTIC DIL – DP28

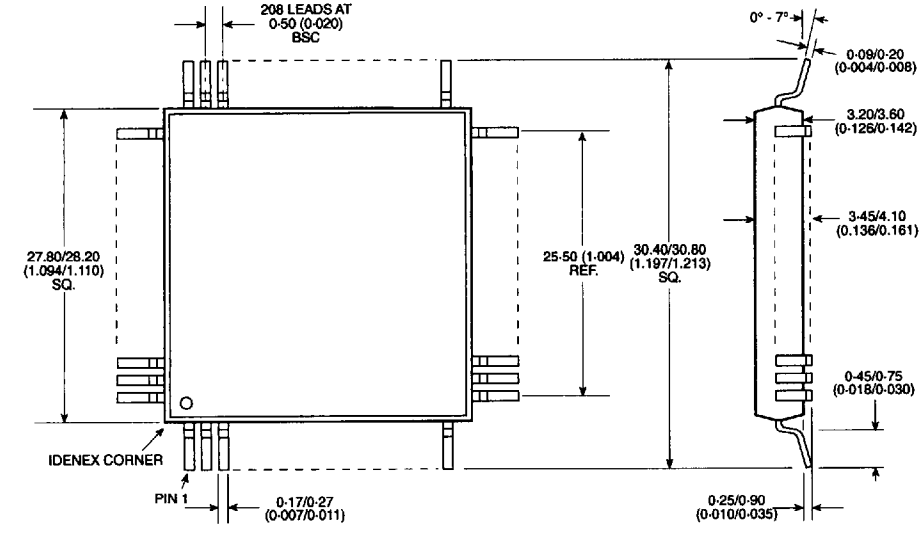


52-LEAD QUAD FLATPACK – GP52



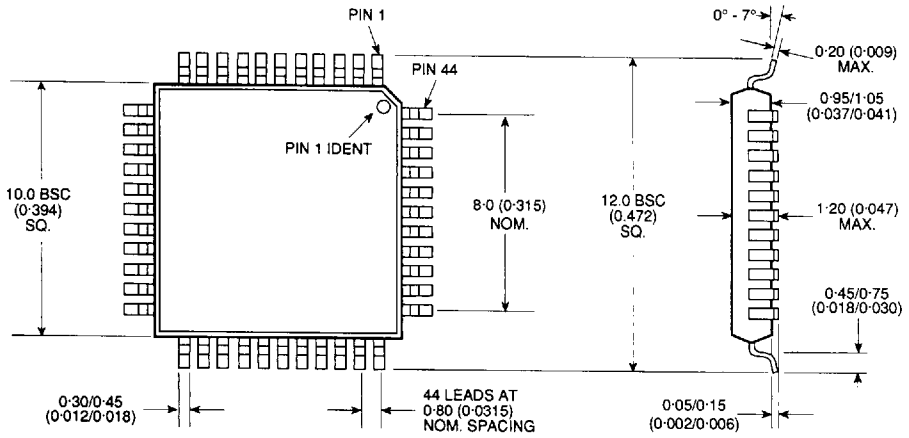
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD PLASTIC QUAD FLATPACK – GP64



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

208-LEAD PLASTIC QUAD FLATPACK – GP208



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

44-LEAD THIN PLASTIC QUAD FLATPACK – TP44