Integrated Circuit Systems, Inc.

ICS9175

Low Skew Output Buffer

General Description

The **ICS9175** is designed to generate low skew clocks for clock distribution in high performance PCs and workstations. Using a 14.318 MHz crystal and phase-locked loop technology, six output clocks are produced at a master frequency or one half of the master frequency. The rising edges of the output clocks are guaranteed to be within 250ps of one another.

There are three versions of the **ICS9175**, each designed to support a different Pentium CPU frequency.

Part Number	CPU Frequency
ICS9175-04	66.6
ICS9175-05	60
ICS9175-06	52

The **ICS9175** is ideal for generating multiple, high-drive CPU clocks for Pentium applications. It meets the typical system specification for maximum skew between outputs (250ps) and clock stability (±250ps).

The use of a phase-locked loop allows the output clocks to run at multiples of the input crystal. The patented VCO design is capable of achieving internal frequencies of greater than 150 MHz operation. In the design of the **ICS9175**, the PLL is programmed to produce internal clocks at twice the desired frequency. The output is divided in half at the output to produce symmetric waveforms. Typical duty cycle is 50% ± 1%.

Features

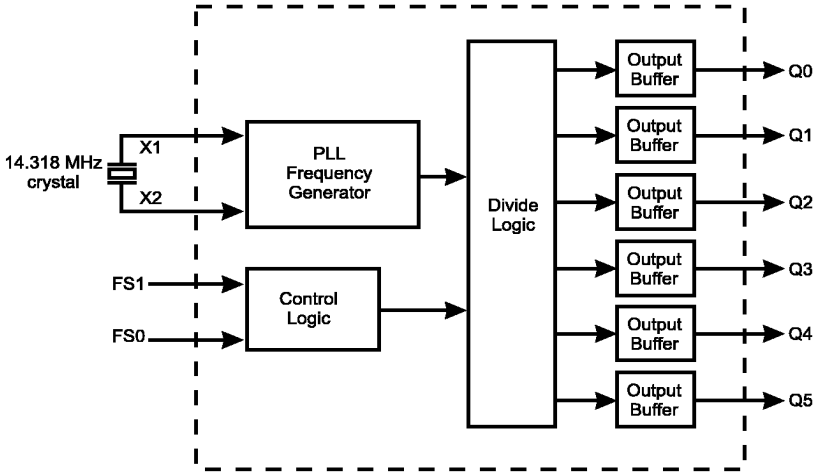
- Generates low skew clocks for Pentium™ micro-processor
- One 14.318 MHz crystal produces six output clocks
- 52 MHz, 60 MHz, and 66 MHz versions available
- ±250ps skew (max) between outputs
- 16-pin SOIC (300 mil) or 16-pin PDIP package
- Inputs and outputs are fully TTL-compatible
- CMOS process results in low power supply current
- High drive, 25mA outputs
- Low cost

The **ICS9175** is capable of producing half speed CPU clocks. Up to three of the six outputs can be configured as half speed CPU clocks. The skew matched circuitry matches rising edges of all CPU clocks and half speed clocks, guaranteeing low skew between outputs.

The **ICS9175** is fabricated using CMOS technology which results in much lower power consumption and cost compared with similar devices based on Gallium arsenide or BiCMOS technology. The typical operating current for the **ICS9175** is 35mA.

The frequencies in the **ICS9175** are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions such as those offered in this data sheet.

Block Diagram



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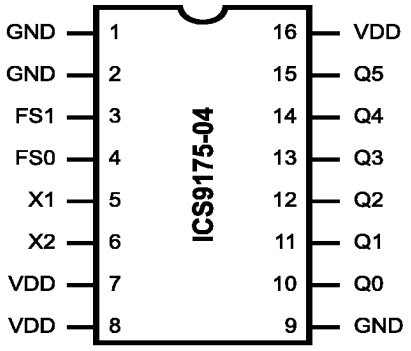
Pin Configuration



16-Pin SOIC or PDIP

Functionality Table for ICS9175-04

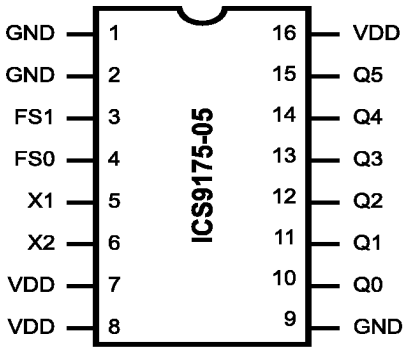
(using 14.318 MHz input)

FS1	FS0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
0	1	66	66	66	66	66	33
1	0	66	66	66	33	33	66
1	1	66	66	66	33	33	33

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND.
2	GND	-	GROUND.
3	SCLK1	Input	SCLK1 selects number of 1/2 speed clocks.
4	SCLK0	Input	SCLK0 selects number of 1/2speed clocks.
5	X1	Input	X1 crystal output.
6	X2	Input	X2 crystal output.
7	VDD	-	Power supply (+5V).
8	VDD	-	Power supply (+5V).
9	GND	-	GROUND.
10	Q0	Output	Q0 is a 66 MHz clock.
11	Q1	Output	Q1 is a 66 MHz clock.
12	Q2	Output	Q2 is a 66 MHz clock.
13	Q3	Output	Q3 can be 66 MHz or 33 MHz clock.
14	Q4	Output	Q4 can be 66 MHz or 33 MHz clock.
15	Q6	Output	Q5 can be 66 MHz or 33 MHz clock.
16	VDD	-	Power supply (+5V).

Pin Configuration



16-Pin SOIC or PDIP

Function Table for ICS9175-05

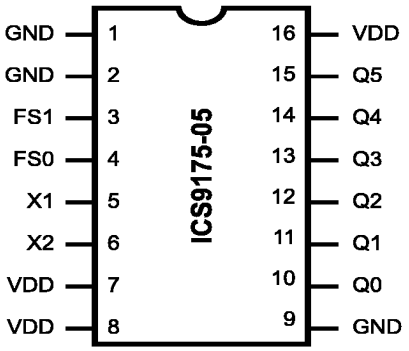
(using 14.318 MHz input)

FS1	FS0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	60	60	60	60	60	60
0	1	60	60	60	60	60	30
1	0	60	60	60	30	30	60
1	1	60	60	60	30	30	30

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND.
2	GND	-	GROUND.
3	SCLK1	Input	SCLK1 selects number of 1/2speed clocks.
4	SCLK0	Input	SCLK0 selects number of 1/2speed clocks.
5	X1	Input	X1 crystal output.
6	X2	Input	X2 crystal output.
7	VDD	-	Power supply (+5V).
8	VDD	-	Power supply (+5V).
9	GND	-	GROUND.
10	Q0	Output	Q0 is a 60 MHz clock.
11	Q1	Output	Q1 is a 60 MHz clock.
12	Q2	Output	Q2 is a 60 MHz clock.
13	Q3	Output	Q3 can be 60 MHz or 30 MHz clock.
14	Q4	Output	Q4 can be 60 MHz or 30 MHz clock.
15	Q6	Output	Q5 can be 60 MHz or 30 MHz clock.
16	VDD	-	Power supply (+5V).

Pin Configuration



16-Pin SOIC or PDIP

Functionality Table for ICS9175-06

(using 14.318 MHz input)

FS1	FS0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	52	52	52	52	52	52
0	1	52	52	52	52	52	26
1	0	52	52	52	26	26	52
1	1	52	52	52	26	26	26

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	GND	-	GROUND.
2	GND	-	GROUND.
3	SCLK1	Input	SCLK1 selects number of 1/2speed clocks.
4	SCLK0	Input	SCLK0 selects number of 1/2speed clocks.
5	X1	Input	X1 crystal output.
6	X2	Input	X2 crystal output.
7	VDD	-	Power supply (+5V).
8	VDD	-	Power supply (+5V).
9	GND	-	GROUND.
10	Q0	Output	Q0 is a 52 MHz clock.
11	Q1	Output	Q1 is a 52 MHz clock.
12	Q2	Output	Q2 is a 52 MHz clock.
13	Q3	Output	Q3 can be 52 MHz or 26 MHz clock.
14	Q4	Output	Q4 can be 52 MHz or 26 MHz clock.
15	Q5	Output	Q5 can be 52 MHz or 26 MHz clock.
16	VDD	-	Power supply (+5V).

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . . 0.5 Watts

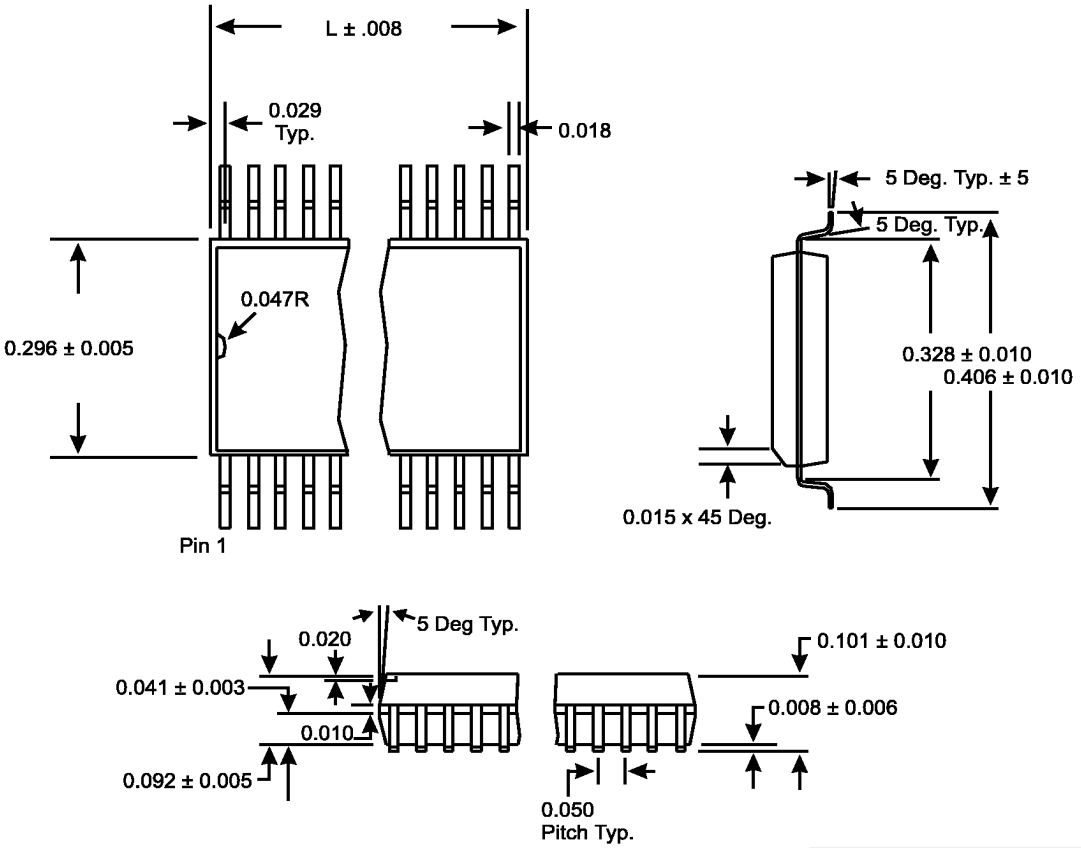
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} =+5V±5%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
InputLow Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-5	-	5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL}=25mA	-	0.5	0.8	V
Output High Voltage	V_{OH}	I_{OH}=-25mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded, SCLK=00	-	35	60	mA
AC Characteristics						
Output Rise time	t_r	15pF load; 0.8 to 2.0V	-	0.7	1	ns
Rise time	t_r	15pF load; 20% to 80%V	-	1.2	2	ns
Output Fall time	t_f	15pF load; 2.0 to 0.8V	-	0.7	1	ns
Fall time	t_f	15pF load; 80% to 20% V_{DD}	-	1.2	2	ns
Output Duty cycle	d_t	15pF load	45	49/51	55	%
Jitter, 1 sigma	T_{1s}		-	60	-	ps
Jitter, absolute	T_{abs}		-	±200	-	ps
Input Frequency	f_i	Note 1	-	14.318	-	MHz
Output Frequency	f_o		-	-	100	MHz
Skew between any 2 outputs at same frequency	t_{skew2}	Note 2, 4	-250	±50	250	ps
Skew between any 2 outputs at different frequencies		Note 2, 4	-	-	500	ps

Notes:
1. It may be possible to operate the **ICS9175** outside of these ranges. Consult ICS for your specific application.
2. All skew specifications are measured with a 50W transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.



LEAD COUNT	16L
DIMENSION L	0.404

SOIC Package (wide)

Ordering Information

ICS9175-04CW16 or ICS9175-05CW16 or ICS9175-06CW16 (SOIC)

Example:

ICS XXXX-PPP M X#W

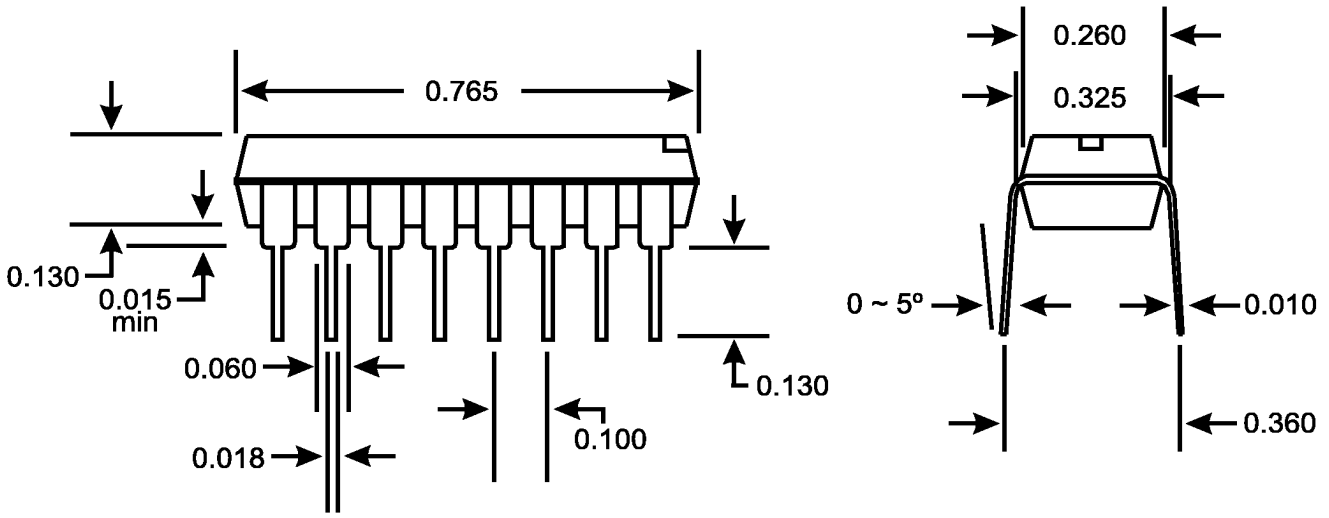
Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
W=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device



16-Pin DIP Package

Ordering Information

ICS9175-04CN16 or ICS9175-05CN16 or ICS9175-06CN16 (DIP)

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic#)

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device