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CYPRESS SEMICONDUCTOR
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ADVANCED INFORMATION

CY7C376

CYPRESS SEMICONDUCTOR

256-Macrocell Flash PLD

Features

- **256 macrocells in 16 logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - t_{PD} = 15 ns
  - t_S = 12 ns
  - t_{CO} = 12 ns
- **Electrically alterable Flash technology**
- **Available in 160-pin PGA and PQFP packages**
- **Pin compatible with the CY7C375**

Functional Description

The CY7C376 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C376 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

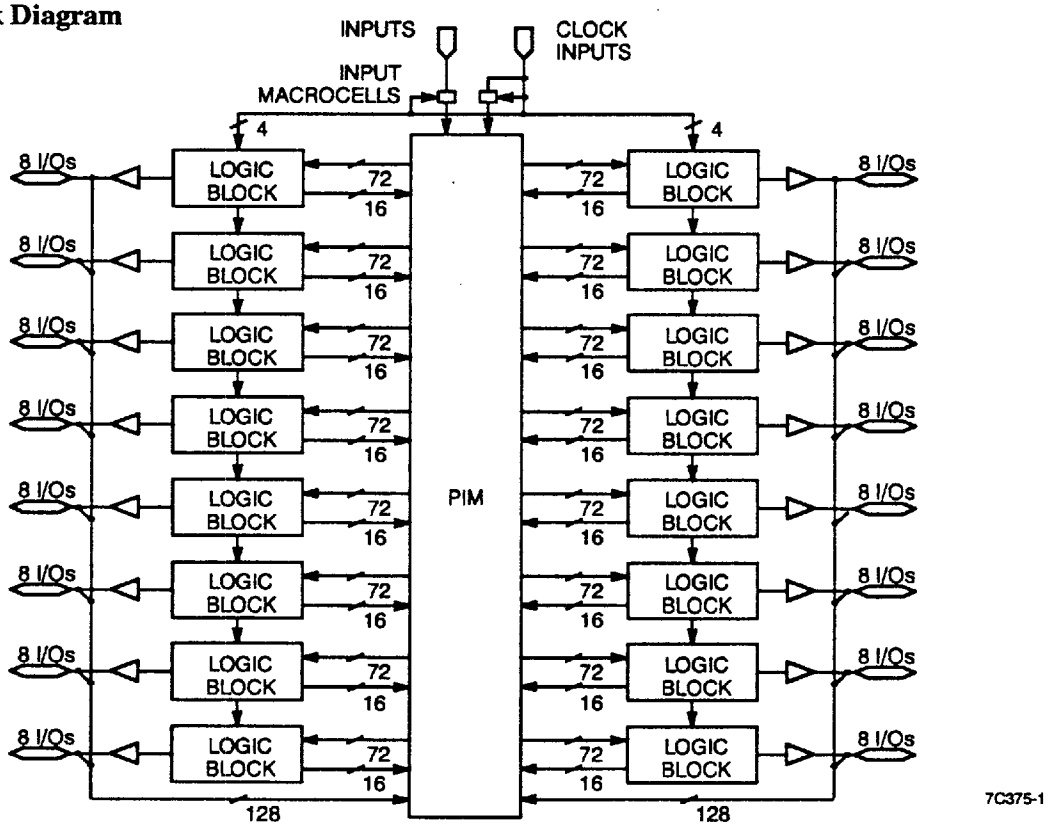
The 256 macrocells in the CY7C376 are divided between sixteen logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C376 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 128 I/O pins on the CY7C376. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C376 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C376 remain the same.

Logic Block Diagram



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