Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

AD8613/AD8617/AD8619

FEATURES

Offset voltage: 2.2 mV max
Low input bias current: 1 pA max
Single-supply operation: 1.8 V to 5 V
Low noise: 22 nV/√Hz
Micropower: 38 μA
No phase reversal
Unity gain stable

APPLICATIONS

Battery-powered instrumentation
Multipole filters
Current shunt sense
Sensors
ADC predrivers
DAC drivers/level shifters
Low power ASIC input or output amplifiers

GENERAL DESCRIPTION

The AD8613/AD8617/AD8619 are single, dual, and quad micropower, rail-to-rail input and output amplifiers that feature low supply current, low input voltage, and low current noise.

The parts are fully specified to operate from 1.8 V to 5.0 V single supply, or ±0.9 V and ±2.5 V dual supply. The combination of low noise, very low input bias currents, and low power consumption make the AD8613/AD8617/AD8619 especially useful in portable and loop-powered instrumentation.

The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power, single-supply systems.

The AD8613 is available in a 5-lead SC70 package and a 5-lead TSOT-23 package. The AD8617 is available in 8-lead MSOP and 8-lead SOIC packages. The AD8619 is available in 14-lead TSSOP and 14-lead SOIC packages.

PIN CONFIGURATIONS

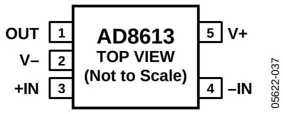

Figure 1. 5-Lead SC70 and 5-Lead TSOT-23

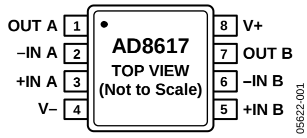

Figure 2. 8-Lead MSOP

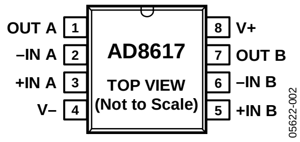

Figure 3. 8-Lead SOIC_N

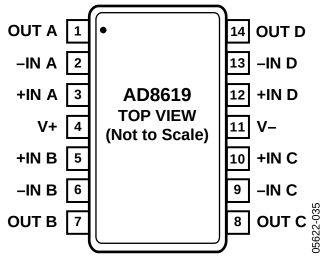

Figure 4. 14-Lead TSSOP

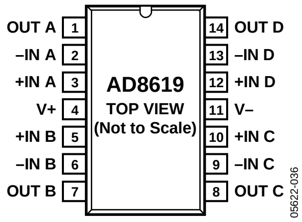

Figure 5. 14-Lead SOIC_N

Rev. B

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10/05—Rev. 0 to Rev. A

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9/05—Revision 0: Initial Version

SPECIFICATIONS

Electrical characteristics @ V_S = 5 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	−0.3 V < V_{CM} < +5.3 V		0.4	2.2	mV
		−40°C < T_A < +125°C, −0.3 V < V_{CM} < +5.2 V			2.2	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	4.5	μV/°C
AD8613				2.5	7.0	μV/°C
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +85°C			110	pA
		−40°C < T_A < +125°C			780	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			250	pA
Common-Mode Rejection Ratio	CMRR	0 V < V_{CM} < 5 V		95		dB
		−40°C < T_A < +125°C	68			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.5 V < V_O < 4.5 V	235	500		V/mV
Input Capacitance	C_{DIFF}			1.9		pF
	C_{CM}			2.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.95	4.98		V
		−40°C to +125°C	4.9			V
		I_L = 10 mA		4.7		V
		−40°C to +125°C	4.50			V
Output Voltage Low	V_{OL}	I_L = 1 mA		20	30	mV
		−40°C to +125°C			50	mV
		I_L = 10 mA		190	275	mV
		−40°C to +125°C			335	mV
Short-Circuit Current	I_{SC}			±80		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 10 kHz, A_V = 1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V < V_S < 5 V	67	94		dB
		−40°C < T_A < +125°C	64			dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2		38		μA
		−40°C <T_A < +125°C			50	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.1		V/μs
Settling Time 0.1%	t_S	G = ±1, 2 V step, C_L = 20 pF, R_L = 1 kΩ		23		μs
Gain Bandwidth Product	GBP	R_L = 100 kΩ		400		kHz
		R_L = 10 kΩ		350		kHz
Phase Margin	$Ø_O$	R_L = 10 kΩ, R_L = 100 kΩ, C_L = 20 pF		70		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise				2.3	3.5	μV
Voltage Noise Density	e_n	f = 1 kHz		25		nV/√Hz
		f = 10 kHz		22		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

Electrical characteristics @ V_S = 1.8 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	−0.3 V < V_{CM} < +1.9 V		0.4	2.2	mV
		−0.3 V < V_{CM} < +1.8 V; −40°C < T_A < +125°C			2.2	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	8.5	µV/°C
AD8613				3.7	9.0	µV/°C
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +85°C			110	pA
		−40°C < T_A < +125°C			780	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			250	pA
Common-Mode Rejection Ratio	CMRR	0 V < V_{CM} < 1.8 V	58	86		dB
		−40°C < T_A < +125°C	55			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.5 V < V_O < 1.3 V	85	1000		V/mV
Input Capacitance	C_{DIFF}			2.1		pF
	C_{CM}			3.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	1.65	1.73		V
		−40°C to +125°C	1.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		44	60	mV
		−40°C to +125°C			80	mV
Short-Circuit Current	I_{SC}			±7		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 10 kHz, A_V = 1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V < V_S < 5 V	67	94		dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2		38		µA
		−40°C < T_A < +125°C			50	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.1		V/µs
Settling Time 0.1%	t_S	G = ±1, 1 V step, C_L = 20 pF, R_L = 1 kΩ		6.5		µs
Gain Bandwidth Product	GBP	R_L = 100 kΩ		400		kHz
		R_L = 10 kΩ		350		kHz
Phase Margin	$Ø_O$	R_L = 10 kΩ, R_L = 100 kΩ, C_L = 20 pF		70		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise				2.3	3.5	µV
Voltage Noise Density	e_n	f = 1 kHz		25		nV/√Hz
		f = 10 kHz		22		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{SS} – 0.3 V to V_{DD} + 0.3 V
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND	Observe derating curve
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at 25°C, unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead TSOT-23 (UJ-5)	207	61	°C/W
5-Lead SC70 (KS-5)	376	126	°C/W
8-Lead MSOP (RM-8)	210	45	°C/W
8-Lead SOIC_N (R-8)	158	43	°C/W
14-Lead SOIC_N (R-14)	120	36	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{SY} = 5 V or ±2.5 V, unless otherwise noted.

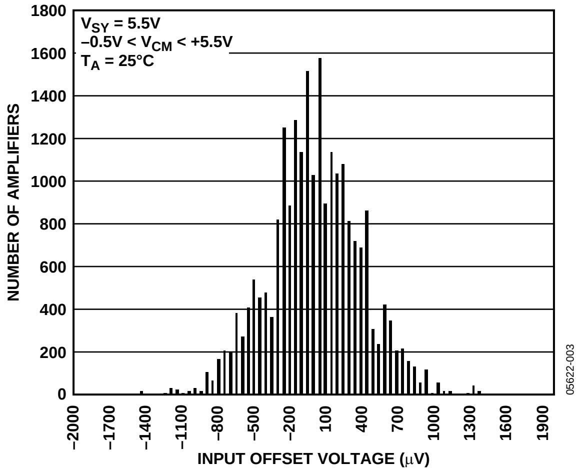

Figure 6. Input Offset Voltage Distribution

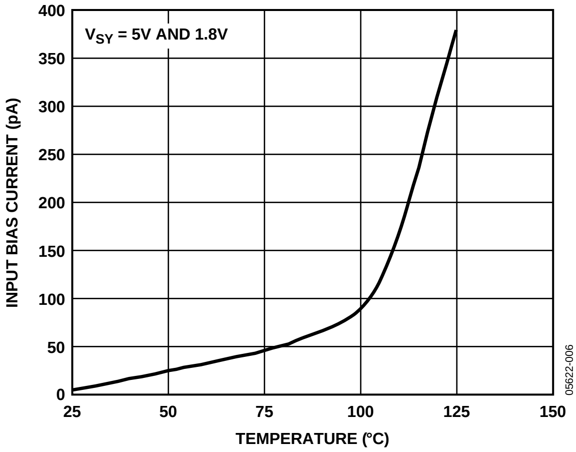

Figure 9. Input Bias Current vs. Temperature

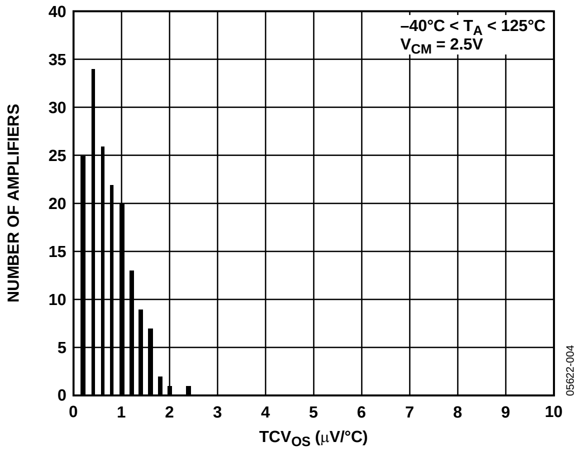

Figure 7. Input Offset Voltage Drift Distribution

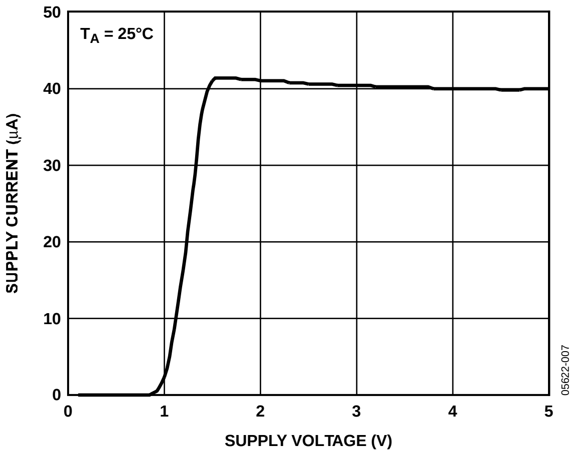

Figure 10. Supply Current vs. Supply Voltage

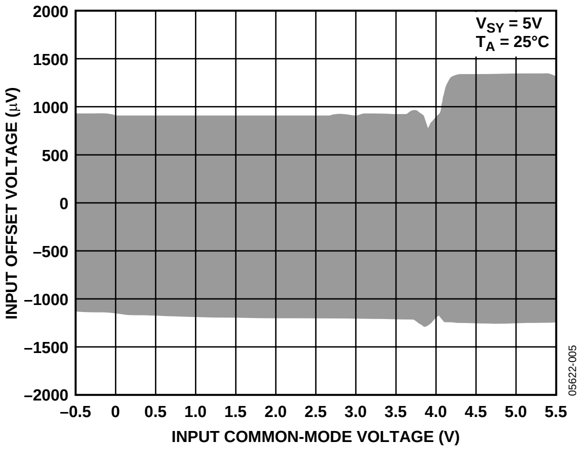

Figure 8. Input Offset Voltage vs. Input Common-Mode Voltage

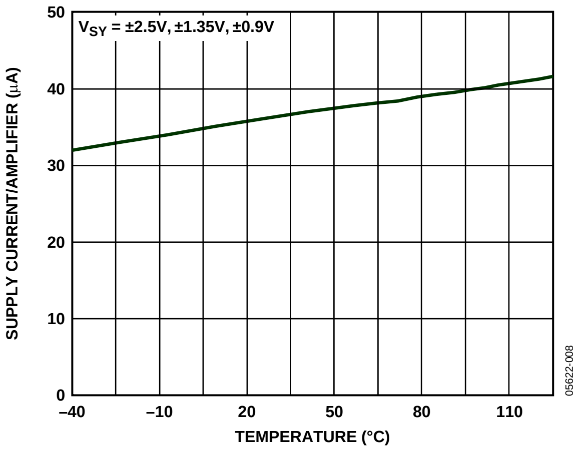

Figure 11. Supply Current vs. Temperature

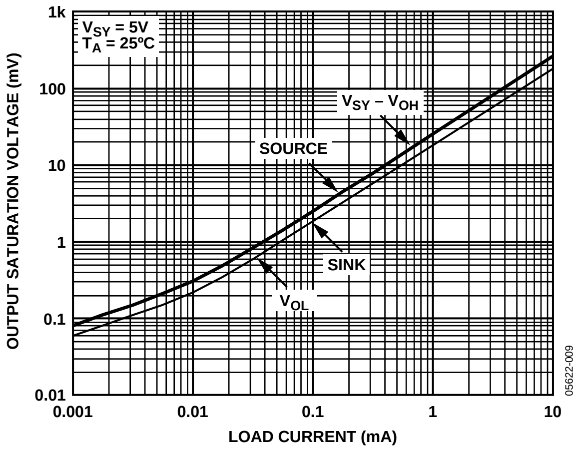

Figure 12. Output Saturation Voltage vs. Load Current

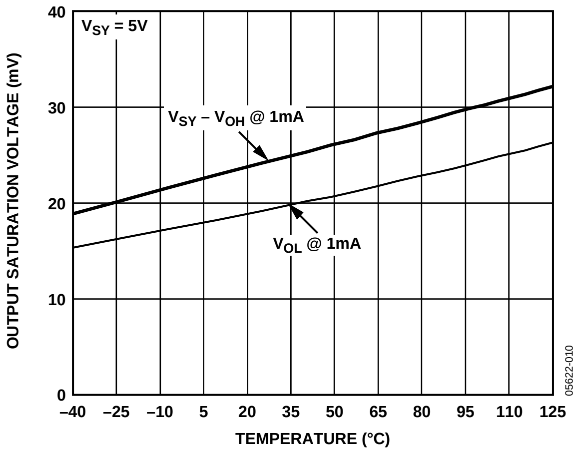

Figure 13. Output Saturation Voltage vs. Temperature (I_L = 1 mA)

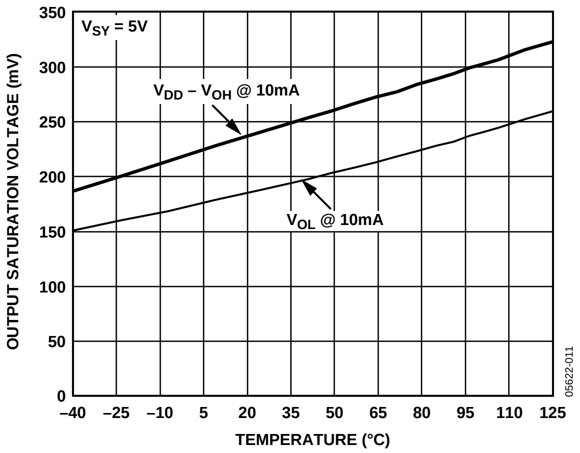

Figure 14. Output Saturation Voltage vs. Temperature (I_L = 10 mA)

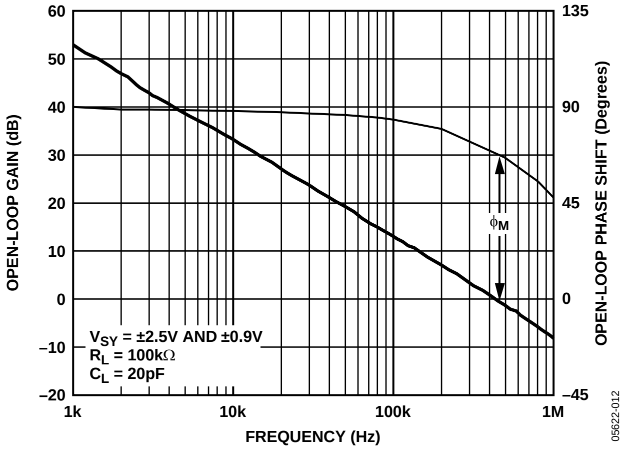

Figure 15. Open-Loop Gain and Phase vs. Frequency

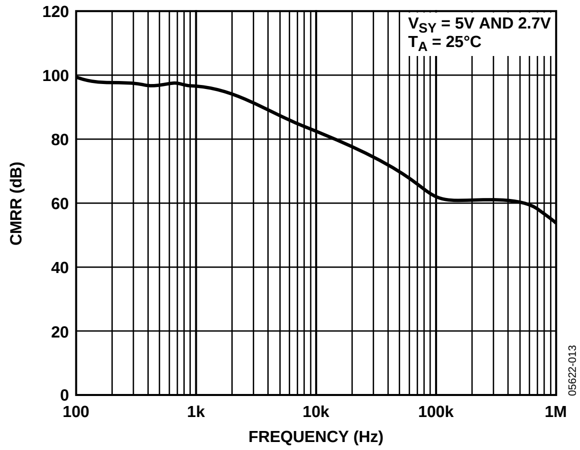

Figure 16. CMRR vs. Frequency

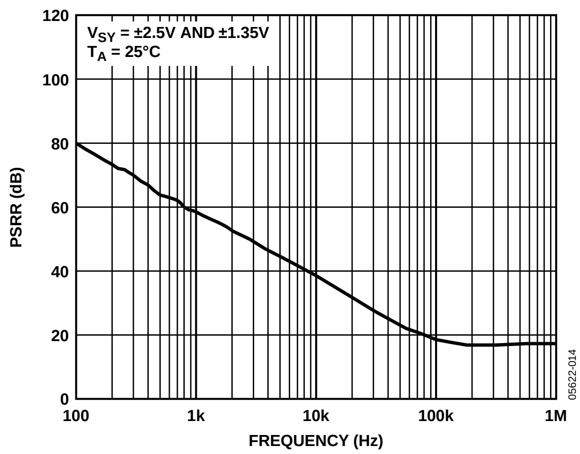

Figure 17. PSRR vs. Frequency

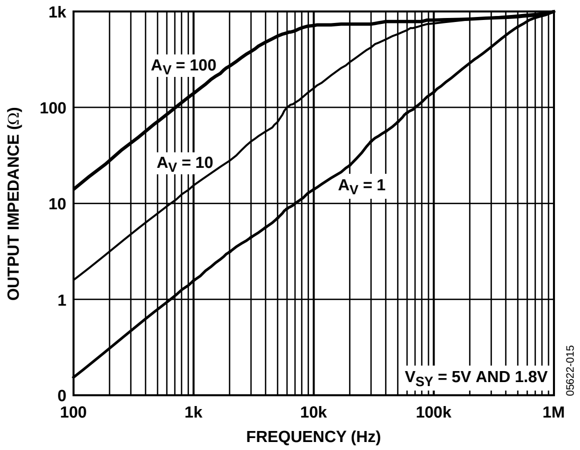

Figure 18. Closed-Loop Output Impedance vs. Frequency

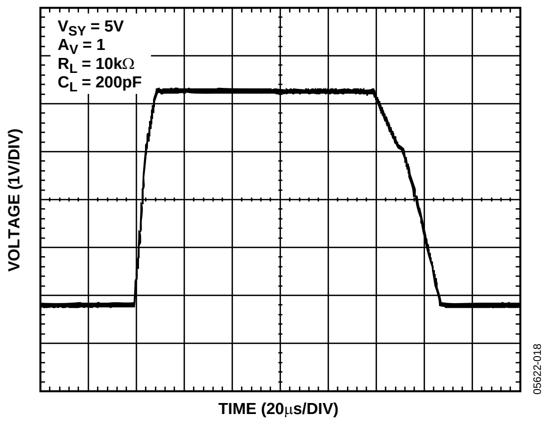

Figure 21. Large Signal Transient Response

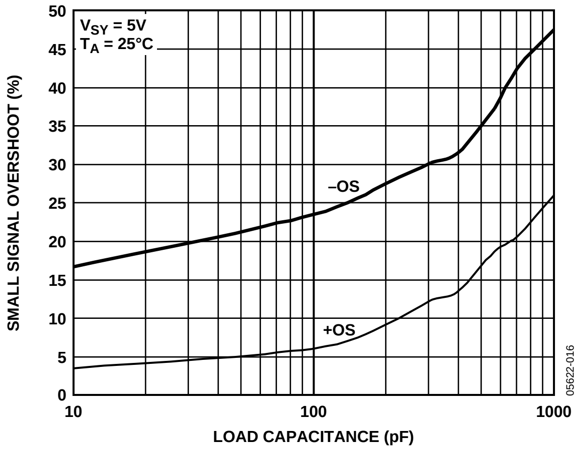

Figure 19. Small Signal Overshoot vs. Load Capacitance

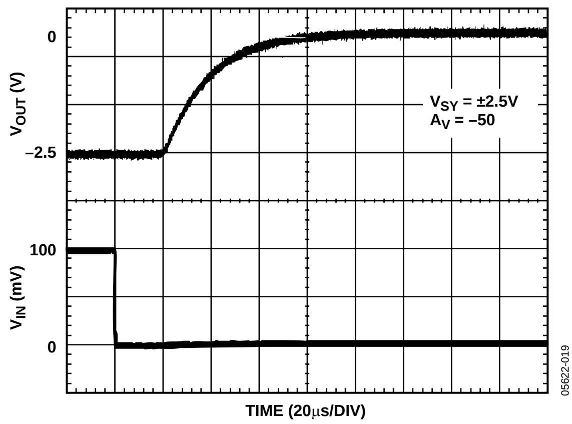

Figure 22. Positive Overload Recovery

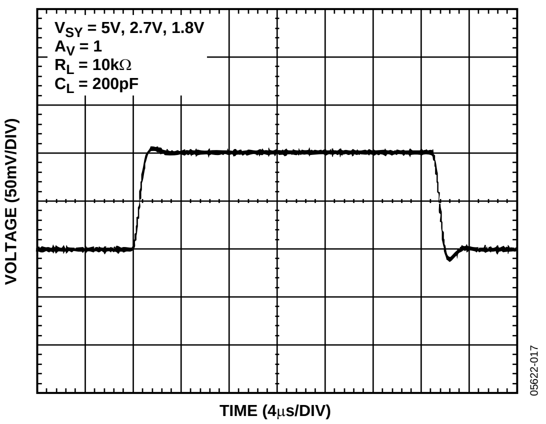

Figure 20. Small Signal Transient Response

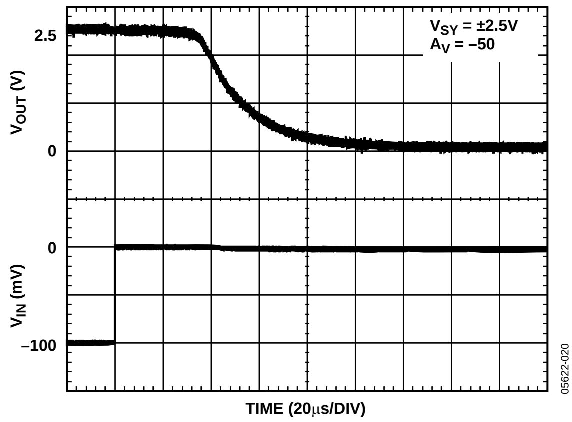

Figure 23. Negative Overload Recovery

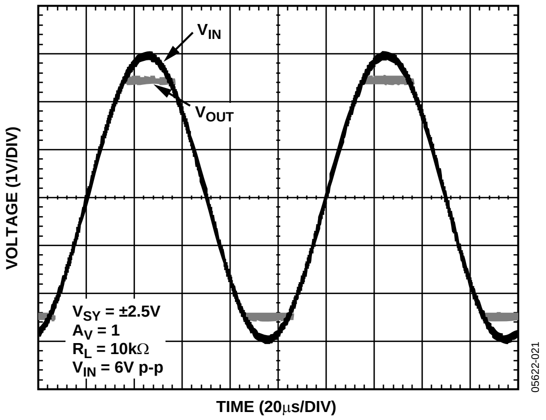

Figure 24. No Phase Reversal

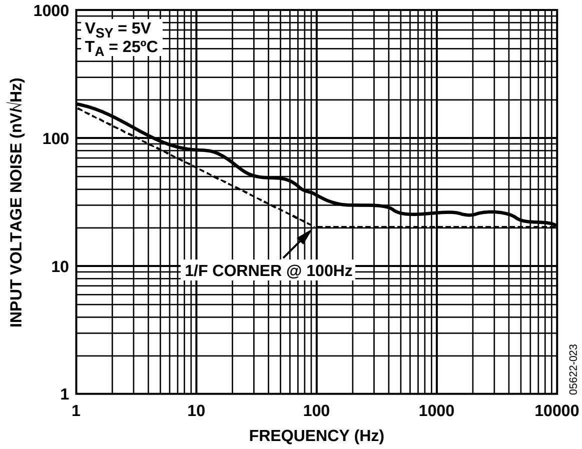

Figure 26. Voltage Noise Density

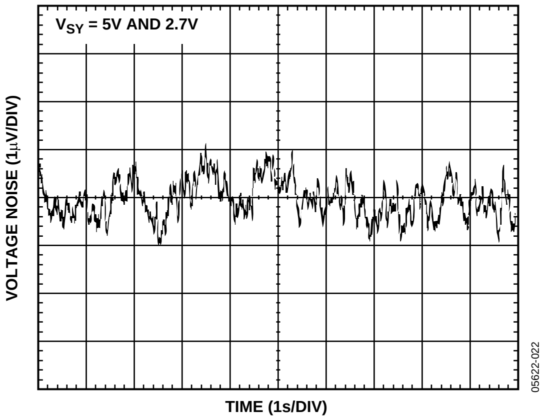

Figure 25. 0.1 Hz to 10 Hz Input Voltage Noise

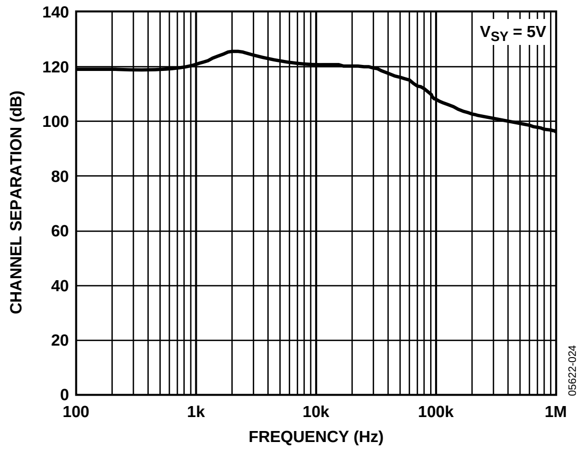

Figure 27. Channel Separation

V_S = 1.8 V or ±0.9 V, unless otherwise noted.

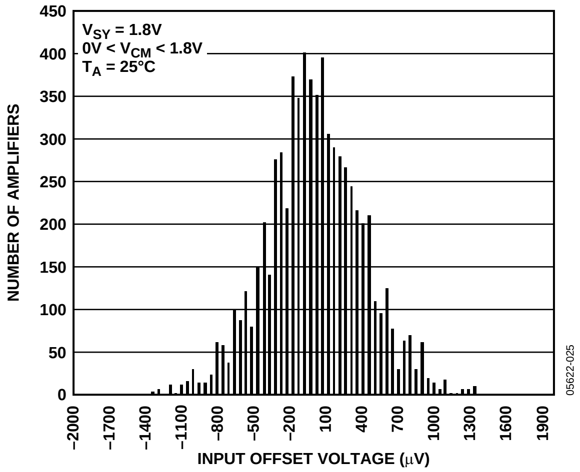

Figure 28. Input Offset Voltage Distribution

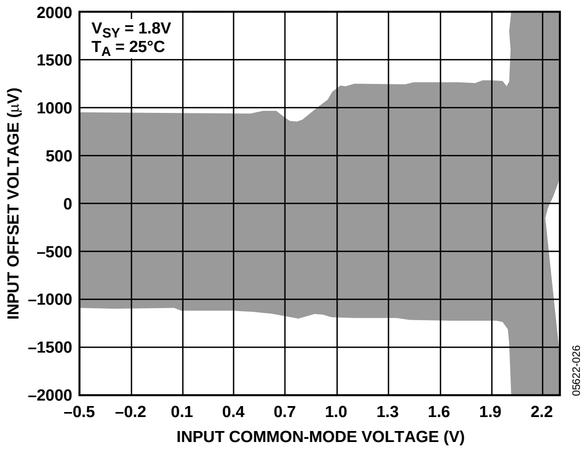

Figure 29. Input Offset Voltage vs. Input Common-Mode Voltage

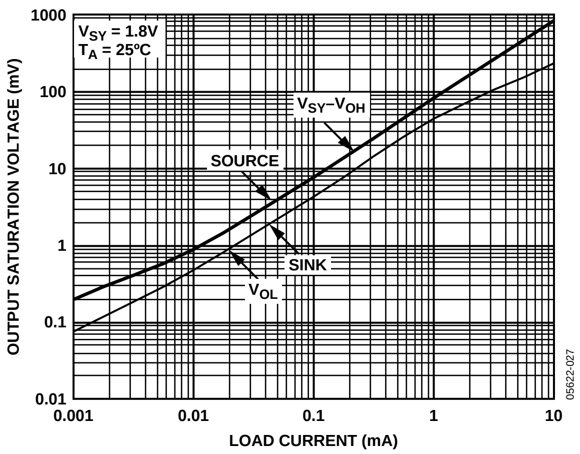

Figure 30. Output Saturation Voltage vs. Load Current

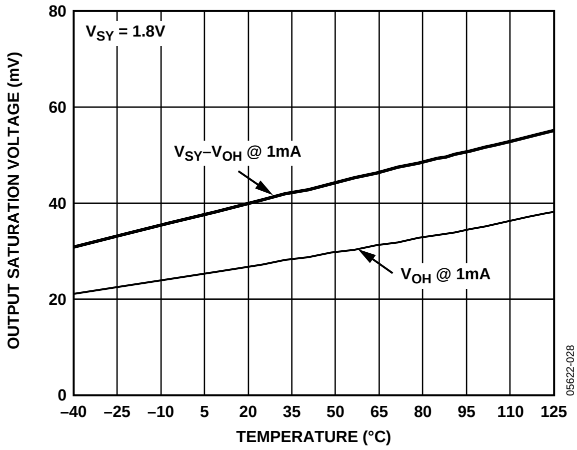

Figure 31. Output Saturation Voltage vs. Temperature (I_L = 1 mA)

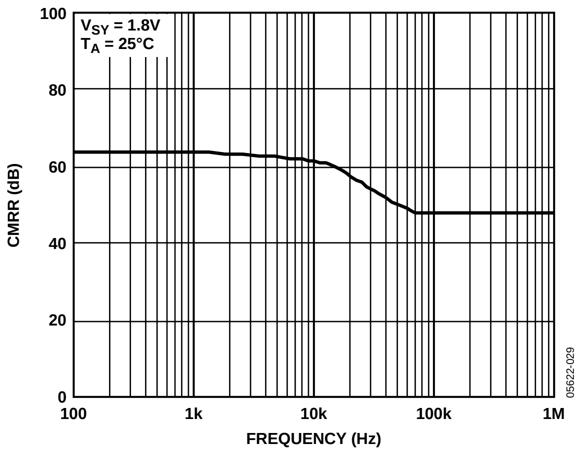

Figure 32. CMRR vs. Frequency

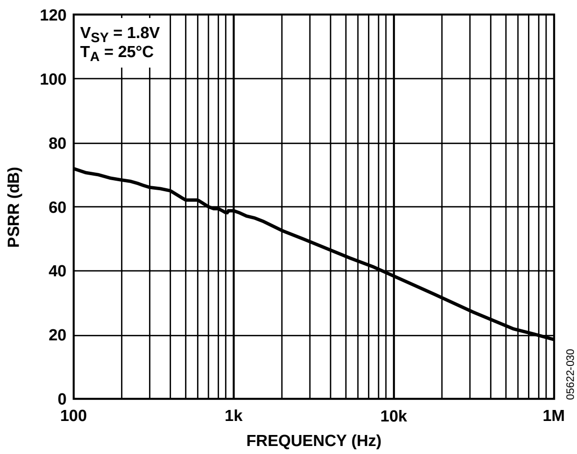

Figure 33. PSRR vs. Frequency

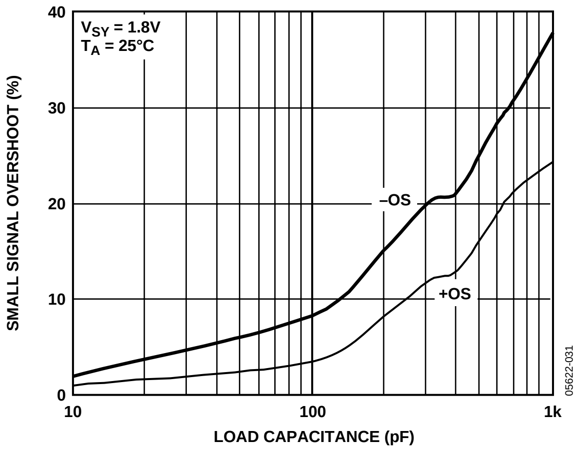

Figure 34. Small Signal Overshoot vs. Load Capacitance

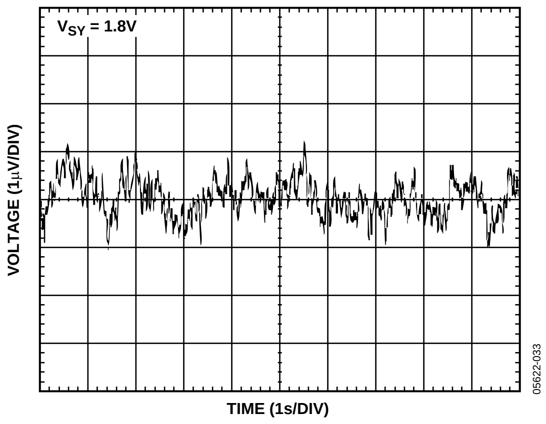

Figure 36. 0.1 Hz to 10 Hz Input Voltage Noise

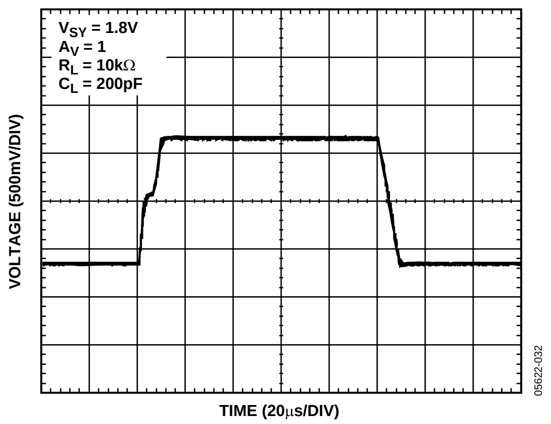

Figure 35. Large Signal Transient Response

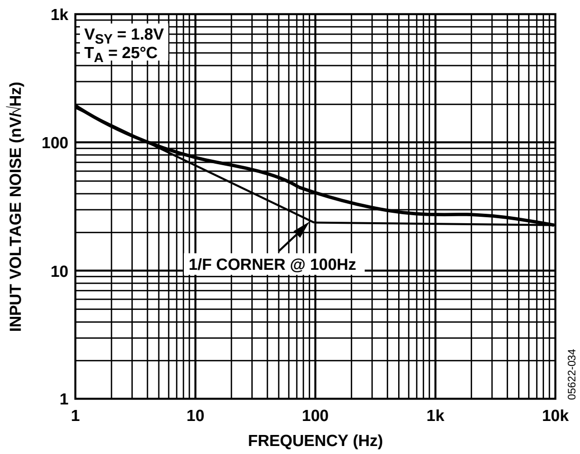

Figure 37. Voltage Noise Density

OUTLINE DIMENSIONS

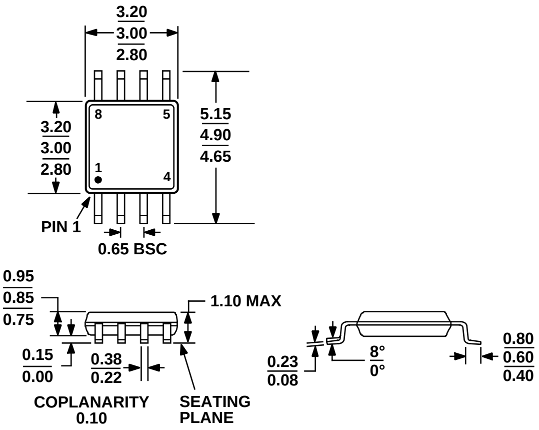

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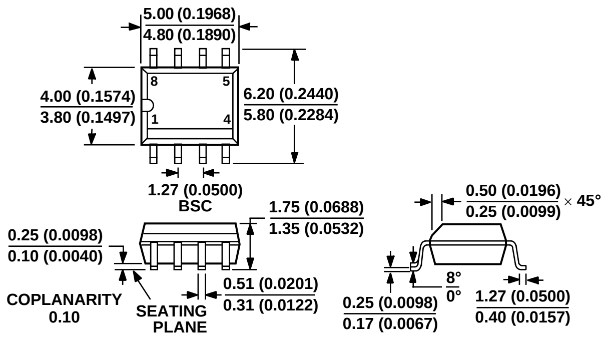
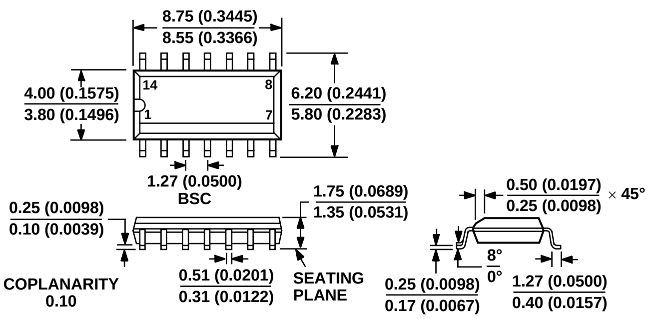
Figure 38. 8-Lead Mini Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

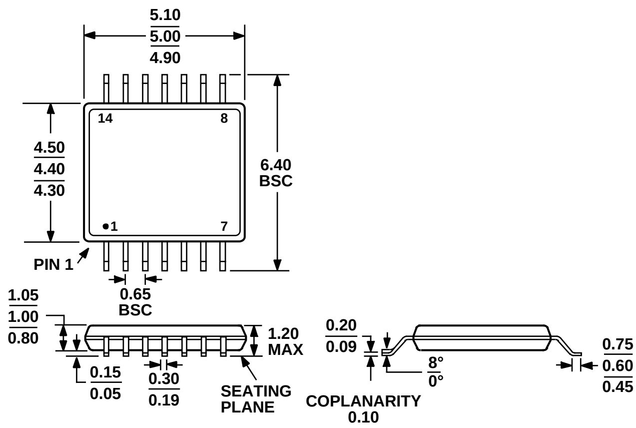
Figure 40. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8) Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB

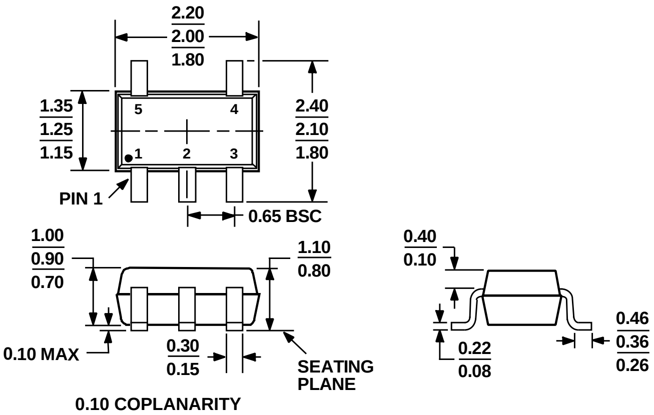
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14) Dimensions shown in millimeters and (inches)



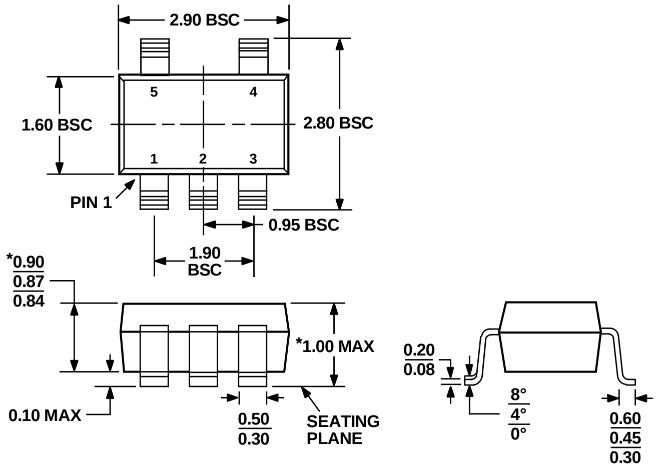
COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 41. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14) Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 42. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 43. 5-Lead Thin Small Outline Transistor Package [TSOT-23]
(UJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8613AKSZ-R2[1]	−40°C to +125°C	5-Lead SC70	KS-5	A0Y
AD8613AKSZ-REEL[1]	−40°C to +125°C	5-Lead SC70	KS-5	A0Y
AD8613AKSZ-REEL7[1]	−40°C to +125°C	5-Lead SC70	KS-5	A0Y
AD8613AUJZ-R2[1]	−40°C to +125°C	5-Lead TSOT-23	UJ-5	A0Y
AD8613AUJZ-REEL[1]	−40°C to +125°C	5-Lead TSOT-23	UJ-5	A0Y
AD8613AUJZ-REEL7[1]	−40°C to +125°C	5-Lead TSOT-23	UJ-5	A0Y
AD8617ARMZ-R2[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A0T
AD8617ARMZ-REEL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A0T
AD8617ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8617ARZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8617ARZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8619ARUZ[1]	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8619ARUZ-REEL[1]	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8619ARZ[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8619ARZ-REEL[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8619ARZ-REEL7[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	

[1] Z = Pb-free part.

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