REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
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SHEET	15	16	17																	
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-12-29

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, ERROR DETECTION AND CORRECTION CIRCUIT WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96711**

SHEET 1 OF 17

DESC FORM 193
JUL 94

<u>DISTRIBUTION STATEMENT A</u>. Approved for public release; distribution is unlimited.

5962-E169-96

9004708 0019515 660

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	F	96711	01	V	Y	C
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

__________ \\/ __________/
Drawing number

1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ACS630	Radiation hardened, SOS, advanced CMOS, error detection and correction circuit with three-state outputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28	28	Dual-in-line
Y	CDFP3-F28	28	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input current, any one input (I_{IN})	±10 mA
DC output current, any one output except DEF or SEF (I_{OUT})	±50 mA
DC output current, DEF or SEF output (I_{OUT})	±25 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case outline X	9°C/W
Case outline Y	10°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Case outline X	49°C/W
Case outline Y	65°C/W
Junction temperature (T_J)	+175°C
Maximum package power dissipation at T_A = +125°C (P_D): 4/	
Case outline X	1.0 W
Case outline Y	0.78 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	30% of V_{CC}
Minimum high level input voltage (V_{IH})	70% of V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum input rise and fall time at V_{CC} = 4.5 V (t_r, t_f)	10 ns/V
Radiation features:	
Total dose	> 3 x 10^5 Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold (LET) no upsets (see 4.4.4.4)	> 100 MeV/(cm^2/mg) 5/
Dose rate upset (20 ns pulse)	> 1 x 10^{11} Rads (Si)/s 5/
Latch-up	None 5/
Dose rate survivability	> 1 x 10^{12} Rads (Si)/s 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C unless otherwise noted.

4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on Θ_{JA}) at the following rate:

Case outline X	13.0 mW/°C
Case outline Y	8.4 mW/°C

5/ Guaranteed by design or process but not tested.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 3.

3.2.5 Irradiation test connections. The irradiation test connections shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
High level output voltage	V_{OH}	For all inputs affecting output under test V_{IN} = 3.15 V or 1.35 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All	4.5 V	1, 2, 3	4.40		V
		M, D, L, R, F 3/	All		1	4.40		
		For all inputs affecting output under test V_{IN} = 3.85 V or 1.65 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All	5.5 V	1, 2, 3	5.40		
		M, D, L, R, F 3/	All		1	5.40		
Low level output voltage	V_{OL}	For all inputs affecting output under test V_{IN} = 3.15 V or 1.35 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All	4.5 V	1, 2, 3		0.1	V
		M, D, L, R, F 3/	All		1		0.1	
		For all inputs affecting output under test V_{IN} = 3.85 V or 1.65 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All	5.5 V	1, 2, 3		0.1	
		M, D, L, R, F 3/	All		1		0.1	
Input current high	I_{IH}	For input under test, V_{IN} = 5.5 V For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		+0.5	µA
					2, 3		+5.0	
		M, D, L, R, F 3/	All		1		+5.0	
Input current low	I_{IL}	For input under test, V_{IN} = GND For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		-0.5	µA
					2, 3		-5.0	
		M, D, L, R, F 3/	All		1		-5.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Output current high (except DEF and SEF outputs) (Source)	I_{OH1} 4/	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = 4.1 V	All	4.5 V	1	-16.0		mA
					2, 3	-12.0		
		M, D, L, R, F 3/	All		1	-12.0		
Output current high (DEF and SEF outputs) (Source)	I_{OH2} 4/	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = 4.1 V	All	4.5 V	1	-8.0		mA
					2, 3	-6.0		
		M, D, L, R, F 3/	All		1	-6.0		
Output current low (except DEF and SEF outputs) (Sink)	I_{OL1} 4/	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = 0.4 V	All	4.5 V	1	16.0		mA
					2, 3	12.0		
		M, D, L, R, F 3/	All		1	12.0		
Output current low (DEF and SEF outputs) (Sink)	I_{OL2} 4/	For all inputs affecting output under test, V_{IN} = 4.5 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = 0.4 V	All	4.5 V	1	8.0		mA
					2, 3	6.0		
		M, D, L, R, F 3/	All		1	6.0		
Three-state output leakage current high	I_{OZH}	S0 = 0.0 V For all other inputs V_{IN} = 0.0 V or 5.5 V V_{OUT} = 5.5 V	All	5.5 V	1		+1.0	µA
					2, 3		+95.0	
		M, D, L, R, F 3/	All		1		+95.0	
Three-state output leakage current low	I_{OZL}	S0 = 0.0 V For all other inputs V_{IN} = 0.0 V or 5.5 V V_{OUT} = 0.0 V	All	5.5 V	1		-1.0	µA
					2, 3		-95.0	
		M, D, L, R, F 3/	All		1		-95.0	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	All	5.5 V	1		0.150	mA
					2, 3		3.0	
		M, D, L, R, F 3/	All		1		3.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Operation current, DBn to CBm	I_{OPER} 5/	V_{IH} = 5.0 V, V_{IL} = 0.0 V f = 1 MHz	All	5.0 V	4		6.4	mA
					5, 6		7.2	
Input capacitance	C_{IN}	V_{IH} = 5.0 V, V_{IL} = 0.0 V f = 1 MHz, see 4.4.1c	All	5.0 V	4		10	pF
Output capacitance	C_{OUT}		All	5.0 V	4		10	pF
Functional test	6/	V_{IH} = 3.15 V, V_{IL} = 1.35 V See 4.4.1b	All	4.5 V	7, 8	L	H	
		M, D, L, R, F 3/	All		7	L	H	
Propagation delay time, DBn to CBm	t_{PHL1} 7/	C_L = 50 pF R_L = 500Ω See figure 3	All	4.5 V	9	1.0	37.0	ns
					10, 11	1.0	37.0	
		M, D, L, R, F 3/	All		9	1.0	37.0	
	t_{PLH1} 7/	C_L = 50 pF R_L = 500Ω See figure 3	All	4.5 V	9	1.0	31.0	ns
					10, 11	1.0	34.0	
		M, D, L, R, F 3/	All		9	1.0	34.0	
Propagation delay time, S1 to DEF	t_{PLH2} 7/	C_L = 50 pF R_L = 500Ω See figure 3	All	4.5 V	9	1.0	18.0	ns
					10, 11	1.0	18.0	
		M, D, L, R, F 3/	All		9	1.0	18.0	
Propagation delay time, S1 to SEF	t_{PLH3} 7/	C_L = 50 pF R_L = 500Ω See figure 3	All	4.5 V	9	1.0	18.0	ns
					10, 11	1.0	18.0	
		M, D, L, R, F 3/	All		9	1.0	18.0	
Propagation delay time, output enable, S0 to DBn or CBm	t_{PZH} 7/	C_L = 50 pF R_L = 500Ω See figure 3	All	4.5 V	9	1.0	27.0	ns
					10, 11	1.0	29.0	
		M, D, L, R, F 3/	All		9	1.0	29.0	
	t_{PZL} 7/	C_L = 50 pF R_L = 500Ω See figure 3	All	4.5 V	9	1.0	23.0	ns
					10, 11	1.0	23.0	
		M, D, L, R, F 3/	All		9	1.0	23.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 2/		Unit
							Min	Max	
Propagation delay time, output disable, S0 to DBn or CBm	t_{PHZ} 7/	C_L = 50 pF R_L = 500Ω See figure 3		All	4.5 V	9	1.0	29.0	ns
						10, 11	1.0	29.0	
			M, D, L, R, F 3/	All		9	1.0	29.0	
	t_{PLZ} 7/	C_L = 50 pF R_L = 500Ω See figure 3		All	4.5 V	9	1.0	27.0	ns
						10, 11	1.0	27.0	
			M, D, L, R, F 3/	All		9	1.0	27.0	
Setup time, high or low, DBn or CBm to S1	t_s 5/	C_L = 50 pF R_L = 500Ω See figure 3		All	4.5 V	9	20.0		ns
						10, 11	20.0		
Hold time, high or low, DBn or CBm to S1	t_h 5/			All	4.5 V	9	10.0		ns
						10, 11	10.0		

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} test, the output terminals shall be open. When performing the I_{CC} test, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ Devices supplied to this drawing meet all levels M, D, L, R, and F of irradiation. However, this device is only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ Force/Measure functions may be interchanged.

5/ This parameter is guaranteed but not tested. This parameter is characterized upon initial design or process changes which affect this characteristic.

6/ The test vectors used to verify the truth tables shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth tables in figure 2 herein. For V_{OUT} measurements, $L \le 0.5$ V and $H \ge 4.0$ V.

7/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V. For propagation delay tests, all paths must be tested.

Device type	All		
Case outlines	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DEF	15	DB12
2	DB0	16	DB13
3	DB1	17	DB14
4	DB2	18	DB15
5	DB3	19	CB5
6	DB4	20	CB4
7	DB5	21	CB3
8	DB6	22	CB2
9	DB7	23	CB1
10	DB8	24	CB0
11	DB9	25	S0
12	DB10	26	S1
13	DB11	27	SEF
14	GND	28	V_{CC}

FIGURE 1. Terminal connections.

Check word generation

Check word bit	16-bit data word															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

NOTE: The six check bits are parity bits derived fron the matrix of data bits as indicated by "X" for each bit.

FIGURE 2. Truth tables.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-96711
		REVISION LEVEL	SHEET 9

Control functions

Memory cycle	Control		EDAC function	Data I/O	Check word	Error flags	
	S1	S0				SEF	DEF
Write	L	L	Generates check word	Input data	Output check word	L	L
Read	L	H	Read data and check word	Input data	Input check word	L	L
Read	H	H	Latch and flag error	Latch data	Latch check word	Enabled	Enabled
Read	H	L	Correct data word and generate syndrome bits	Output corrected data	Output syndrome bits	Enabled	Enabled

Error syndrome codes

Syndrome error code	Error locations																						
	DB																CB						No error
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Error functions

Total number of errors		Error flags		Data correction
16-bit data	6-bit check word	SEF	DEF	
0	0	L	L	Not applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

H = High voltage level
L = Low voltage level

FIGURE 2. Truth tables - Continued.

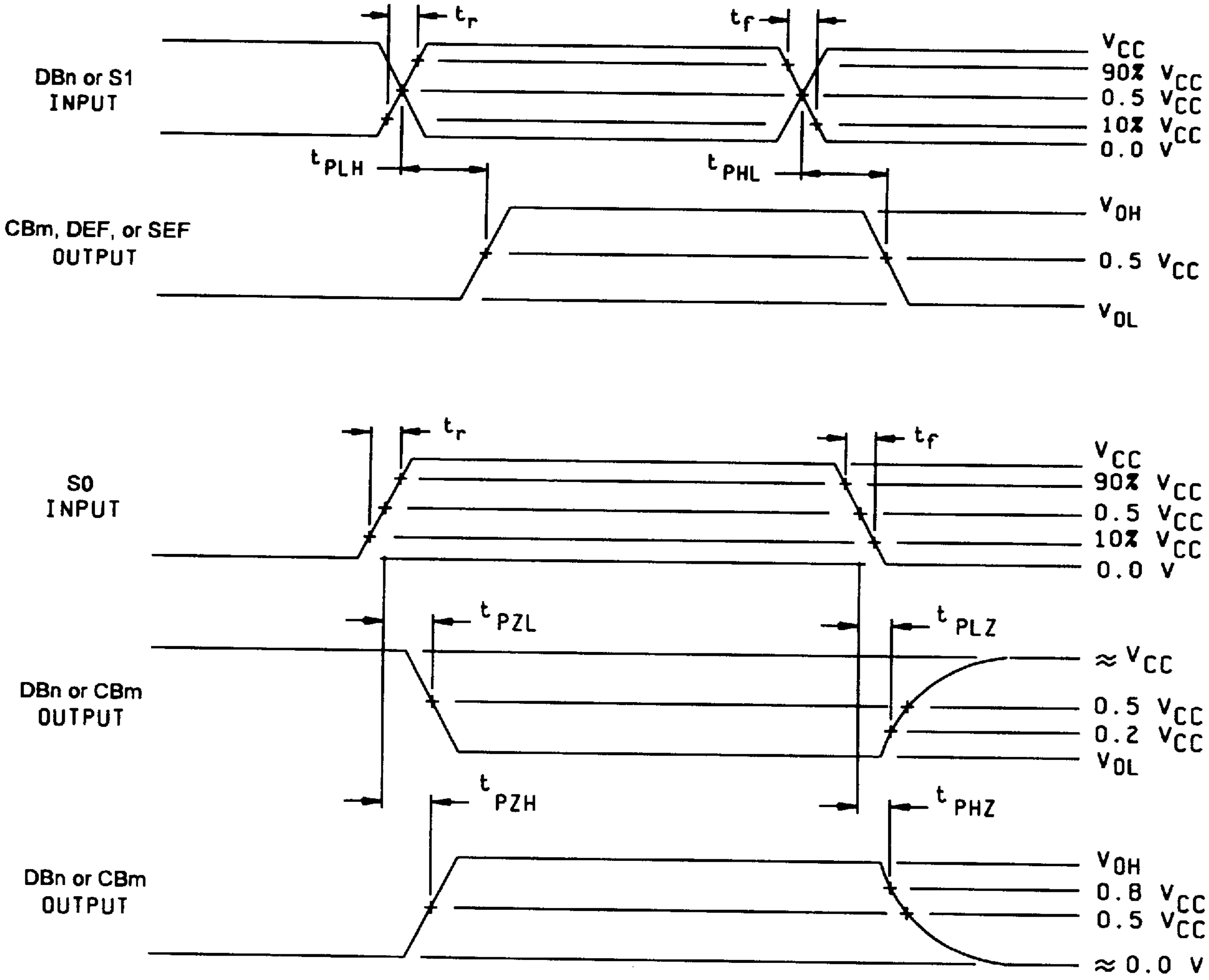
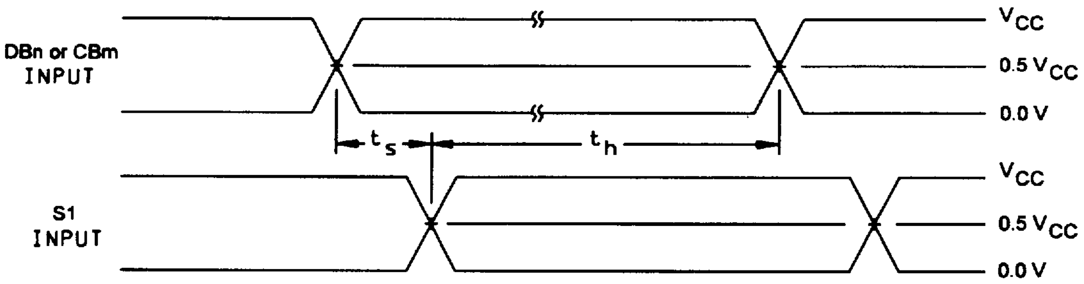
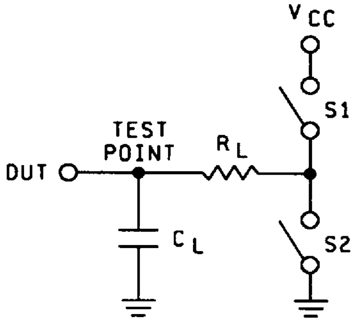


FIGURE 3. Switching waveforms and test circuit.





NOTES:

1. When measuring t_{PZL} and t_{PLZ}, S1 is closed and S2 is open.
2. When measuring t_{PLH}, t_{PHL}, t_{PZH}, and t_{PHZ}, S1 is open and S2 is closed.
3. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
4. R_L = 500Ω or equivalent.
5. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 10% V_{CC} to 90% V_{CC} and from 90% V_{CC} to 10% V_{CC}, respectively.

FIGURE 3. Switching waveforms and test circuit - Continued.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 39 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity (ESDS) qualification inspection. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 or as specified in QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth tables in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect these parameters. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{OUT}, tests shall be sufficient to validate the limits defined in table I herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, 9, and Δ's.
3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C).

Parameters 1/	Delta limits
I_{CC}	±30 µA
I_{OL}/I_{OH}	±15%
I_{OZL}/I_{OZH}	±200 nA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, test method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging testing. Accelerated aging testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535.

TABLE III. Irradiation test connections.

Open	Ground	V_{CC} = 5 V ±0.5 V
1, 27	14	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 28

NOTE: Each pin except V_{CC} and GND will have a resistor of 47 kΩ ±5% for irradiation testing.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

GND	Ground zero voltage potential.
I_{CC}	Quiescent supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
I_{OPER}	Operation current.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
C_{IN}	Input terminal-to-GND capacitance.
C_{OUT}	Output terminal-to-GND capacitance.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).