REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12												

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Chase Heusing

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 21 JULY 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, BIPOLAR, PROGRAMMABLE LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88515
A	67268	

SHEET 1 OF 12

DESC FORM 193
SEP 87

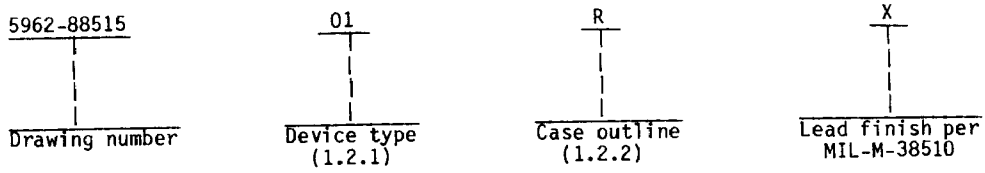
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E715

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	(See 6.4)	16-input, 8-output, combinatorial AND-OR-INVERT gate array
02	(See 6.4)	16-input, 8-output, 8-register AND-OR-INVERT gate array
03	(See 6.4)	16-input, 8-output, 6-register AND-OR-INVERT gate array
04	(See 6.4)	16-input, 8-output, 4-register AND-OR-INVERT gate array

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100" maximum), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc to +5.5 V dc
Off-state output voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	303 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R, S, and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA	1, 2, 3	All		-1.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V, I_{OH} = -1.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V, I_{OL} = 4.0 mA	1, 2, 3	All		0.5	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 2.4 V	1, 2, 3	All		25	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V	1, 2, 3	All		-0.25	mA
Input current	I_I	V_{CC} = 5.5 V, V_I = 5.5 V	1, 2, 3	All		1.0	mA
Output short circuit 1/ current	I_{OS}	V_{CC} = 5.0 V, V_O = 0 V	1, 2, 3	All	-30	-250	mA
Off-state output 2/ current	I_{OLZ}	V_{CC} = 5.5 V, V_O = 0.4 V	1, 2, 3	All		-100	µA
Off-state output 2/ current	I_{OHZ}	V_{CC} = 5.5 V, V_O = 2.4 V	1, 2, 3	All		100	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	All		55	mA
Propagation delay input or feedback to output	t_{PHL}	V_{CC} = 4.5 V to 5.5 V, V_{IL} = 0 V, V_{IH} = 3.0 V, C_L = 50 pF ±10%, R_1 = 800Ω, R_2 = 1.56 kΩ See figure 3	9,10,11	01,03, 04		50	ns
Propagation delay input or feedback to output	t_{PLH}		9,10,11	01,03, 04		50	ns
Propagation delay clock to output or feedback	t_{CLK}		9,10,11	02,03, 04		25	ns
Propagation delay high impedance to output high ($\overline{OE}$ to output enabled)	t_{PZH1}		9,10,11	02,03, 04		25	ns
Propagation delay high impedance to output low ($\overline{OE}$ to output enabled)	t_{PZL1}		9,10,11	02,03, 04		25	ns

See footnotes at end of table.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Propagation delay high impedance to output high	t_{PZH2}	V_{CC} = 4.5 V to 5.5 V, V_{IL} = 0 V, V_{IH} = 3.0 V, C_L = 50 pF ±10%, R_1 = 800Ω, R_2 = 1.56 kΩ See figure 3	9,10,11	01,03, 04		45	ns
Propagation delay high impedance to output low	t_{PZL2}		9,10,11	01,03, 04		45	ns
Propagation delay output high to high impedance ($\overline{OE}$ to output disabled)	t_{PHZ1}		9,10,11	02,03, 04		25	ns
Propagation delay output low to high impedance ($\overline{OE}$ to output disabled)	t_{PLZ1}		9,10,11	02,03, 04		25	ns
Propagation delay output high to high impedance	t_{PHZ2}		9,10,11	01,03, 04		45	ns
Propagation delay output low to high impedance	t_{PLZ2}		9,10,11	01,03, 04		45	ns
Clock pulse width, high	$t_{PW(H)}$		9,10,11	02,03, 04	25		ns
Clock pulse width, low	$t_{PW(L)}$		9,10,11	02,03, 04	25		ns
Hold time	t_H		9,10,11	02,03, 04	0		ns
Setup time	t_{SU}		9,10,11	02,03, 04	50		ns
Maximum clock frequency, data path register 3/	f_{MAX1}		9,10,11	02,03, 04 04	20		MHz
Maximum clock frequency, state machine 4/	f_{MAX2}		9,10,11	02,03, 04 04	13.3		MHz

1/ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

2/ I/O pin leakage is worst case of I_{OXZ} or I_{IX}; i.e., I_{IL} and I_{OHZ}.

3/ f_{MAX1} for a data path register is limited by the greater of the data setup time (t_{SU}) or the minimum clock period ($t_{PW(H)} + t_{PW(L)}$) and is guaranteed but not directly tested.

4/ f_{MAX2} for a state machine is guaranteed by $\frac{1}{t_{SU} + t_{CLK}}$ but not directly tested.

	Pin name			
Device	01	02	03	04
Package	R,S,2	R,S,2	R,S,2	R,S,2
Pin number				
1	I_0	CLOCK	CLOCK	CLOCK
2	I_1	I_0	I_0	I_0
3	I_2	I_1	I_1	I_1
4	I_3	I_2	I_2	I_2
5	I_4	I_3	I_3	I_3
6	I_5	I_4	I_4	I_4
7	I_6	I_5	I_5	I_5
8	I_7	I_6	I_6	I_6
9	I_8	I_7	I_7	I_7
10	GND	GND	GND	GND
11	I_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
12	O_0	O_0	I/O_0	I/O_0
13	I/O_1	O_1	O_1	I/O_1
14	I/O_2	O_2	O_2	O_2
15	I/O_3	O_3	O_3	O_3
16	I/O_4	O_4	O_4	O_4
17	I/O_5	O_5	O_5	O_5
18	I/O_6	O_6	O_6	I/O_6
19	O_7	O_7	I/O_7	I/O_7
20	V_{CC}	V_{CC}	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

☆U.S. GOVERNMENT PRINTING OFFICE: 1987 748-129 60913

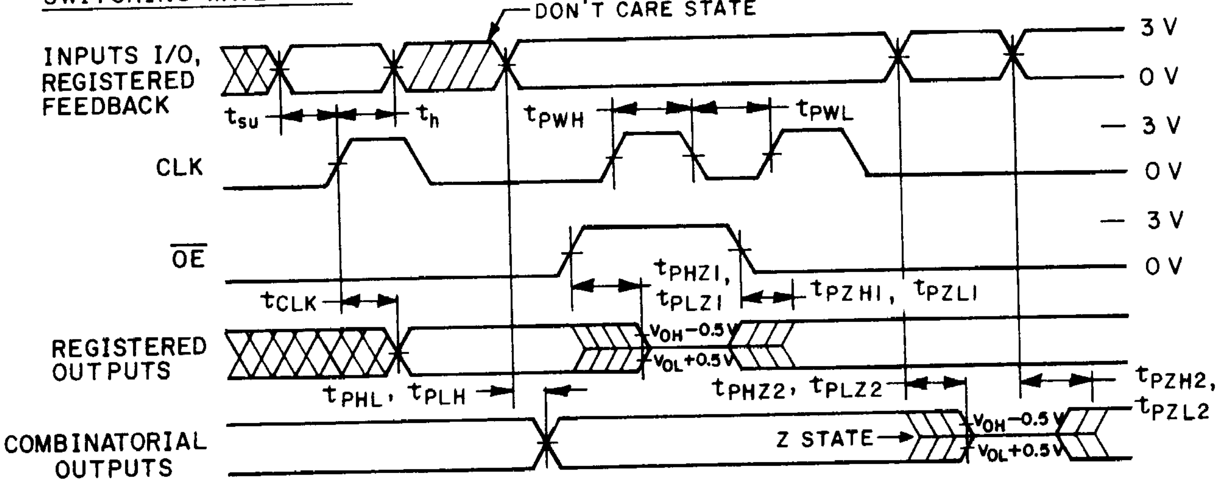
Device types 01 through 04 (see notes 1, 2, and 3)

Truth table																				
Address												Output level								
CLK	$\overline{OE}$	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	Device
		X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	01
CLK	L			X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	02
CLK	L			X	X	X	X	X	X	X	X	Z	H	H	H	H	H	H	Z	03
CLK	L			X	X	X	X	X	X	X	X	Z	Z	H	H	H	H	Z	Z	04

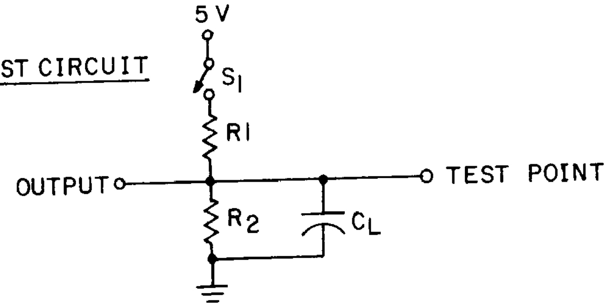
NOTES:
1. Z = 3-state.
2. Device types 02,03,04:
   Clock (pin 1) - low to high transition required to obtain valid data after last address transition.
3. Device types 02,03,04:
   Output enable (pin 11) - must be low to enable output.

FIGURE 2. Truth table (unprogrammed).

SWITCHING WAVEFORMS



TEST CIRCUIT



NOTES:
1. t_{PHL} and t_{PLH} are tested with switch S_1 closed. C_L = 50 pF and is measured at 1.5 V output level.
2. t_{PZH1}, t_{PZL1}, t_{PZH2}, and t_{PZL2} are measured at the 1.5 V level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PHZ1}, t_{PLZ1}, t_{PHZ2}, and t_{PLZ2} are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured V_{OH} -0.5 V output level. S_1 is closed for "0" to high impedance test measured to V_{OL} +0.5 V output level.
4. Equivalent test loads may be used on automatic test equipment.

FIGURE 3. Switching waveforms and test circuit.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88515
		REVISION LEVEL	SHEET 8

DESC FORM 193A
SEP 87

☆U.S. GOVERNMENT PRINTING OFFICE: 1987 748-129-60913

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11 group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test method 1005 of MIL-STD-883 conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedure shall be as specified by the device manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8

1/ (*) indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high speed testers.

3/ Subgroups 7 and 8 functional tests shall also verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8851501RX	50364	PAL16L8B-4MJ/883B	---
5962-8851501SX	50364	PAL16L8B-4MW/883B	---
5962-88515012X	50364	PAL16L8B-4ML/883B	---
5962-8851502RX	50364	PAL16R8B-4MJ/883B	---
5962-8851502SX	50364	PAL16R8B-4MW/883B	---
5962-88515022X	50364	PAL16R8B-4ML/883B	---
5962-8851503RX	50364	PAL16R6B-4MJ/883B	---
5962-8851503SX	50364	PAL16R6B-4MW/883B	---
5962-88515032X	50364	PAL16R6B-4ML/883B	---
5962-8851504RX	50364	PAL16R4B-4MJ/883B	---
5962-8851504SX	50364	PAL16R4B-4MW/883B	---
5962-88515042X	50364	PAL16R4B-4ML/883B	---

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Fusible link
50364	Monolithic Memories, Incorporated 2175 Mission College Boulevard Santa Clara, CA 95051	Titanium-Tungsten