DJB Device
Quad DS1 Dejitter Buffer
TXC-03351

DATA SHEET
Preliminary

FEATURES

- Reduces receive jitter on DS1 signals due to transmission and stuffing source jitter
- Dejitters four DS1 signals
- Satisfies Bellcore category I jitter requirements for DS1 signals
- Interfaces with DS1 line interface devices
- For use following a DS3 demux such as TranSwitch's M13 device
- Designed with digital signal processing techniques

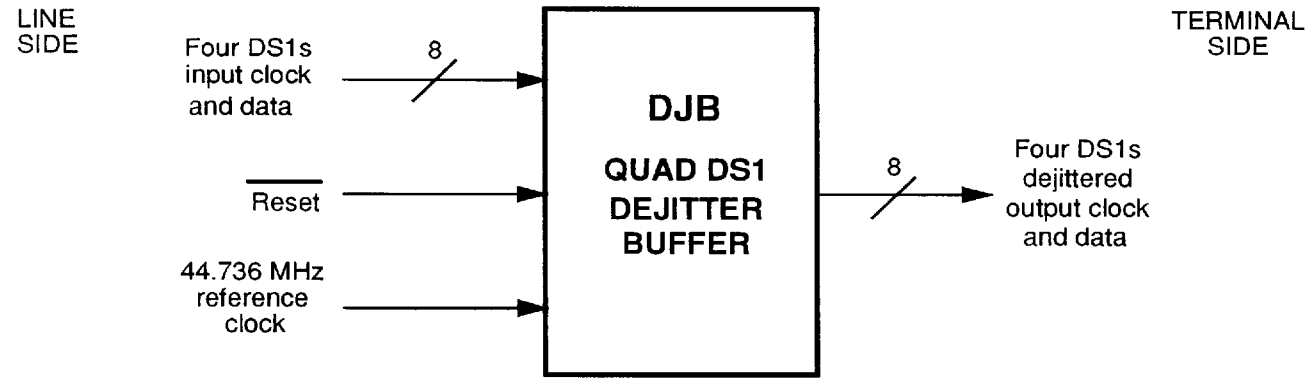
DESCRIPTION

The Quad DS1 Dejitter Buffer (DJB) is one of a family of related DS3/DS1 products from TranSwitch. The DJB performs jitter reduction on a DS1 signal when used in conjunction with a multiplexer (M13) device. Jitter occurs because the multiplexing process requires stuffing to compensate for differences in clock frequencies. In addition, noise, crosstalk, and clock recovery mechanisms in repeaters introduce timing jitter in DS1 signals. The DJB device uses a patented digital signal processing technique to reduce jitter caused by these sources.

The DJB is used primarily with TranSwitch's M13 device to dejitter four DS1 signals. It is normally connected between the four DS1 multiplex outputs and their line interface devices.

APPLICATIONS

- M13 multiplexer
- Add/drop multiplexer
- T1 add/drop test set



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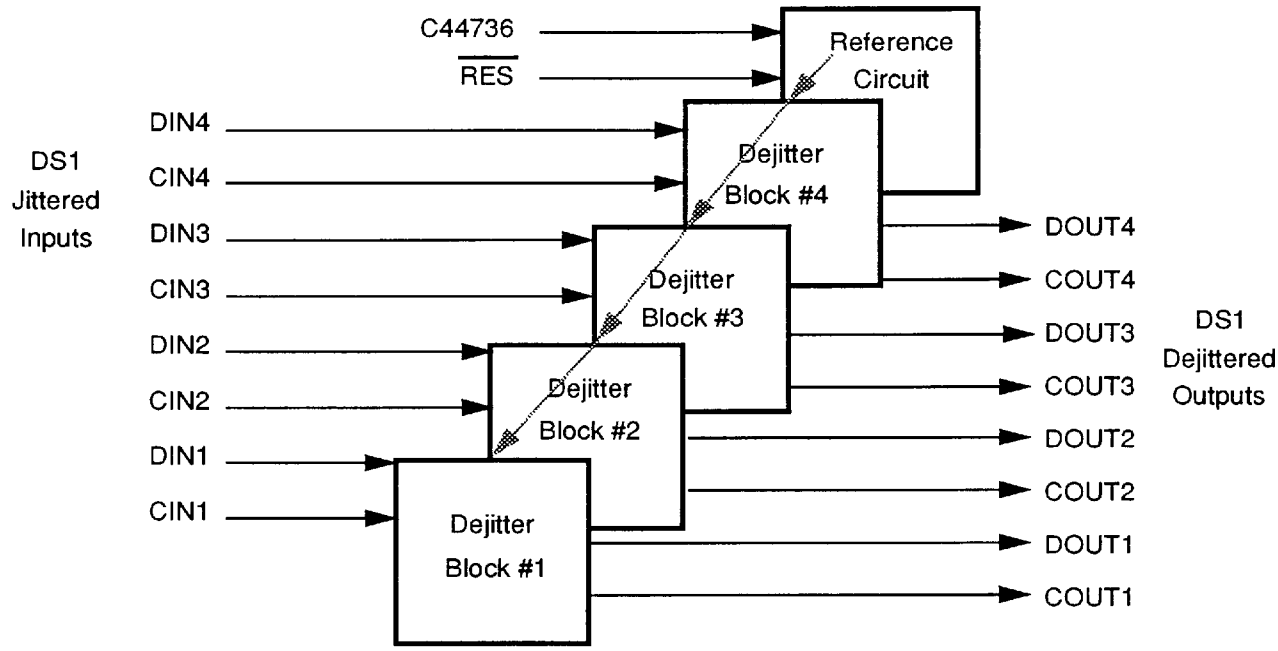


Figure 1. DJB Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 illustrates the block diagram of the DJB device. Each dejitter block contains a FIFO, programmable counters, and other digital logic circuits. The DS3 input clock (C44736) provides a clock source for deriving the clock for the DS1 outputs. The DJB uses a digital arithmetic unit to divide the input reference clock by a variable rate which depends on the state of the FIFO in each of the dejitter functional blocks.

The FIFO in each block does not fill at a constant rate. A divisor is set up for each block to clock the data out of the FIFO; it can alter the length of one DS1 frame (193 bits) by +/-22.35 nanoseconds. The number of bits in the FIFO determines if the length of the DS1 frame is changed.

The reference clock and any of the four dejitter functional blocks allow the DS1 input frequency to range over +/- 130 ppm from the standard 1.544 MHz rate. The actual "pull range" is 158 ppm allowing for +/- 20 ppm for the DS3 clock.

The FIFOs and counters in the DJB are reset by placing an active low on the $\overline{\text{RES}}$ lead. The reset lead must be held low for at least one DS1 clock cycle for each Dejitter Block after power becomes stable.

PIN DIAGRAM

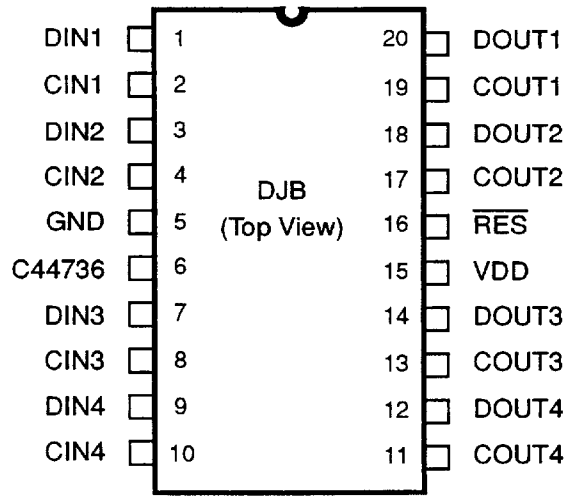


Figure 2. DJB Pin Diagram With Numbers and Names

PIN DESCRIPTIONS

Symbol	Pin No.	I/O/P*	Type	Name/Function
DIN1	1	I	TTL	Data Input Number 1
CIN1	2	I	TTL	Clock Input for DIN1
DIN2	3	I	TTL	Data Input Number 2
CIN2	4	I	TTL	Clock Input for DIN2
GND	5	P	--	V_{SS} or Ground
C44736	6	I	TTL	DS3 reference clock, +/- 20 ppm
DIN3	7	I	TTL	Data Input Number 3
CIN3	8	I	TTL	Clock Input for DIN3
DIN4	9	I	TTL	Data Input Number 4
CIN4	10	I	TTL	Clock Input for DIN4
COUT4	11	O	TTL4mA	Clock Output for DOUT4
DOUT4	12	O	TTL4mA	Data Output Number 4
COUT3	13	O	TTL4mA	Clock Output for DOUT3
DOUT3	14	O	TTL4mA	Data Output Number 3
VDD	15	P	--	5-volt Supply Voltage, +/-5%
$\overline{RES}$	16	I	TTLp	Reset Active Low to Initialize DJB
COUT2	17	O	TTL4mA	Clock Output for DOUT2
DOUT2	18	O	TTL4mA	Data Output Number 2
COUT1	19	O	TTL4mA	Clock Output for DOUT1
DOUT1	20	O	TTL4mA	Data Output Number 1

*Note: I = Input; O = Output; P = Power

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		116	mW
Ambient operating temperature	T_A	-40	85	°C
Operating junction temperature	T_J		150	°C
Storage temperature range	T_S	-55	150	°C

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal res - junc to ambient			TBD	°C/W	
Thermal res - junc to case		TBD		°C/W	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5	5.25	V	
I_{DD}			22	mA	
P_{DD}			116	mW	Input switching

INPUT AND OUTPUT PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 9K (nominal) internal pull-up resistor.

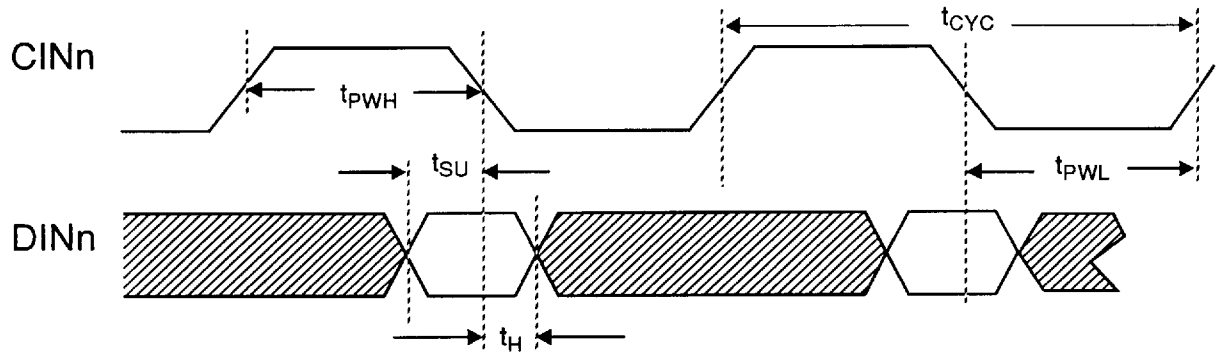
Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$ mA
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	$C_{LOAD} = 15$ pF
t_{FALL}	1.3	2.3	3.4	ns	$C_{LOAD} = 15$ pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the DJB are illustrated in Figures 3 through 6, with values of the timing intervals following each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

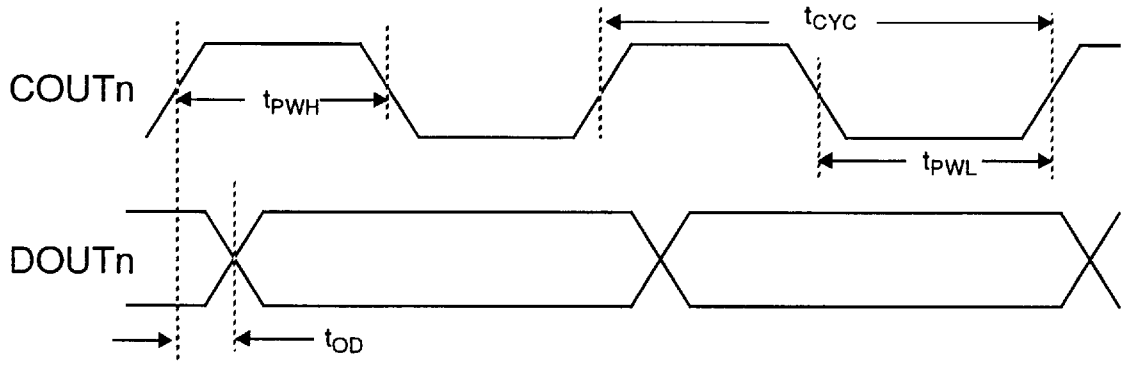
Figure 3. DJB Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
CIN clock period	t_{CYC}		1.544*		MHz
CIN high time	t_{PWH}	300			ns
CIN low time	t_{PWL}	300			ns
DIN set-up time to CIN ↓	t_{SU}	30			ns
DIN hold time after CIN ↓	t_H	25			ns

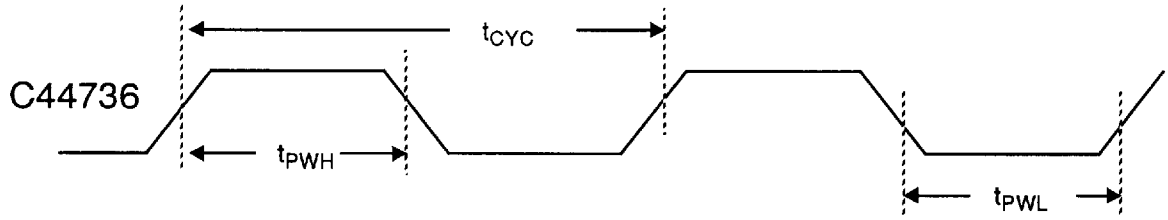
*The nominal frequency of DS1 is 1.544 MHz and the limits on this frequency are ± 158 ppm for proper operation of the DJB, assuming the reference clock (C44736) limit is ± 20 ppm.

Figure 4. DJB Output Timing



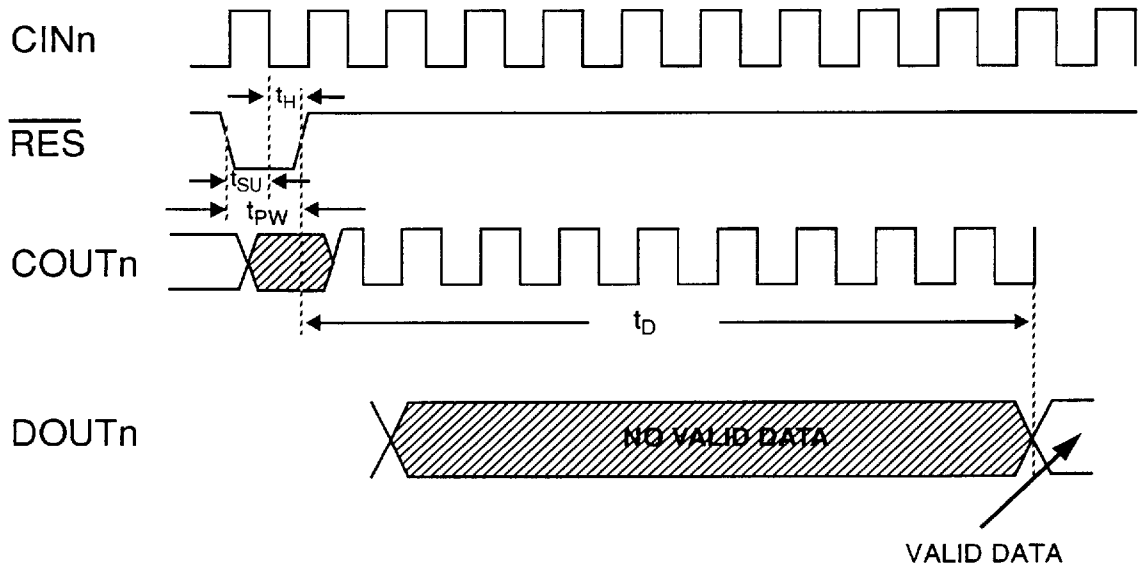
Parameter	Symbol	Min	Typ	Max	Unit
COUT clock period	t_{CYC}	620	647.66	675	ns
COUT high time	t_{PWH}	300			ns
COUT low time	t_{PWL}	300			ns
DOUT output delay after COUT ↑	t_{OD}			100	ns

Figure 5. DJB Reference Clock



Parameter	Symbol	Min	Typ	Max	Unit
C44736 clock period	t_{CYC}		22.35		ns
C44736 high time	t_{PWH}	9			ns
C44736 low time	t_{PWL}	9			ns

Figure 6. DJB Reset Timing



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Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RES}$ set-up time to CIN ↓	t_{SU}	30			ns
$\overline{RES}$ hold time after CIN ↓	t_H	25			ns
$\overline{RES}$ pulse width	t_{PW}	55			ns
DOUT delay after $\overline{RES}$ ↑	t_D			5.4	µsec

PACKAGING

The DJB device is packaged in a plastic 20-pin DIP leaded chip carrier. All dimensions shown are in inches, and are nominal unless otherwise noted.

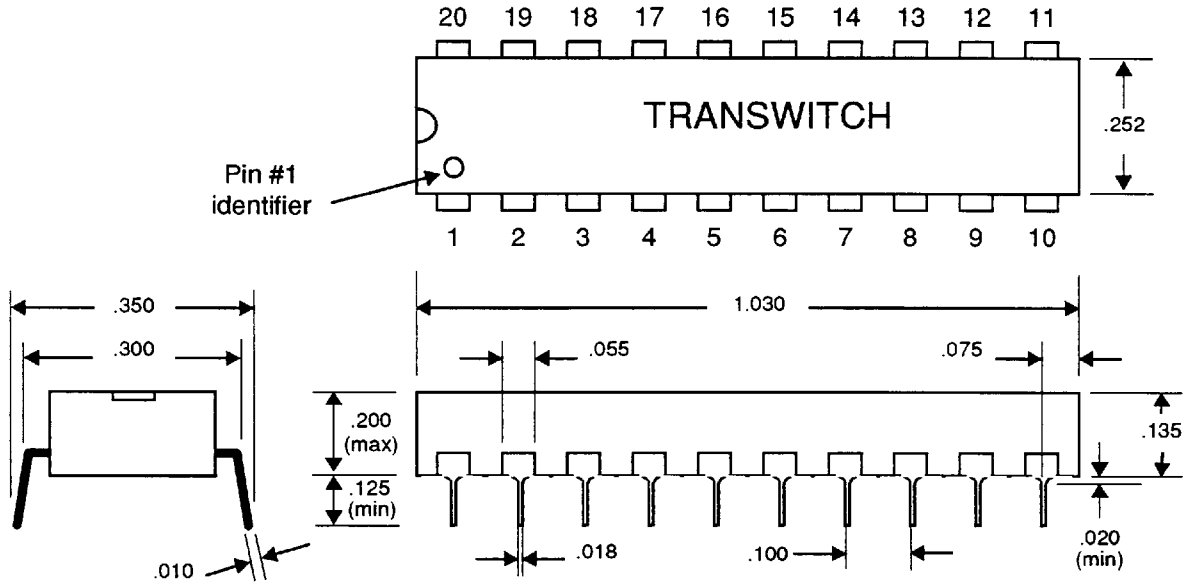

Figure 7. DJB Plastic 20-Pin DIP

ORDERING INFORMATION

Part Number:	TXC-03351-AIPD	Plastic 20-pin DIP leaded chip carrier
	TXC-03351-AIPD/B	Plastic 20-pin DIP leaded chip carrier with 96-hour burn-in at 125°C

RELATED PRODUCT

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-21002, M13 Evaluation Board. A complete, ready-to-use single-board test system that demonstrates the functions and features of the M13 and DJB VLSI devices.