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PRELIMINARY

LH511000UL

CMOS 1M (128K × 8) Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 330 mW (MAX.)
  Standby at T_A = 0 to 70°C
  22 µW (MAX.)
- Wide temperature range
  -40 to +85°C
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH511000UL is a 1M bit static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

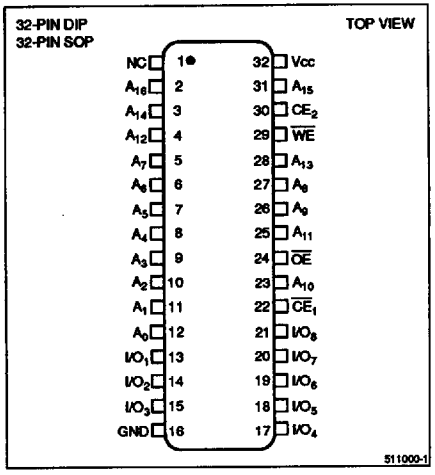

Figure 1. Pin Connections for DIP and SOP Packages

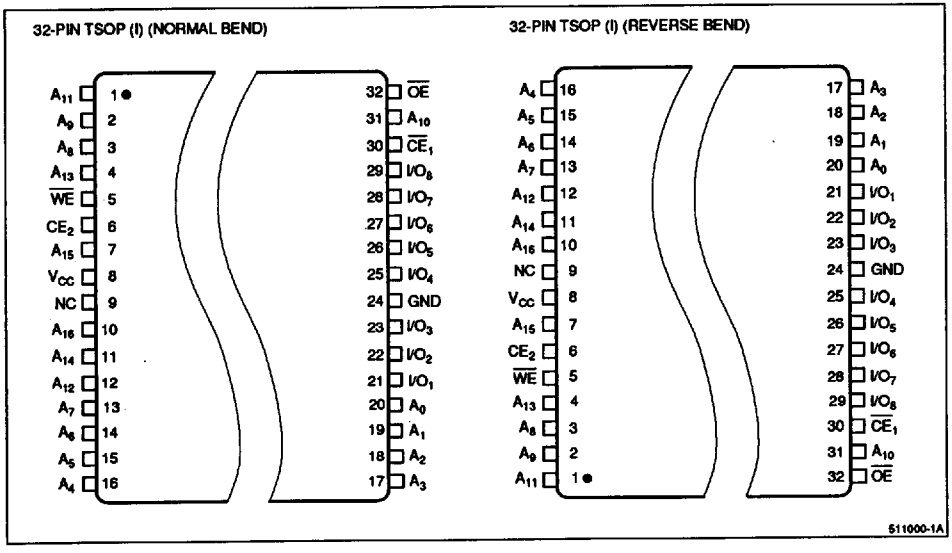

Figure 2. Pin Connections for TSOP Packages

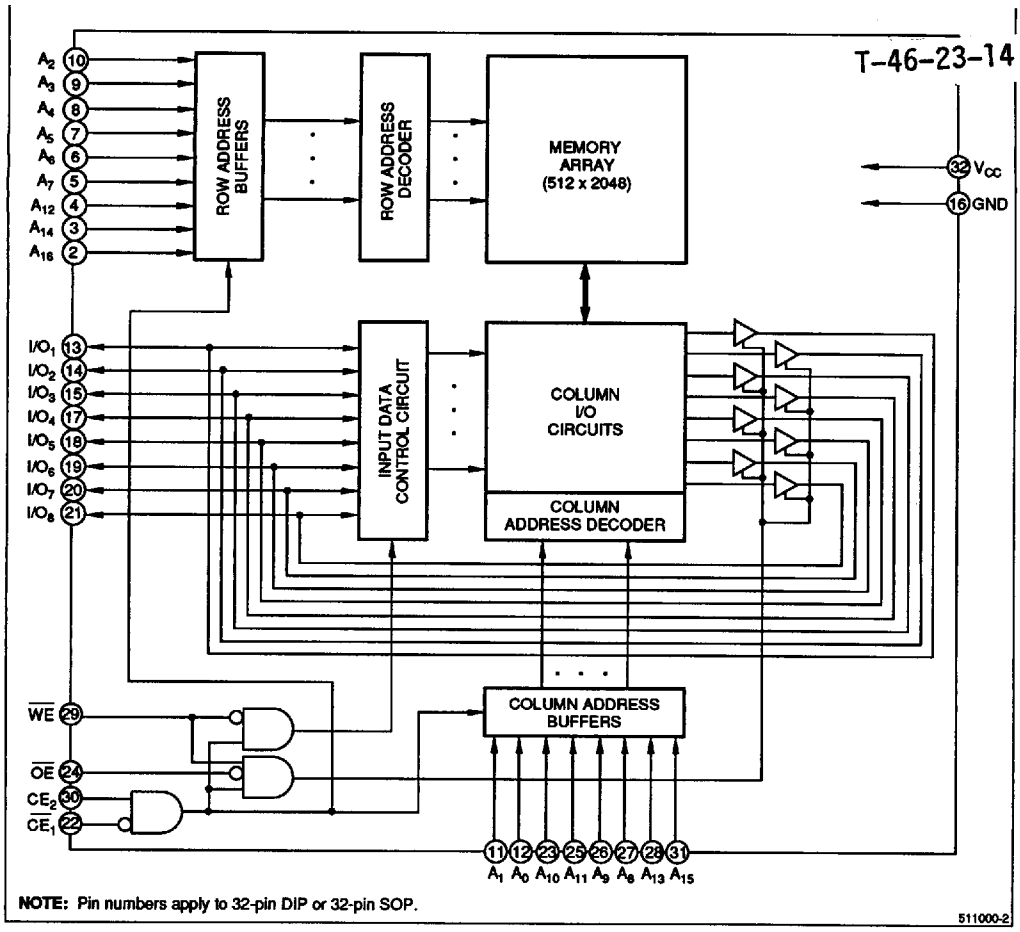

Figure 3. LH511000UL Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	STANDBY CURRENT	NOTE
H	X	X	X	Non selected	High-Z	Standby (I_{SB}, I_{SB1})	1
X	L	X	X	Non selected	High-Z	Standby (I_{SB}, I_{SB1})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output LOW voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output HIGH voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}			1	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}, or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 to V_{CC}			1	µA	
Operating current	I_{CC1}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Cycle = MIN. Outputs open			60	mA	
	I_{CC2}	$\overline{CE_1}$ ≤ 0.2 V, CE_2 ≥ V_{CC} - 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} - 0.2 V, Cycle = 1 MHz, Outputs open		1	6	mA	1
				5	15		2
Standby current	I_{SB1}	CE_2, $\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			3	mA	
	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$, CE_2 ≥ V_{CC} - 0.2 V			4	µA	3
					12		4

NOTES:
1. Read cycle
2. Write cycle
3. T_A = 0 to 70°C
4. T_A = -40 to +85°C

AC CHARACTERISTICS

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(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	100 ns		120 ns		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read cycle time	t_{RC}	100		120		ns
Address access time	t_{AA}		100		120	ns
Chip enable access time	t_{ACE1}		100		120	ns
	t_{ACE2}		100		120	ns
Output enable time	t_{OE}		50		60	ns
Output hold time	t_{OH}	10		10		ns
$\overline{CE}$ Low to output in Low-Z	t_{LZ1}	5		5		ns
	t_{LZ2}	5		5		ns
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns
$\overline{CE}$ High to output in High-Z	t_{HZ1}	0	35	0	45	ns
	t_{HZ2}	0	35	0	45	ns
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	35	0	45	ns

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH511000/N-10UL		LH511000/N-12UL		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write cycle time	t_{WC}	100		120		ns
$\overline{CE}$ Low to end of write	t_{CW}	80		100		ns
Address valid to end of write	t_{AW}	80		100		ns
Address setup time	t_{AS}	0		0		ns
Write recovery time	t_{WR}	0		0		ns
Write pulse width	t_{WP}	75		85		ns
Input data setup time	t_{DW}	40		50		ns
Input data hold time	t_{DH}	0		0		ns
$\overline{WE}$ High to output in High-Z	t_{OW}	0		0		ns
$\overline{WE}$ Low to output in High-Z	t_{WZ}	5		5		ns
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	35	0	45	ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + 100 pF (Includes scope and jig capacitance)

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CAPACITANCE (T_A = 25°C, f = 1MHz)

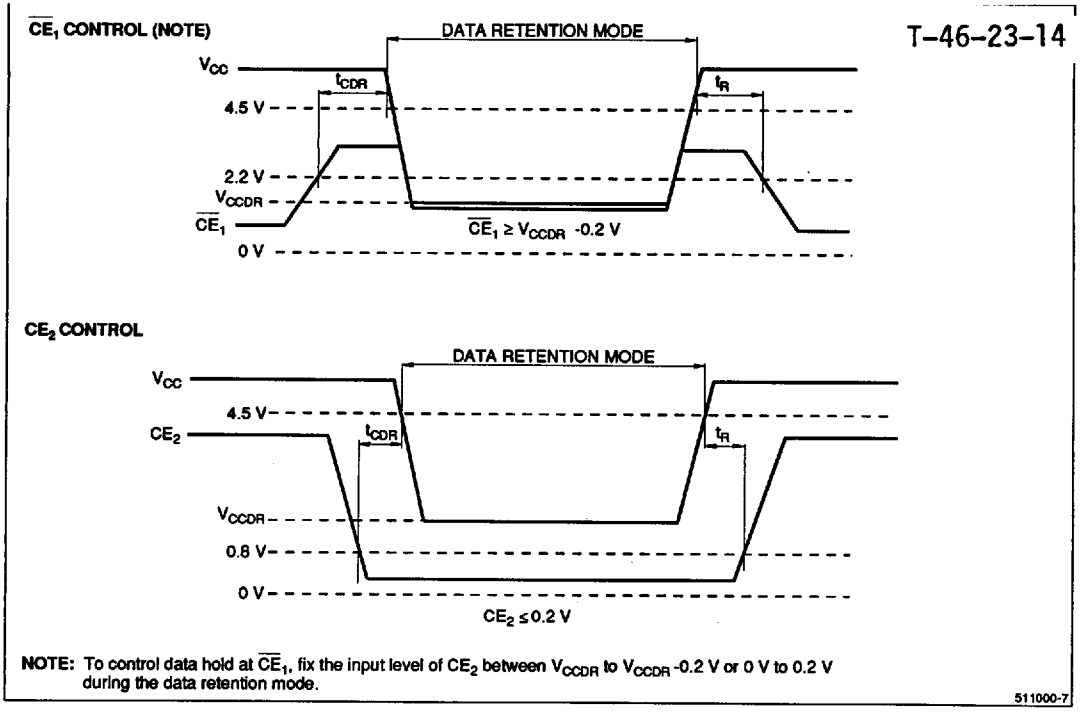
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V			10	pF	1
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF	1

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_2} \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V		2.0			V	
	I_{CCDR}	$\overline{CE_2} \le 0.2$ V, V_{CC} = 2 V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V V_{CC} = 3 V	25°C			0.1	µA	
			0 to 70°C			2	µA	
			-40 to 85°C			6	µA	
$\overline{CE}$ setup time	t_{CDR}			0			ns	
$\overline{CE}$ hold time	t_R			t_{RC}			ns	1

NOTE:
1. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE}_1$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention mode.

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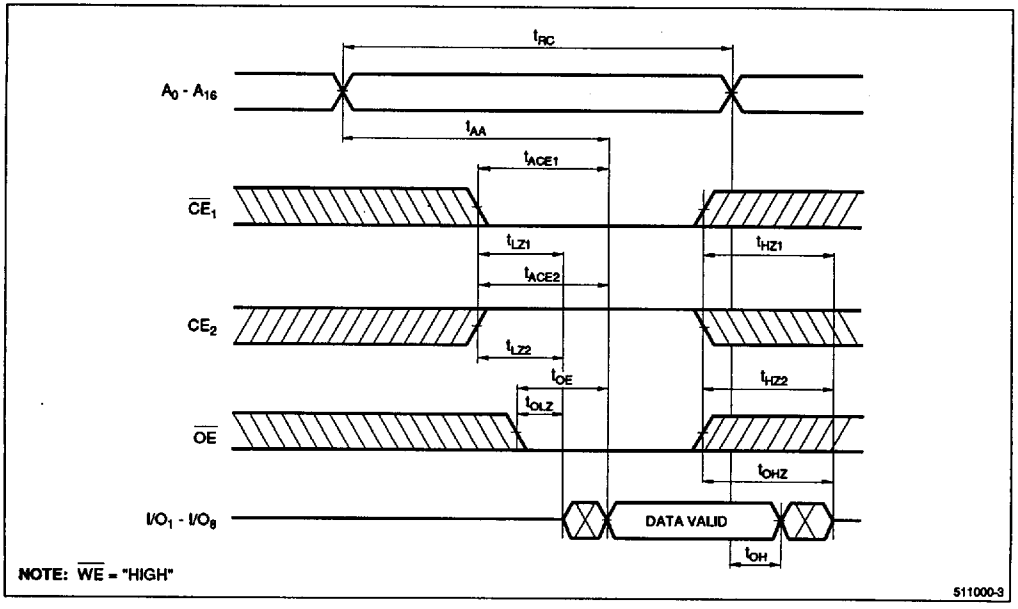
Figure 4. Low Voltage Data Retention



NOTE: $\overline{WE}$ = "HIGH"

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Figure 5. Read Cycle

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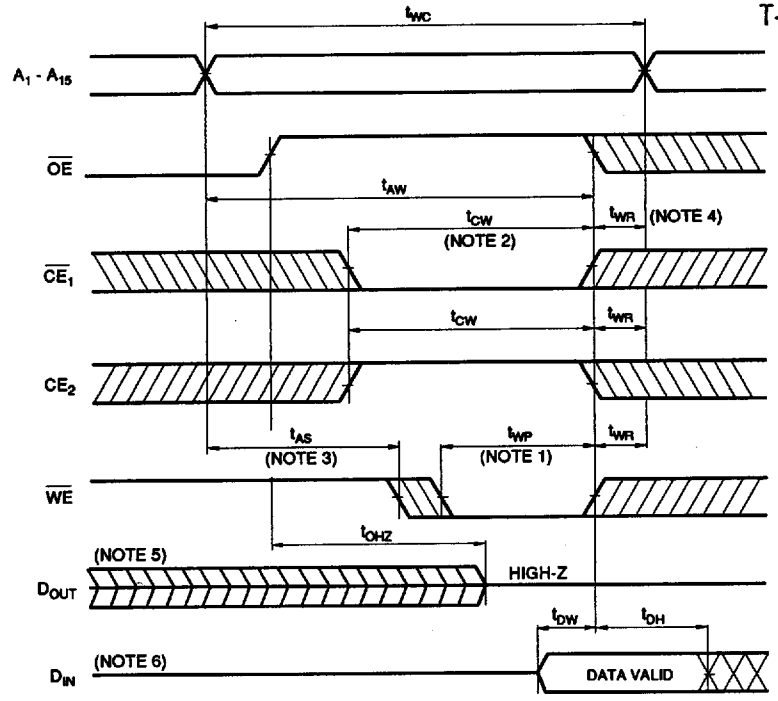

NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 6. Write Cycle 1

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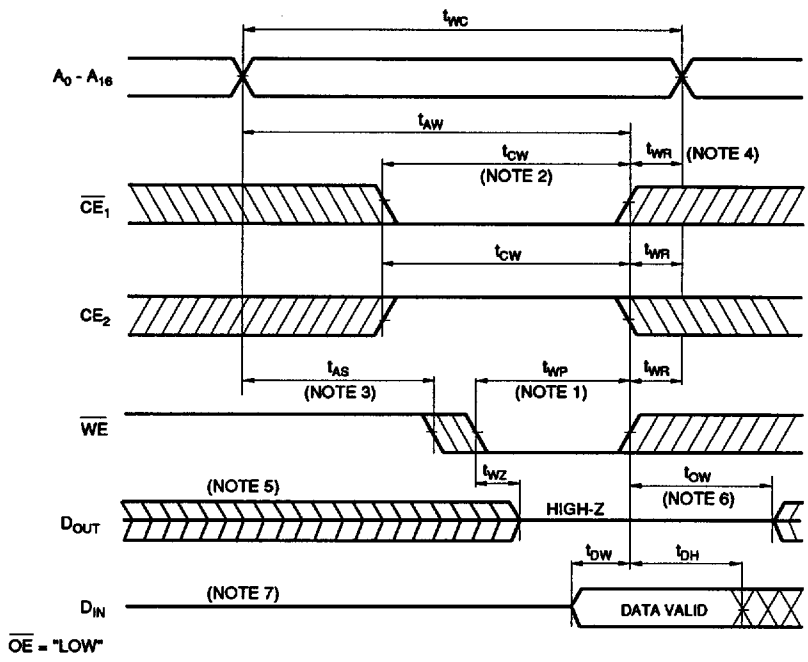

NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 7. Write Cycle 2

ORDERING INFORMATION

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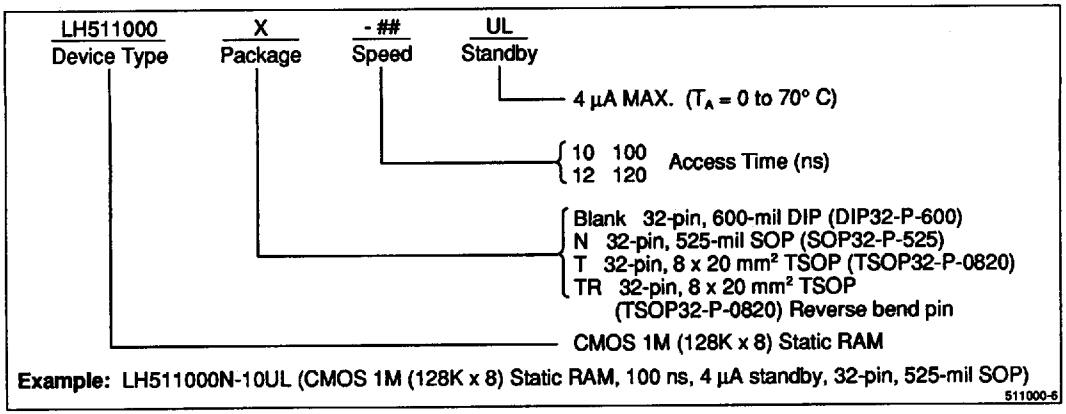

Example: LH511000N-10UL (CMOS 1M (128K x 8) Static RAM, 100 ns, 4 µA standby, 32-pin, 525-mil SOP)

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