HM514270/L Series — Preliminary

262,144-word × 16-bit Dynamic Random Access Memory

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM514270 are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM514270 have realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514270 offer fast page mode as a high speed access mode.
Multiplexed address input permits the HM514270 to be packaged in standard 400-mil 40-pin plastic SOJ, standard 475-mil 40-pin plastic ZIP and standard 400-mil 40-pin plastic TSOP II.

Features

- Single 5 V (±10%)
- High speed
  - Access time: 70 ns/80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 935 mW/825 mW/715 mW (max)
  - Standby mode: 11 mW (max)
    1.1 mW (max)(L-version)
- Fast page mode capability
- 512 refresh cycles: 8 ms
  128 ms (L-version)
- 2 $\overline{WE}$ byte control
- 3 variations of refresh
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- Battery back up operation (L-version)

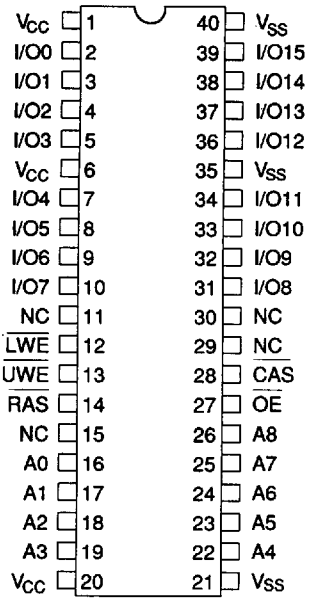
Ordering Information

Type No.	Access time	Package
HM514270JP-7	70 ns	400-mil 40-pin plastic SOJ (CP-40DA)
HM514270JP-8	80 ns	
HM514270JP-10	100 ns	
HM514270ZP-7	70 ns	475-mil 40-pin plastic ZIP (ZP-40)
HM514270ZP-8	80 ns	
HM514270ZP-10	100 ns	
HM514270TT-7	70 ns	400-mil 40-pin plastic TSOP II (TTP-40DB)
HM514270TT-8	80 ns	
HM514270TT-10	100 ns	
HM514270LJP-7	70 ns	400 mil 40-pin plastic SOJ (CP-40DA)
HM514270LJP-8	80 ns	
HM514270LJP-10	100 ns	
HM514270LZP-7	70 ns	475-mil 40-pin plastic ZIP (ZP-40)
HM514270LZP-8	80 ns	
HM514270LZP-10	100 ns	
HM514270LTT-7	70 ns	400-mil 40-pin plastic TSOP II (TTP-40DB)
HM514270LTT-8	80 ns	
HM514270LTT-10	100 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

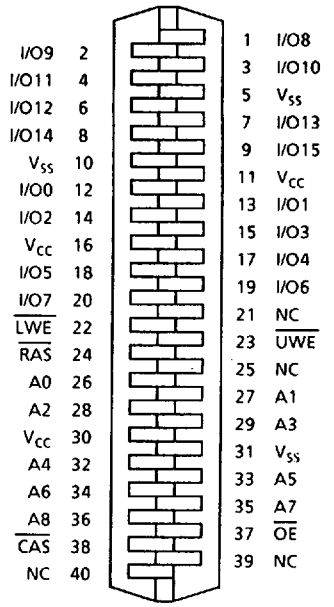
Pin Arrangement

HM514270JP/LJP Series



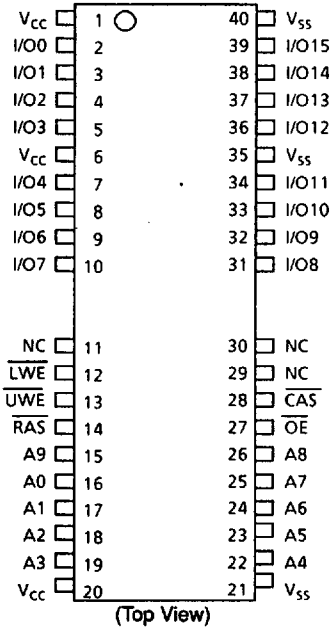
(Top View)

HM514270ZP/LZP Series



(Bottom View)

HM514270TT/LTT Series



(Top View)

Pin Description

Pin name	Function
A0 – A8	Address input – Row address A0 – A8 – Column address A0 – A8 – Refresh address A0 – A8
I/O0 – I/O15	Data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{UWE}$,$\overline{LWE}$	Read/write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

Block Diagram

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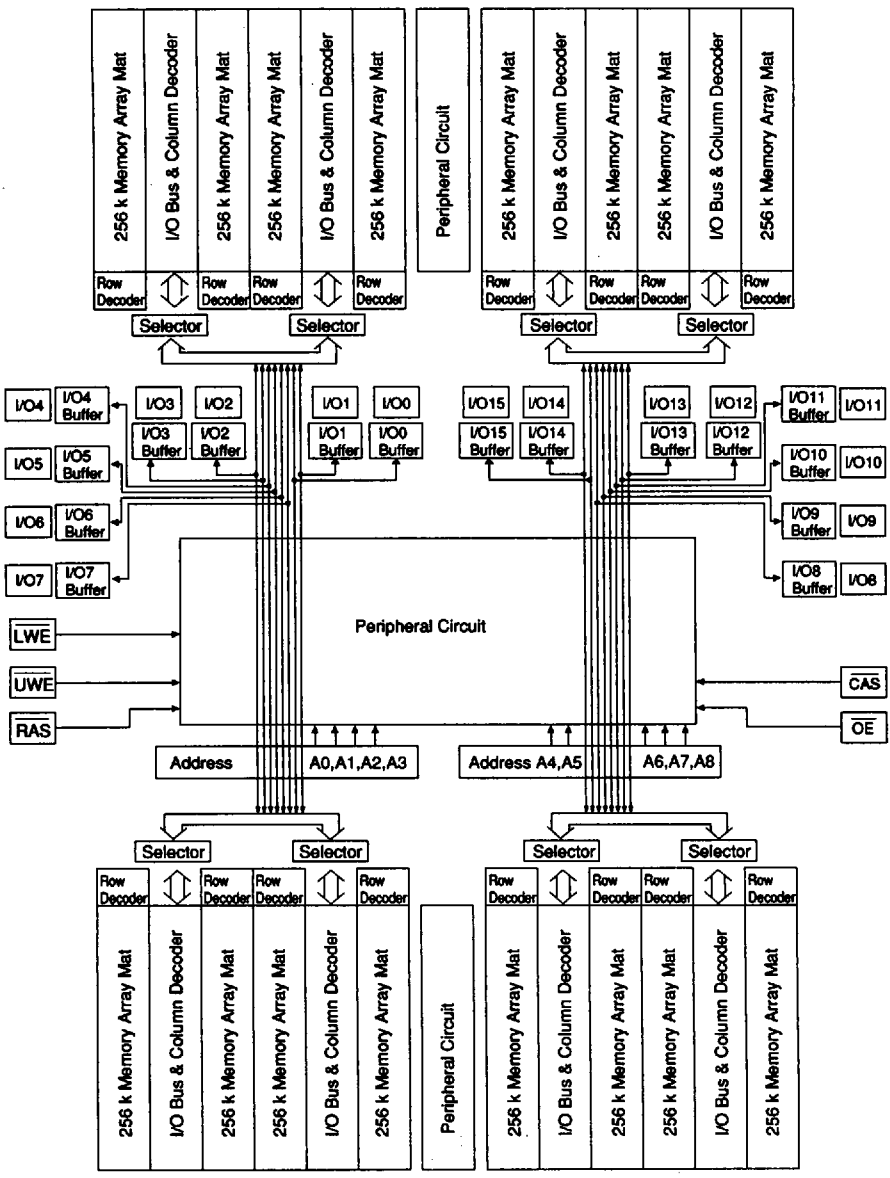


Truth Table

Inputs					I/O		
$\overline{RAS}$	$\overline{LWE}$	$\overline{UWE}$	$\overline{CAS}$	$\overline{OE}$	I/O0 – I/O7	I/O8 – I/O15	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	H	H	L	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	H	H	L	H	High-Z	High-Z	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin)	V_{IL}	–1.0	—	0.8	V	1
	(Others)	V_{IL}	–2.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514270/L-7		HM514270/L-8		HM514270/L-10				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	170	—	150	—	130	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)		—	200	—	200	—	200	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	150	—	130	—	110	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	150	—	130	—	110	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	130	—	120	—	110	mA	t_{PC} = min	1, 3
Battery back up current (Standby with CBR refresh) (L-version)	I_{CC10}	—	300	—	300	—	300	µA	Standby: CMOS interface Dout = High-Z CBR refresh: t_{RC} = 250 µs t_{RAS} ≤ 1 µs, $\overline{CAS}$ = V_{IL} $\overline{LWE}$, $\overline{UWE}$, OE = V_{IH}	4
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *14, *15, *17, *18

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514270/L-7		HM514270/L-8		HM514270/L-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	15	—	15	—	15	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (cont)

		HM514270/L-7		HM514270/L-8		HM514270/L-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

		HM514270/L-7		HM514270/L-8		HM514270/L-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	16
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514270/L-7 Min	HM514270/L-7 Max	HM514270/L-8 Min	HM514270/L-8 Max	HM514270/L-10 Min	HM514270/L-10 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	25	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	20	—	ns	11
$\overline{CAS}$ to $\overline{OE}$ delay time	t_{COD}	—	0	—	0	—	0	ns	18

Read-Modify-Write Cycle

Parameter	Symbol	HM514270/L-7 Min	HM514270/L-7 Max	HM514270/L-8 Min	HM514270/L-8 Max	HM514270/L-10 Min	HM514270/L-10 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	60	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514270/L-7 Min	HM514270/L-7 Max	HM514270/L-8 Min	HM514270/L-8 Max	HM514270/L-10 Min	HM514270/L-10 Max	Unit	Note
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514270/L-7 Min	HM514270/L-7 Max	HM514270/L-8 Min	HM514270/L-8 Max	HM514270/L-10 Min	HM514270/L-10 Max	Unit	Notes
Fast page mode cycle time	t_{PC}	50	—	55	—	60	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	15	—	15	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	65	—	70	—	85	—	ns	
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	110	—	ns	

Counter Test Cycle

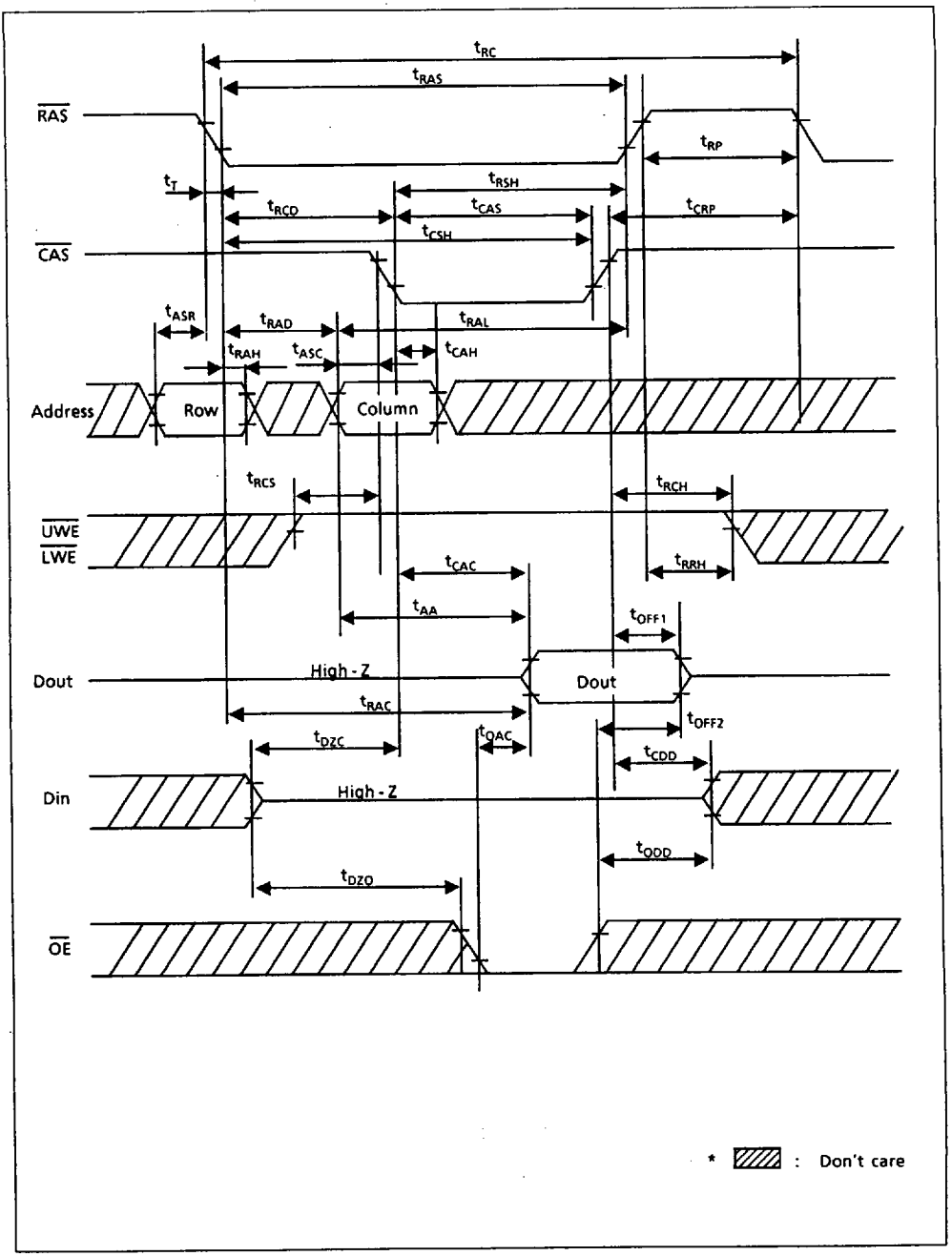
Parameter	Symbol	HM514270/L-7 Min	HM514270/L-7 Max	HM514270/L-8 Min	HM514270/L-8 Max	HM514270/L-10 Min	HM514270/L-10 Max	Unit	Note
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	50	—	50	—	50	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

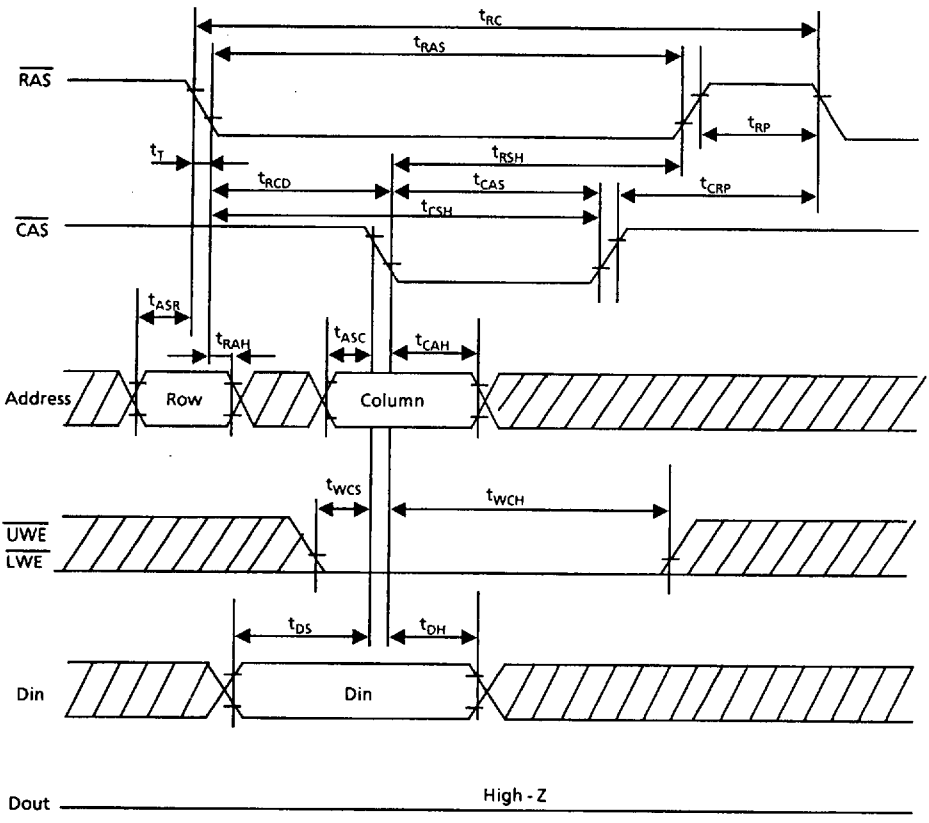
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.
17. When both $\overline{LWE}$ and $\overline{UWE}$ go low at the same time, all 16-bits data are written into the device. $\overline{LWE}$ and $\overline{UWE}$ cannot be staggered within the same write cycles.
18. Do not enable Dout buffer when using delayed write timing.

Timing Waveforms

Read Cycle



Early Write Cycle



* ▨ : Don't care

** $\overline{OE}$: Don't care

Delayed Write Cycle

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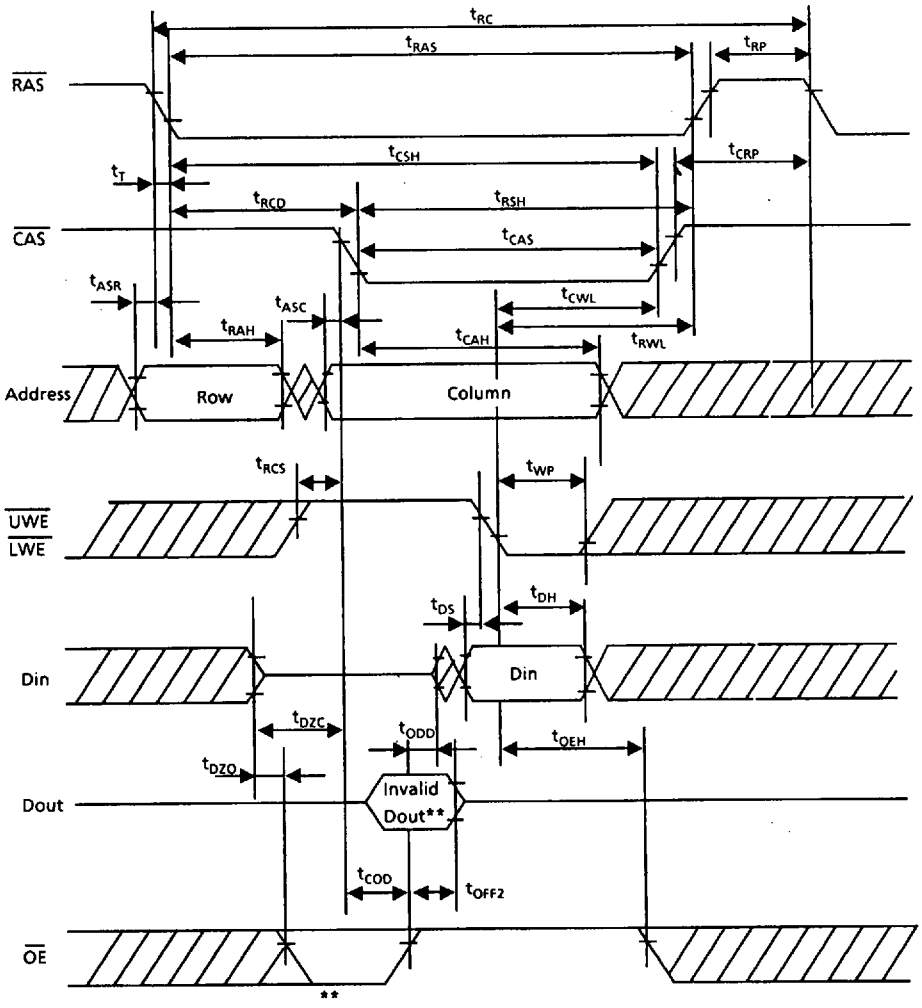
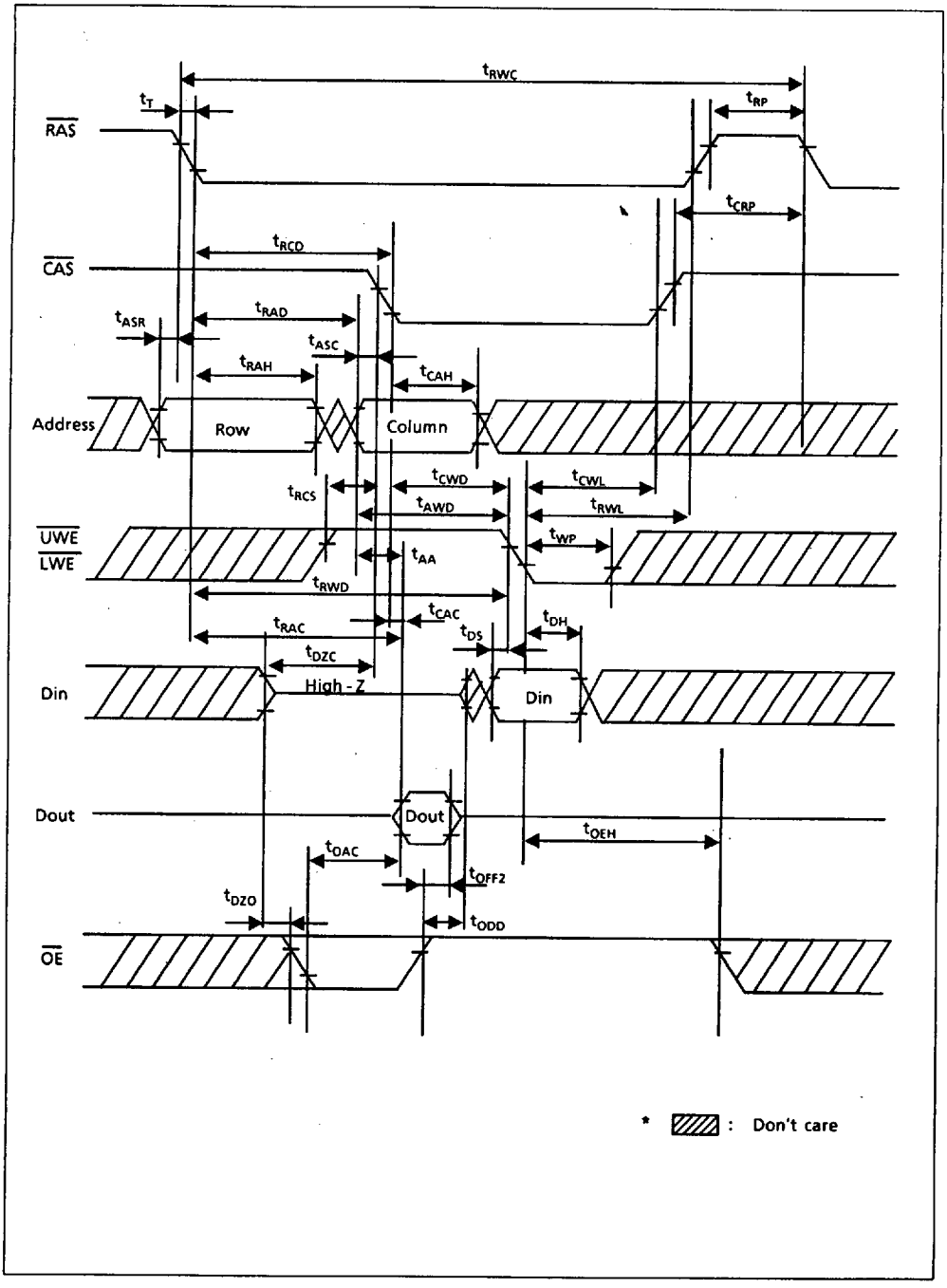


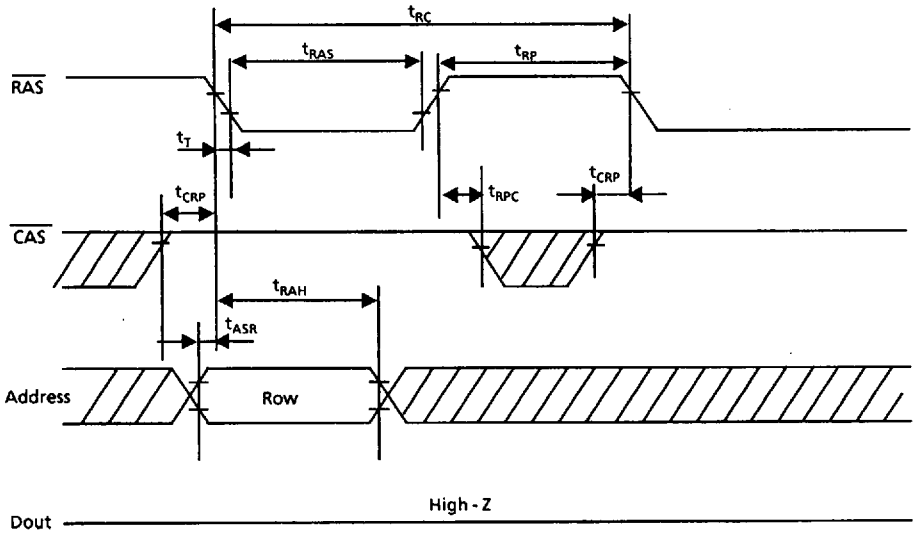
* ▨ : Don't care

** Invalid Dout comes out, when $\overline{OE}$ is low level.

Read-Modify-Write Cycle



$\overline{RAS}$-Only Refresh Cycle

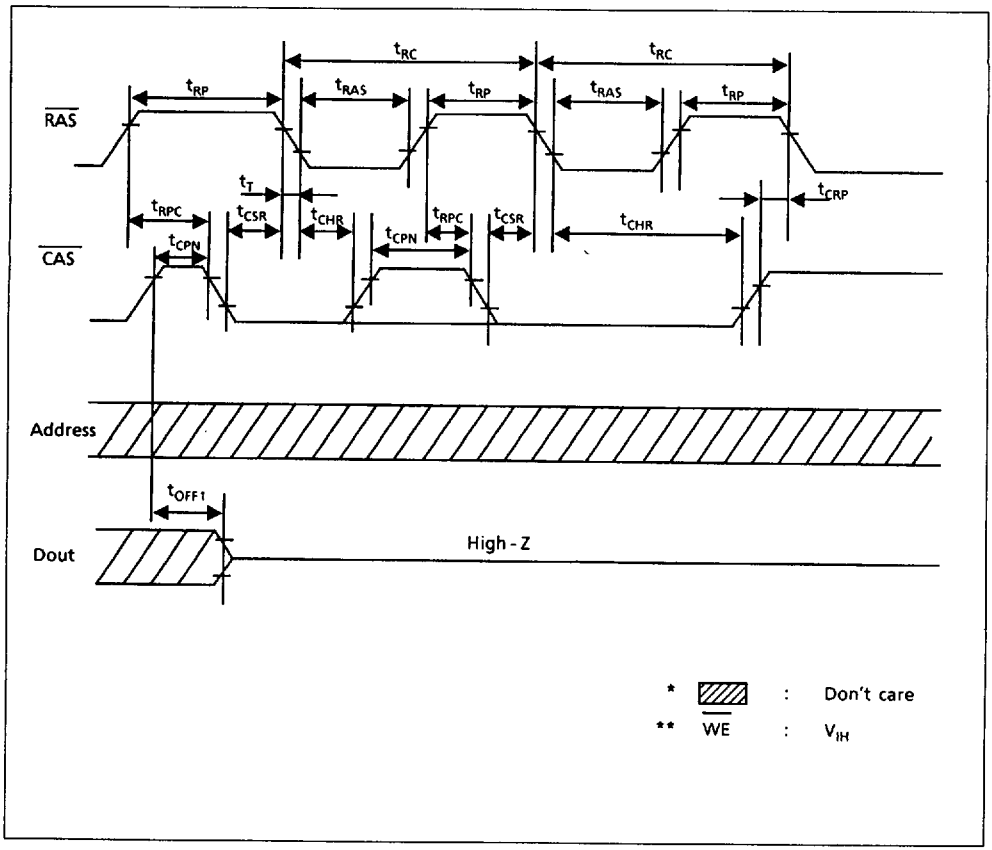


* $\overline{OE}$, $\overline{WE}$: Don't care

** ▨ : Don't care

*** Refresh address : A0 - A8 (AX0 - AX8)

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle

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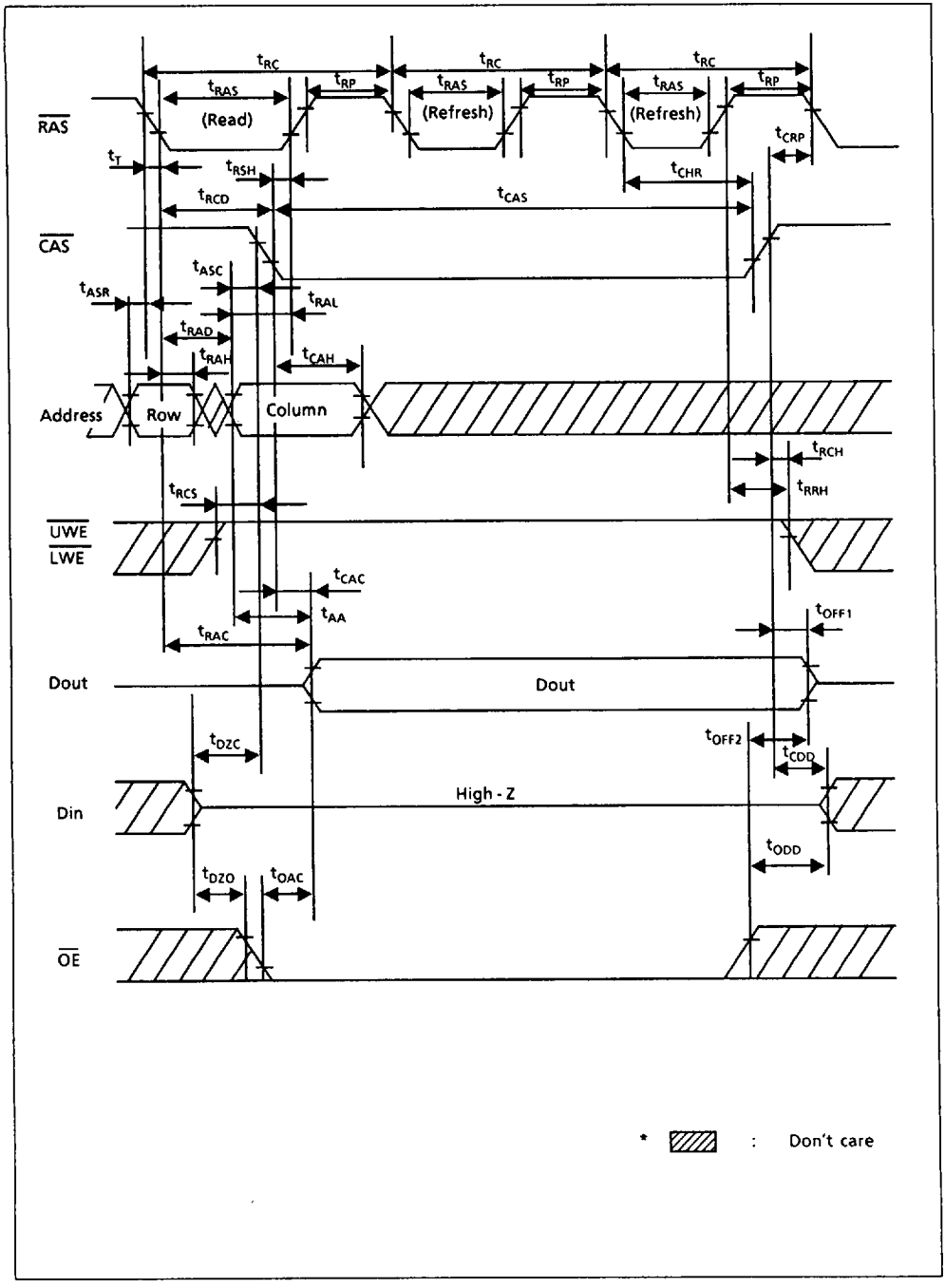
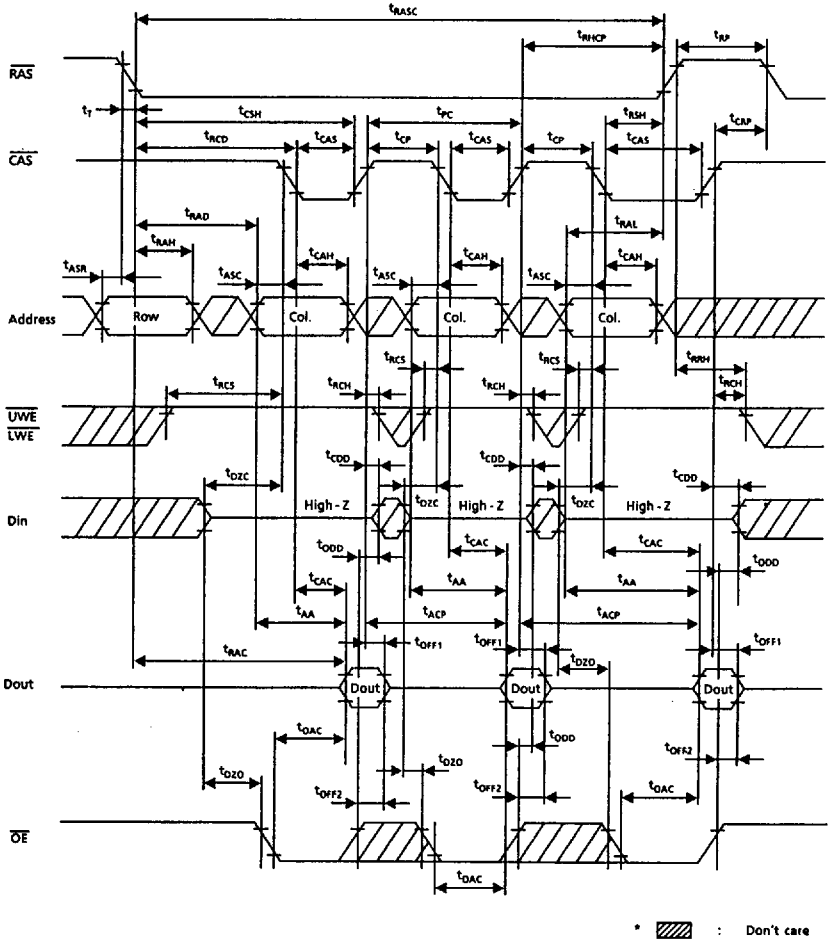


Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle

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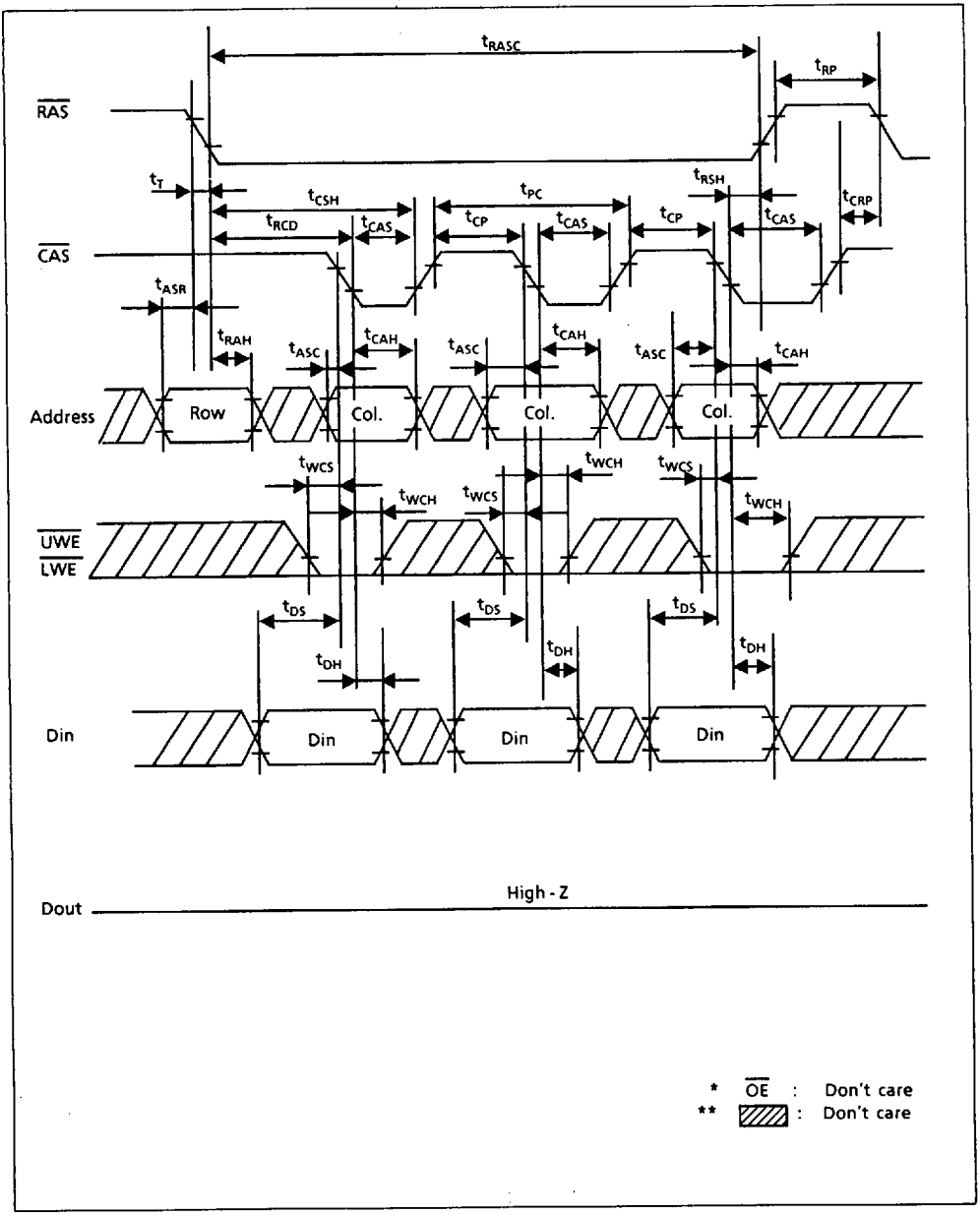
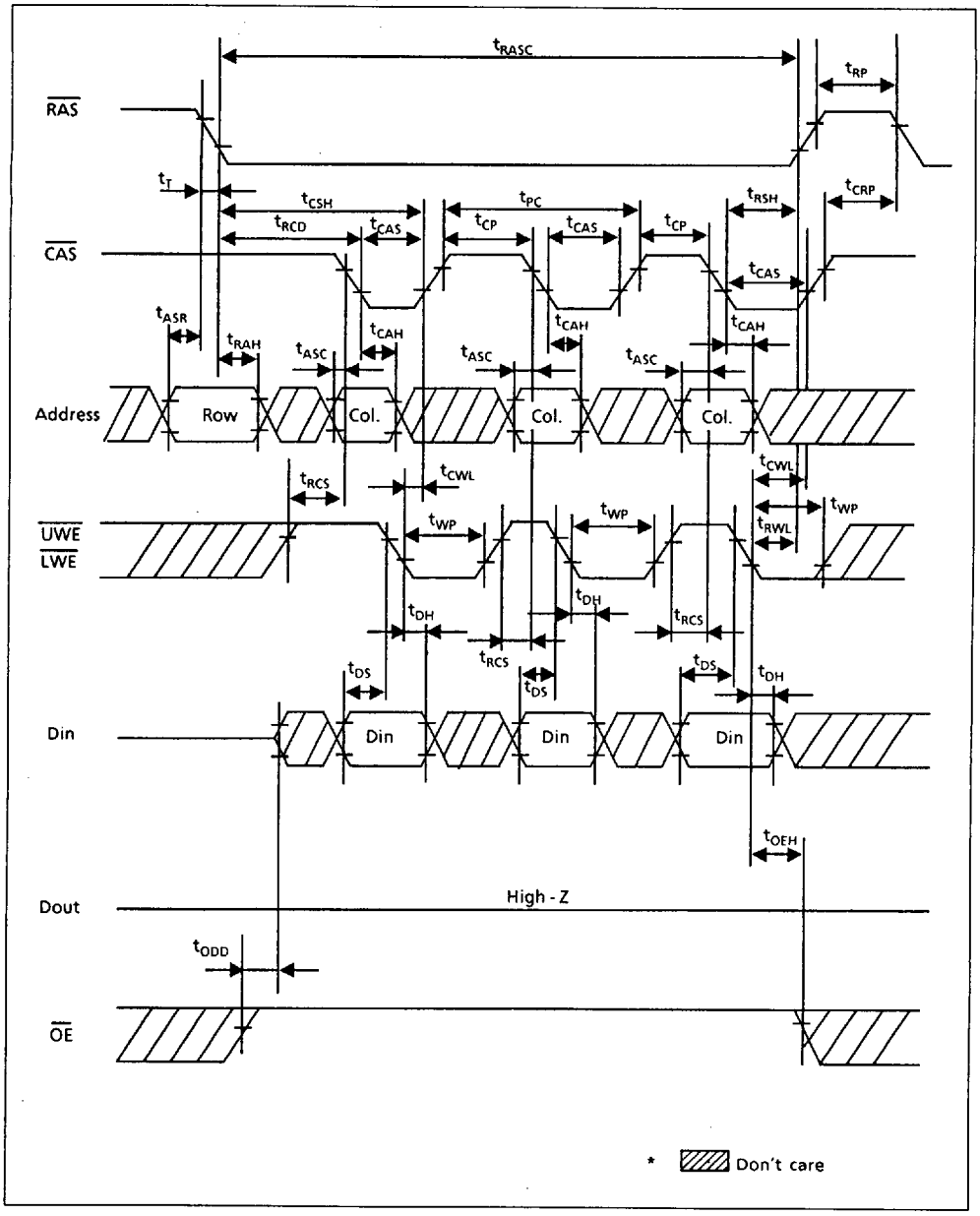
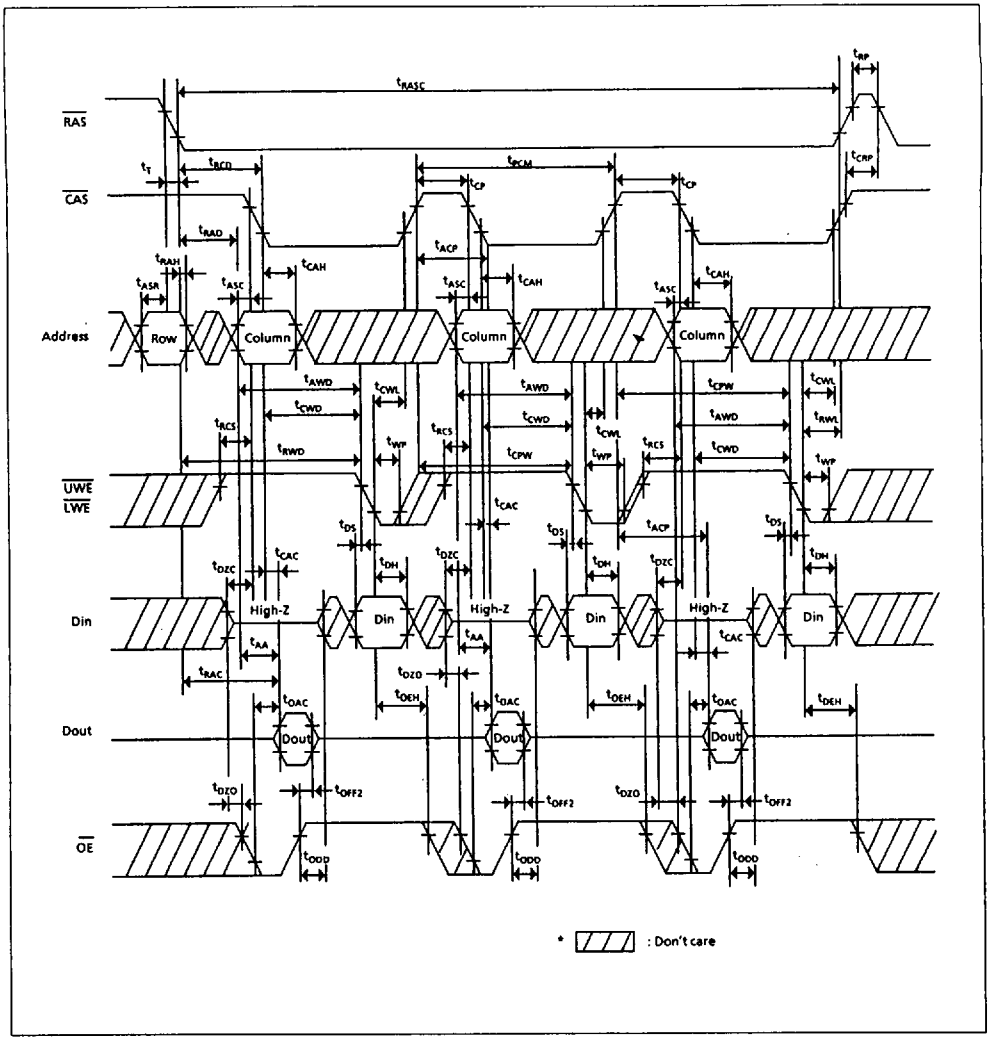


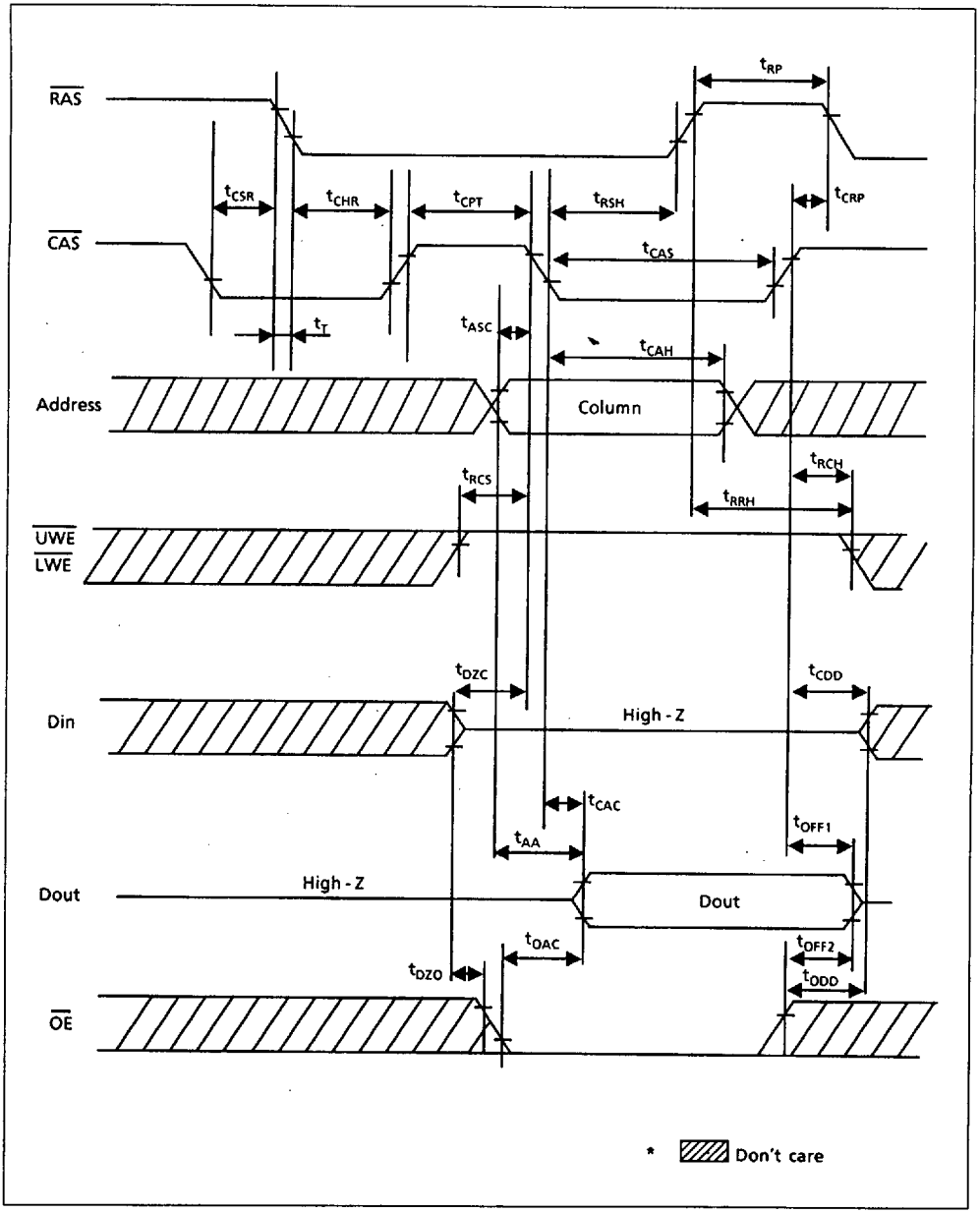
Fast Page Mode Delayed Write Cycle



Fast Page Mode Read-Modify-Write Cycle



CAS-Before-RAS Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)